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3D Integration Technology Basics and Its Impact on Design

Mustafa Badaroglu & Pol Marchal

IMEC, Leuven, Belgium

FWI: Workshop on Technology-Architecture Interaction
Emerging Technologies and Their Impact on Computer Architecture
June 19, 2010



Held in conjunction with the 37th International Symposium on Computer Architecture (ISCA-37).
Saint-Malo, France, June 19-23, 2010

OUTLINE

Technology-architecture interaction in 3D

Technology description

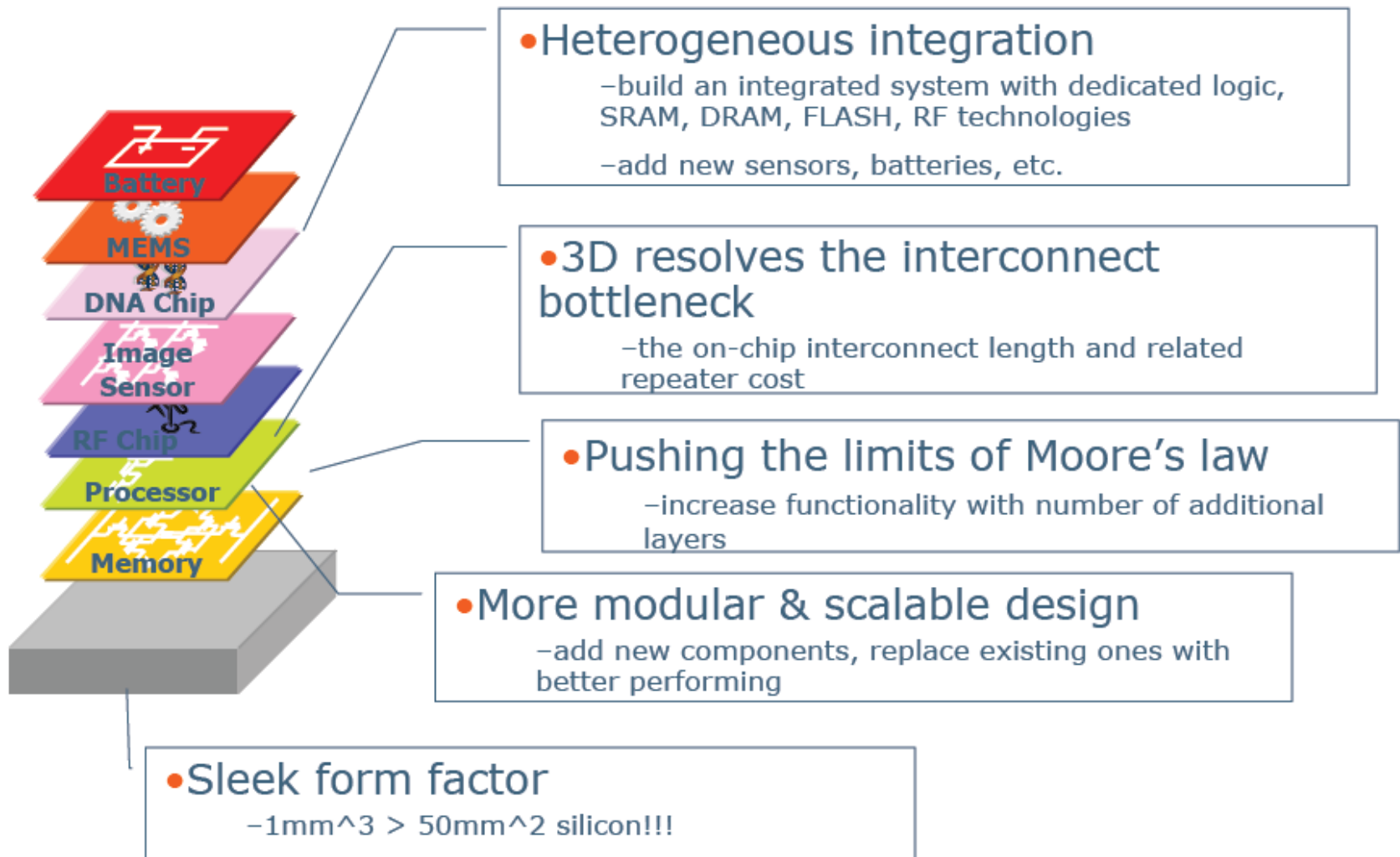
TSV characterization data and DC/AC behavior

Chip package interactions

Design flow for 3D

Conclusions

3D TECHNOLOGY – WHY?



3D TECHNOLOGY – SYSTEM BENEFITS

BANDWIDTH

Compute systems (servers)
Performance, Power efficiency,
heat dissipation, Reliability

Innovations
3D memory systems
3D solid state drives
3D cooling solutions

Mobile systems
Cost, Power, Form factor ,
Performance

Innovations
3D DRAM
3D MEMS & CIS

REUSE

Consumer
Cost, Power, Performance,
Form factor,

Innovations
3D DRAM for graphics

3D Integration &
advanced packaging

- Architectural solutions
- Power efficient performance (BW/mW)
- Platform for MtM technologies

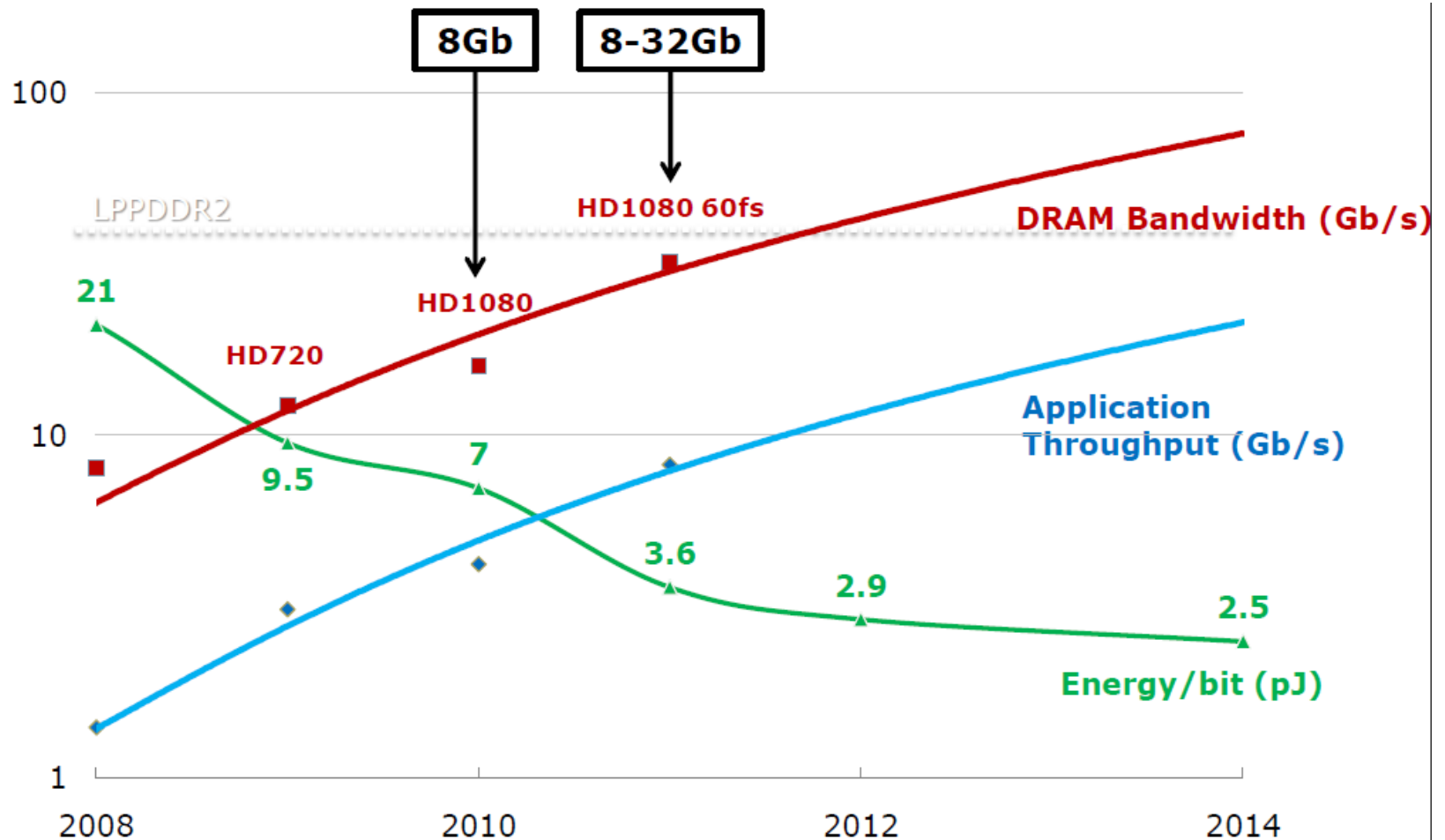
MODULARITY

Healthcare
Form-factor, power, reliability

Innovations
eCubes

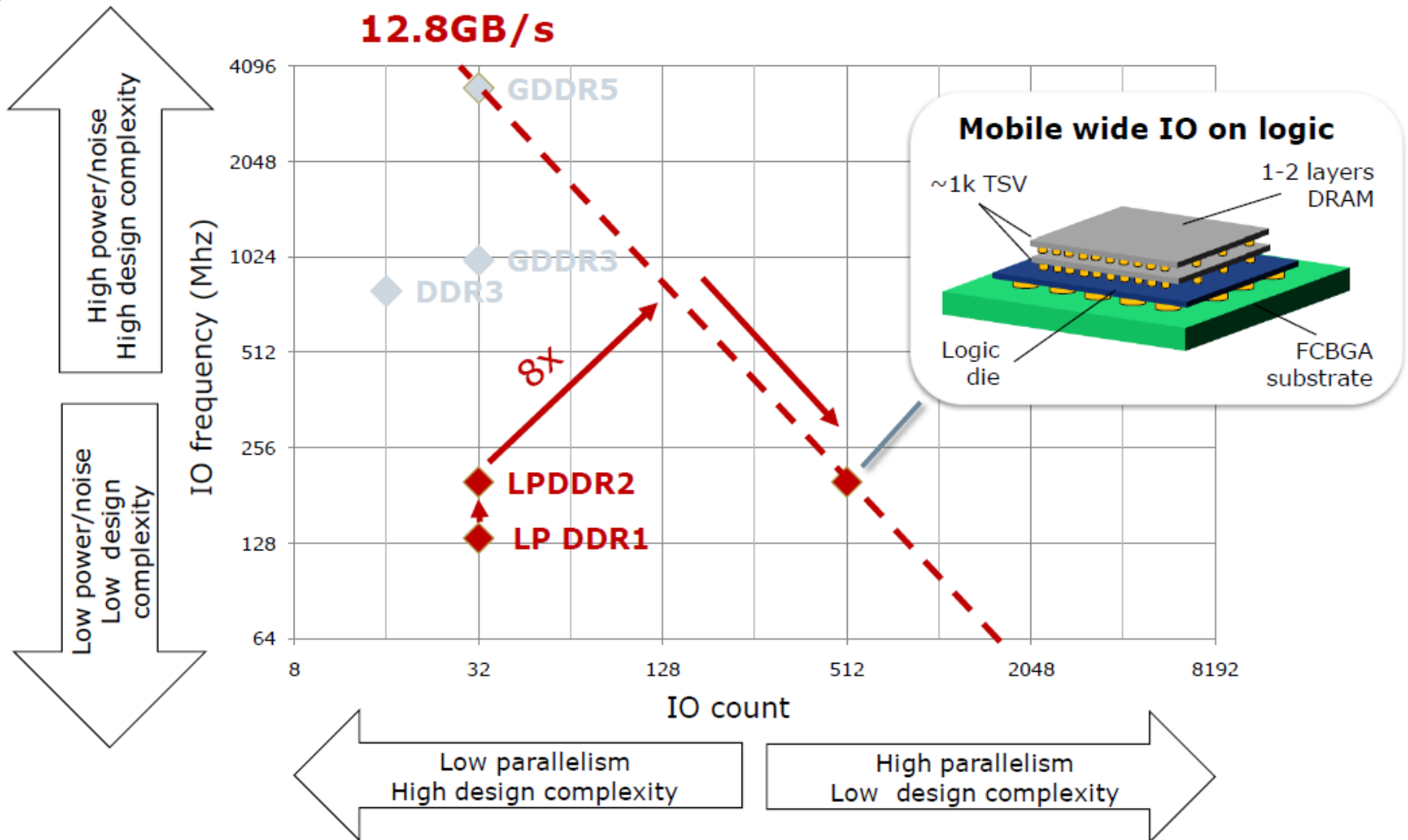
FORMFACTOR

BANDWIDTH VERSUS APPLICATION REQUIREMENTS



[Source: STE. ISSCC2010]

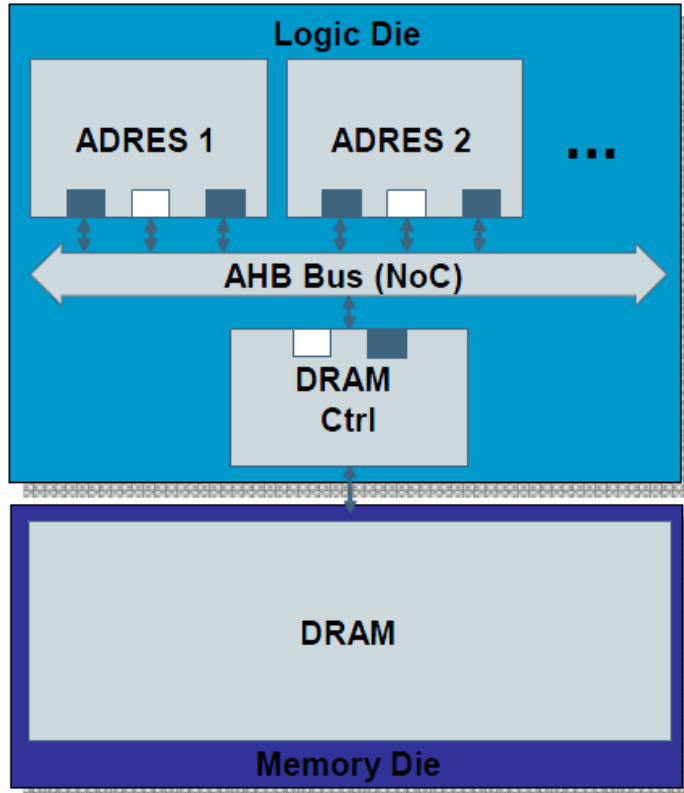
NEED FOR 3D INTEGRATION



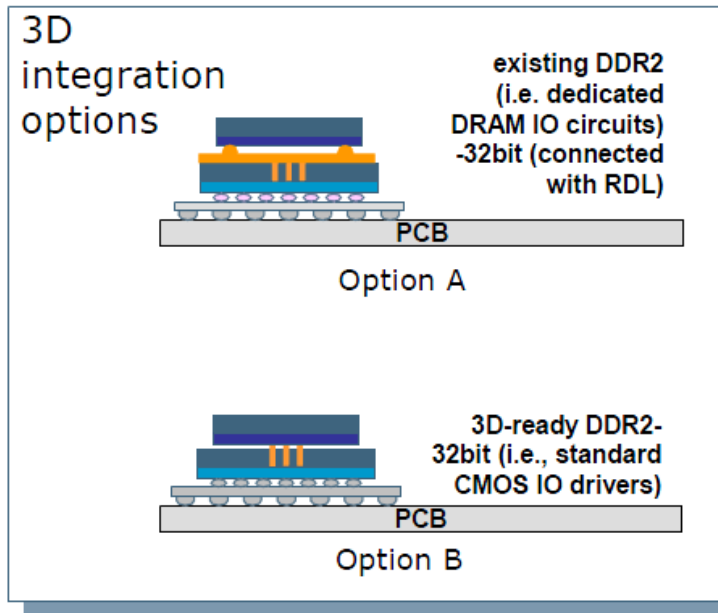
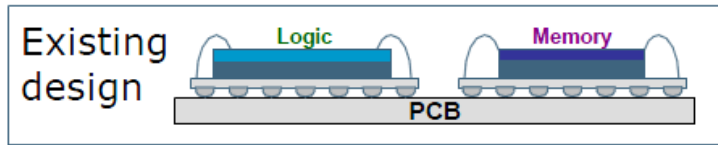
COST/POWER/PERFORMANCE TRADE-OFFS FOR DIFFERENT 3D INTEGRATION SCHEMES?



IMEC AVC-H264



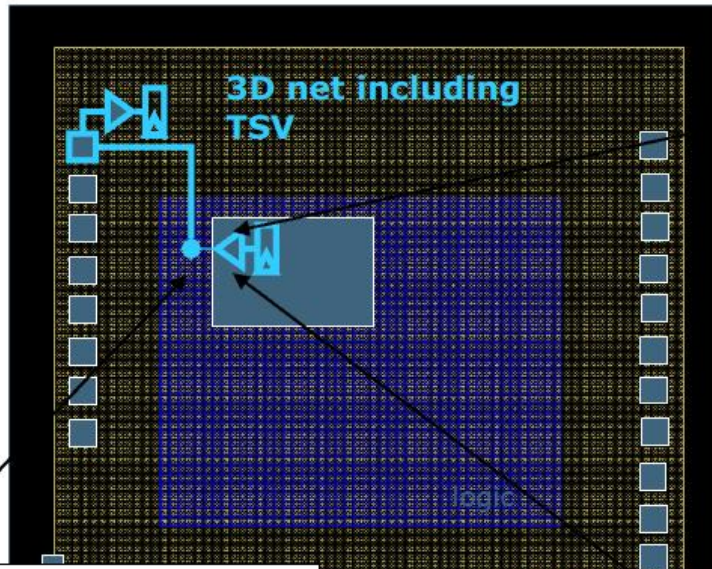
System: IMEC AVC-H264
in TSMC 90nm CMOS



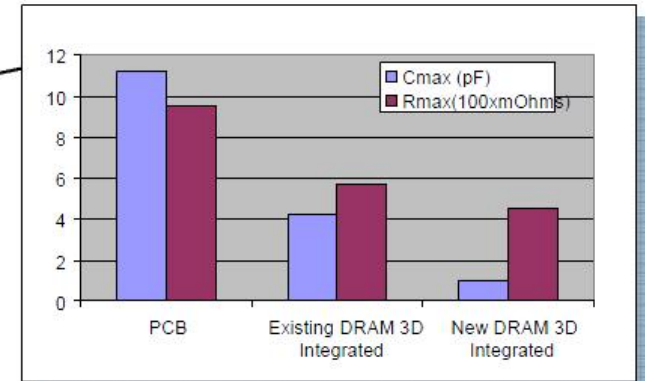
3D integration options

- ▶ 2D DRAM using standard I/O circuits
- ▶ 3D-ready using optimized drivers

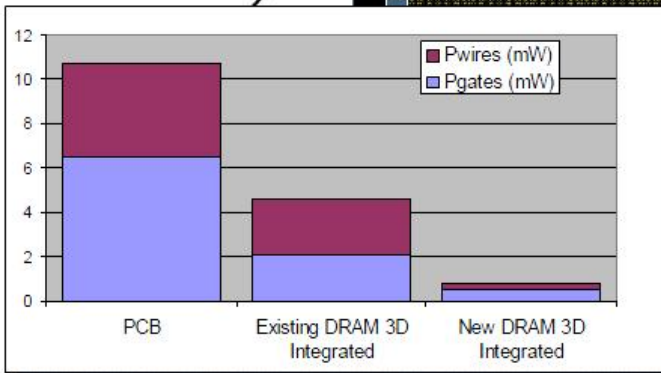
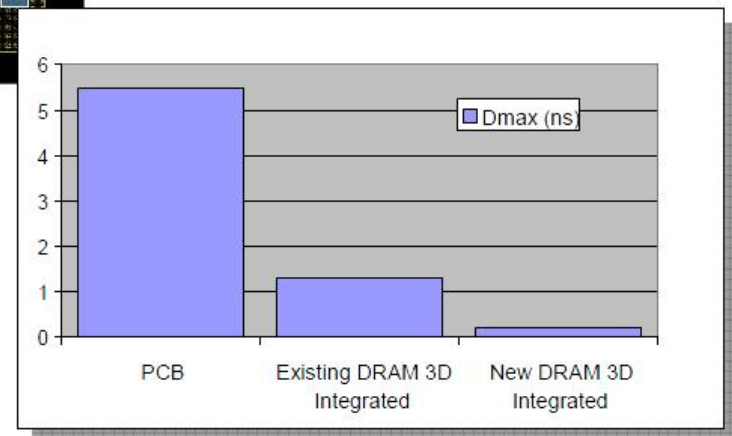
ANSWERING QUESTIONS



RC extraction of 3D Nets



Delay of 3D nets



Power of 3D nets

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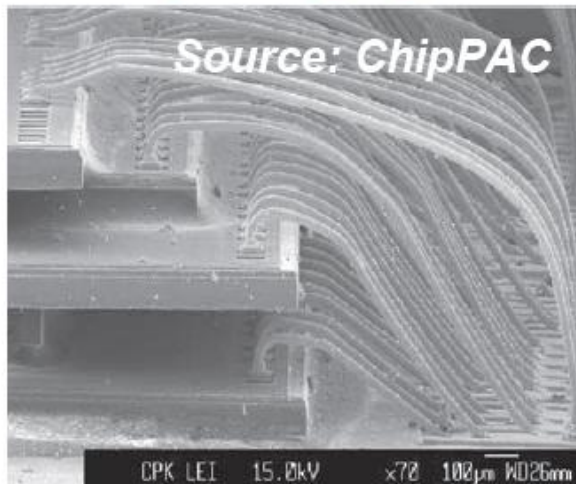
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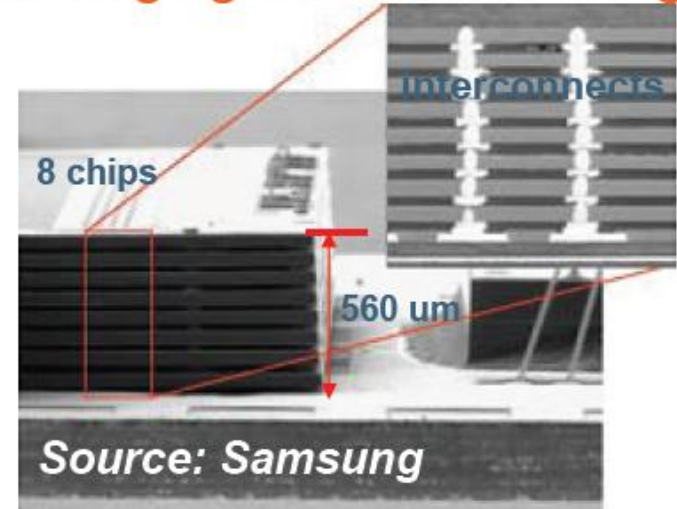
TODAY'S 3D TECHNOLOGIES

Established 3D packaging technology



- Limitations
 - Peripheral bonds only
 - Limited rerouting capabilities in laminate substrate
 - Long wire bonds (high inductance, high crosstalk, low speed interconnect)
- ➔ For applications with low-density interconnects and with specific I/O pad routing

Emerging 3D TSV technology



- Limitations
 - Often serial via processing limited to low number of interconnects
 - Limited scalability
- ➔ For applications with intermediate-density / intermediate-bandwidth interconnects

3D INTERCONNECT FLAVORS

- **3D-SIP: Traditional packaging & interconnection technologies**

- Wire-bonded die stack
- Stacking of packages: preferably SIP packages
- 3D interconnects realized at **1st packaging interconnect level**

Package level
interconnect



- **3D-WLP: Wafer-level packaging**

WLP: technology used for flip chip bumping, redistribution and CSP technology

- 3D interconnects realized at wafer level
- 3D interconnects processed *post IC passivation*
- 3D interconnects realized at **0-level packaging interconnect**

Through-Si interconnect
(TSV)



- **3D-SIC and 3D-IC: IC-foundry technology**

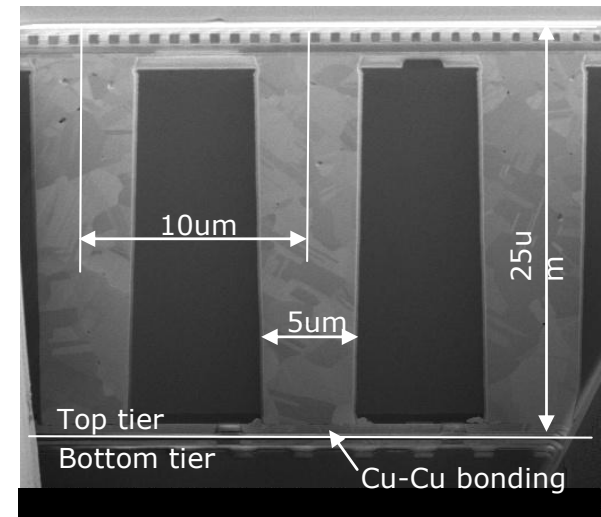
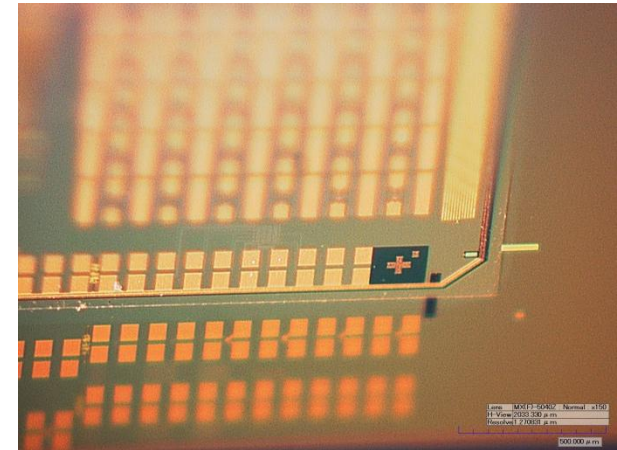
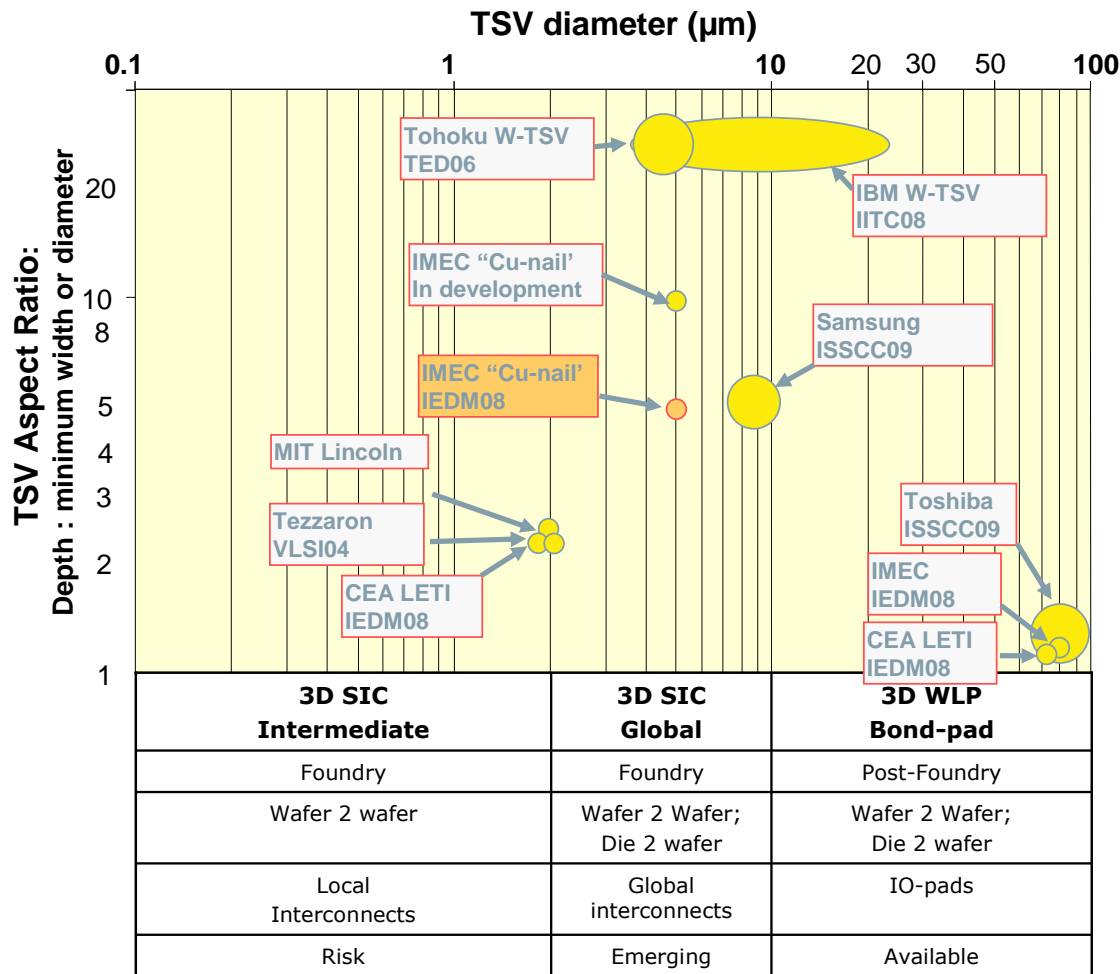
- 3D interconnects realized at wafer level
- 3D interconnects processed *post Front End and prior to Back End local interconnects*
- 3D interconnects at **intermediate and global interconnect levels (3D-SIC)** or **local (3D-IC)**

BENCHMARKING OF DIFFERENT 3D OPTIONS

	3D-SIP	3D-WLP		3D-SiC	
		UTCS	VIA-1	VIA-2	
3D Interconnect Technology	Package interposer	Embedded Thin die	Conformal Cu TSV	Cu-Filled TSV	Cu-nail TSV
Interconnect density	‘package-to-package’	‘around’ die	Through Si	Through Si	Through Si
Peripheral	2 - 3 /mm	10 - 50 /mm	6 - 20 /mm	25 - 50 /mm	≥100 /mm
Area-array	4 - 11 /mm ²	100 - 2.5k/mm ²	44 - 400 /mm ²	625 - 2.5k/mm ²	≥ 10k/mm ²
3D-TSV pitch	-	-	50 - 150 μm	20-40 μm	≤ 10 μm
3D-Interconnect pitch	300 - 500 μm	20 - 100 μm	-	-	-
3D-TSV diameter			40 - 100 μm	15 - 25 μm	1 - 5 μm
Die thickness	50 μm	10 - 20 μm	50 - 100 μm	25 - 50 μm	10 - 20 μm

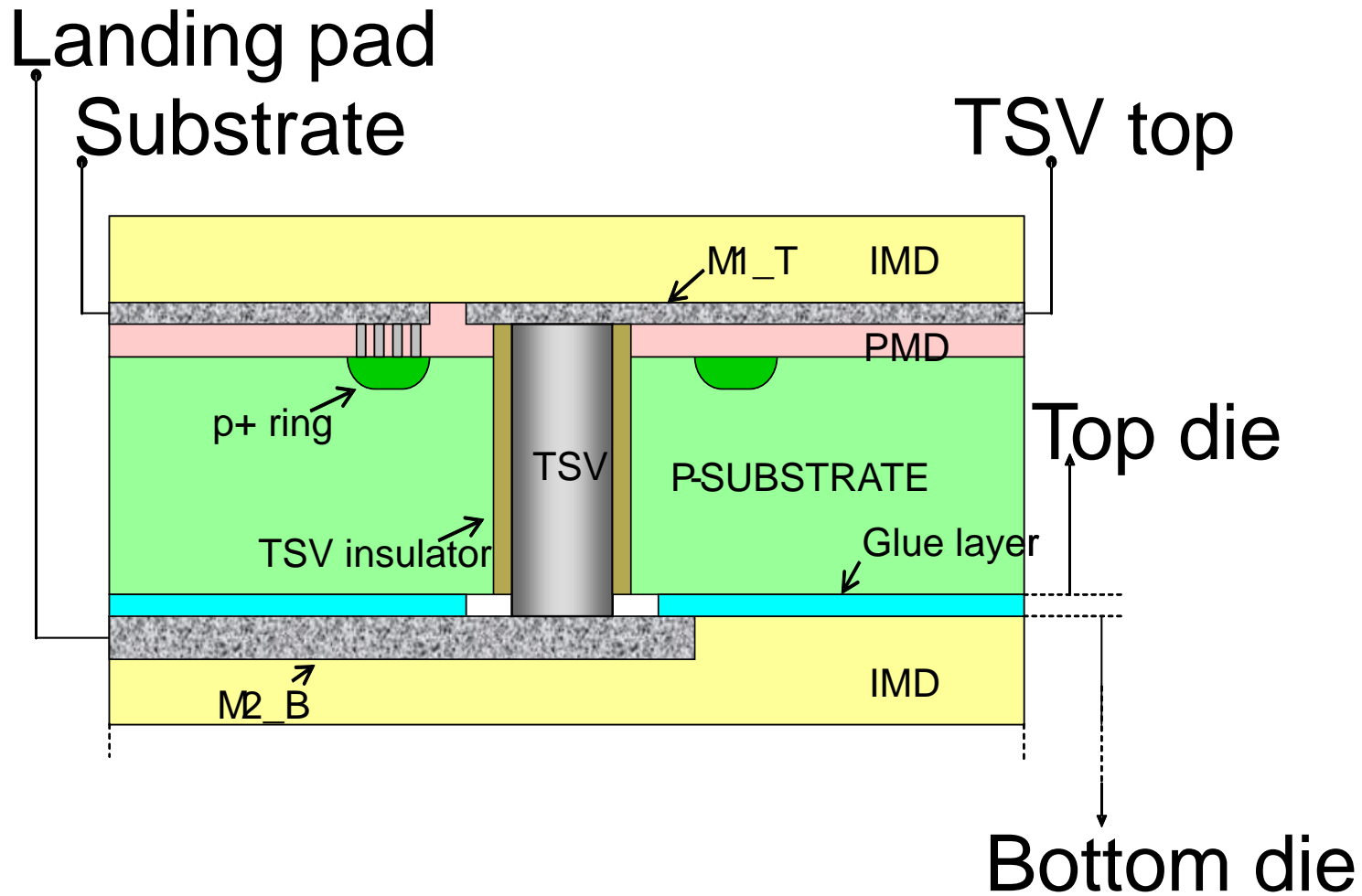
This presentation

FOCUS ON 3D SIC TECHNOLOGY

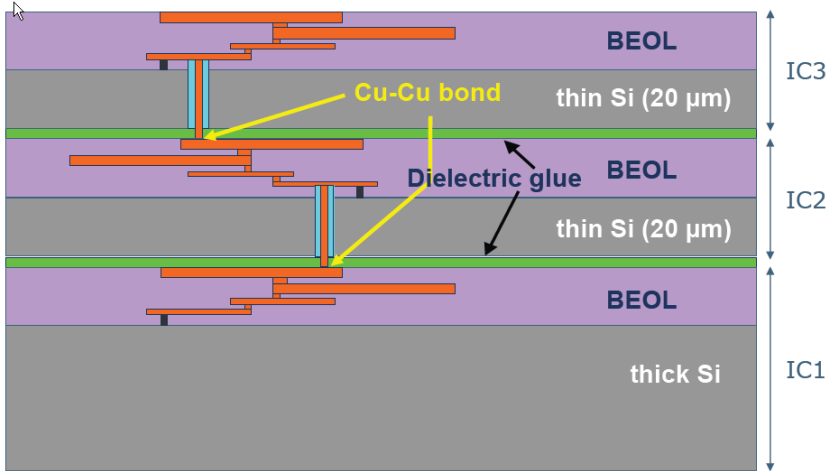


TSV resistance	~20 [40]mΩ
TSV capacitance	37 [74]fF(depletion)

THRU SILICON VIA (TSV) CROSS SECTION



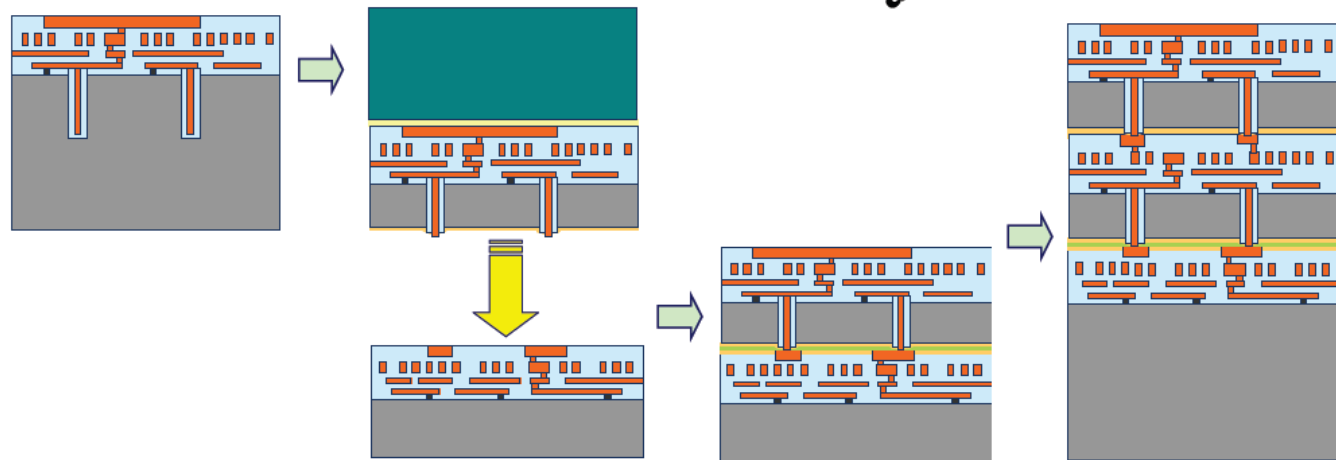
3D-SIC PROCESSING: TSV, THINNING, AND COLLECTIVE DIE TO WAFER BONDING



• Via processing

• Extreme thinning

• Pick-and-place and bonding



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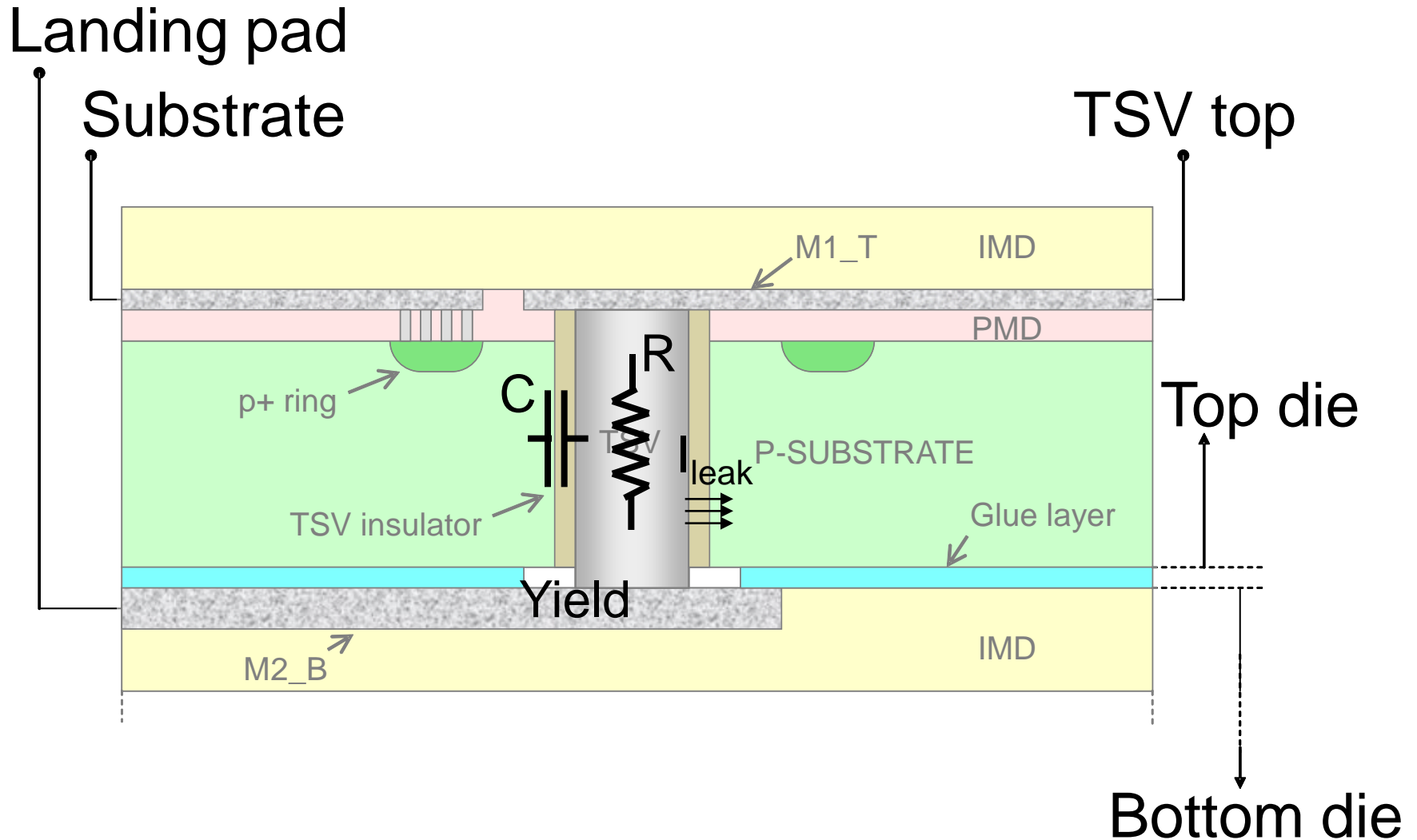
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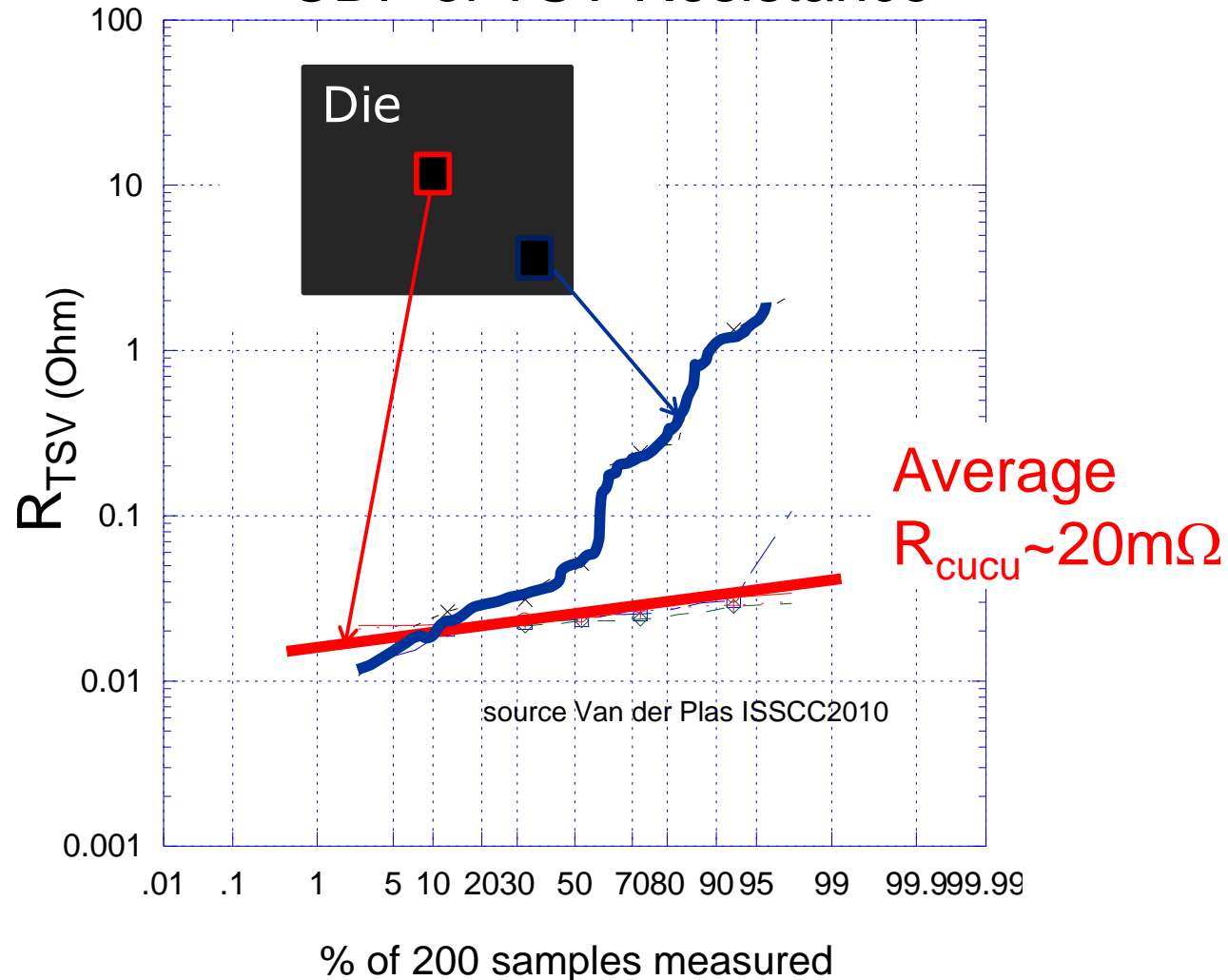
Conclusions

TSV CHARACTERISTICS – DC + AC

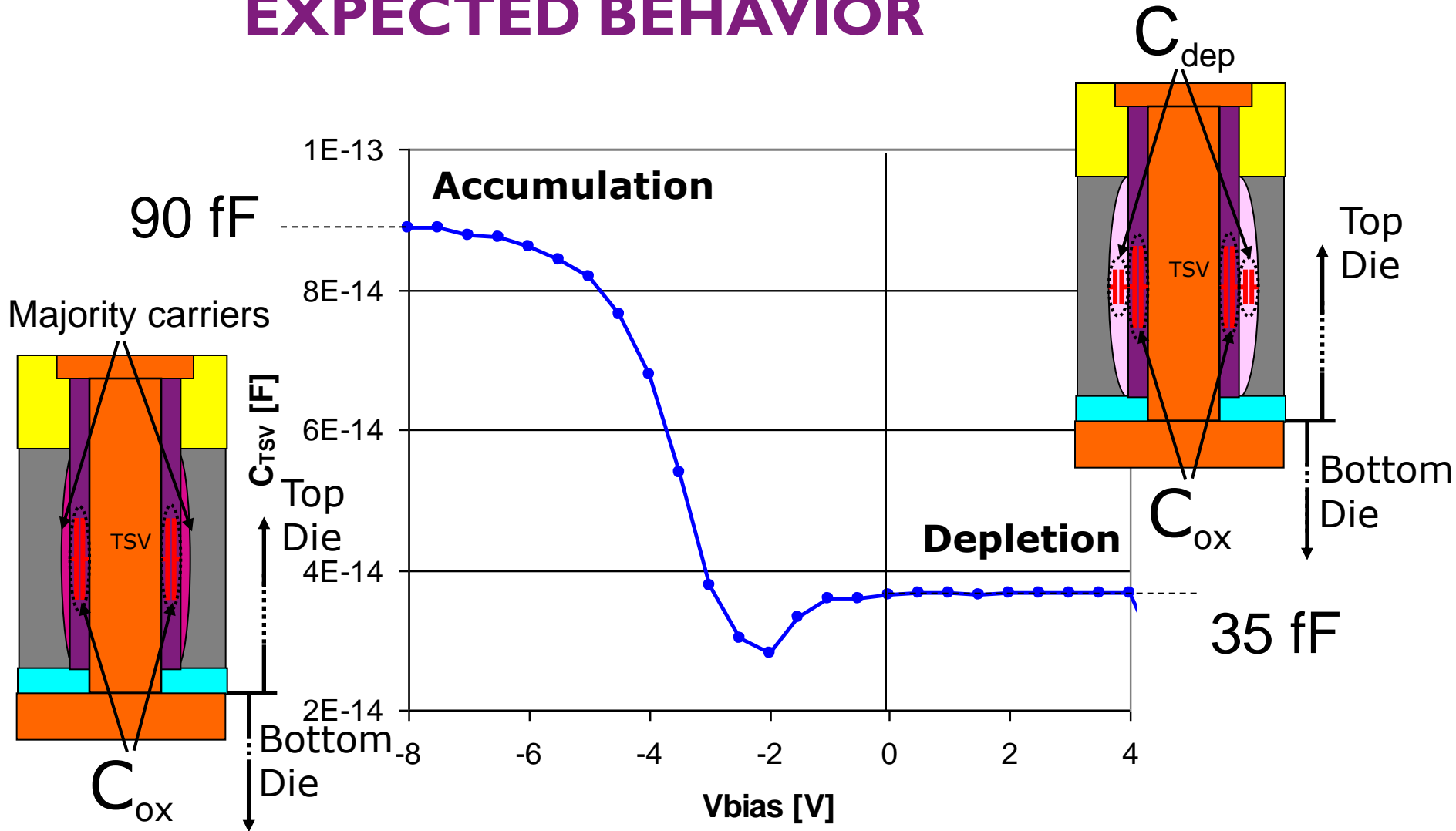


TSV RESISTANCE – LOW RESISTIVE 3D INTERCONNECTS POSSIBLE

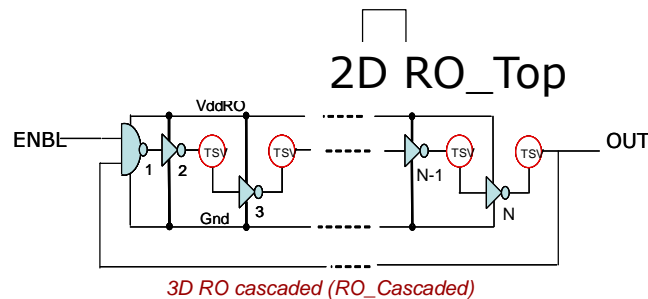
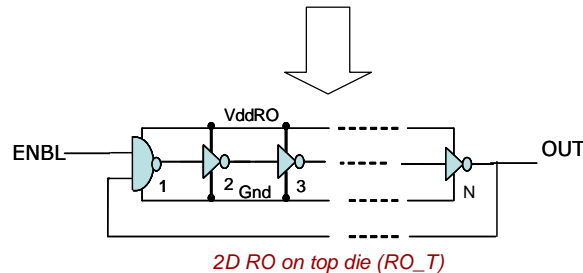
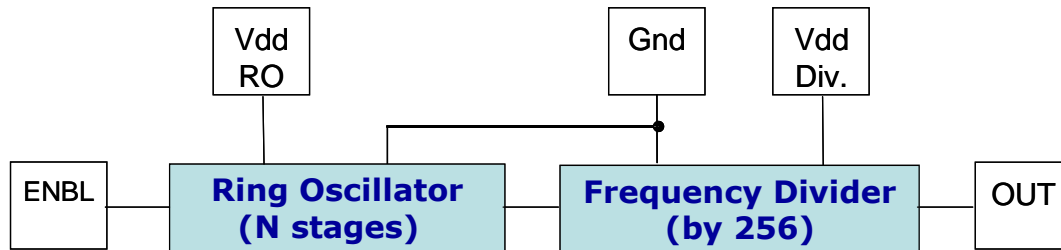
CDF of TSV Resistance



TSV CAPACITANCE - IN LINE WITH EXPECTED BEHAVIOR



3D RING OSCILLATORS: 2D VS 3D



3D RO_Cascaded

Design Details:

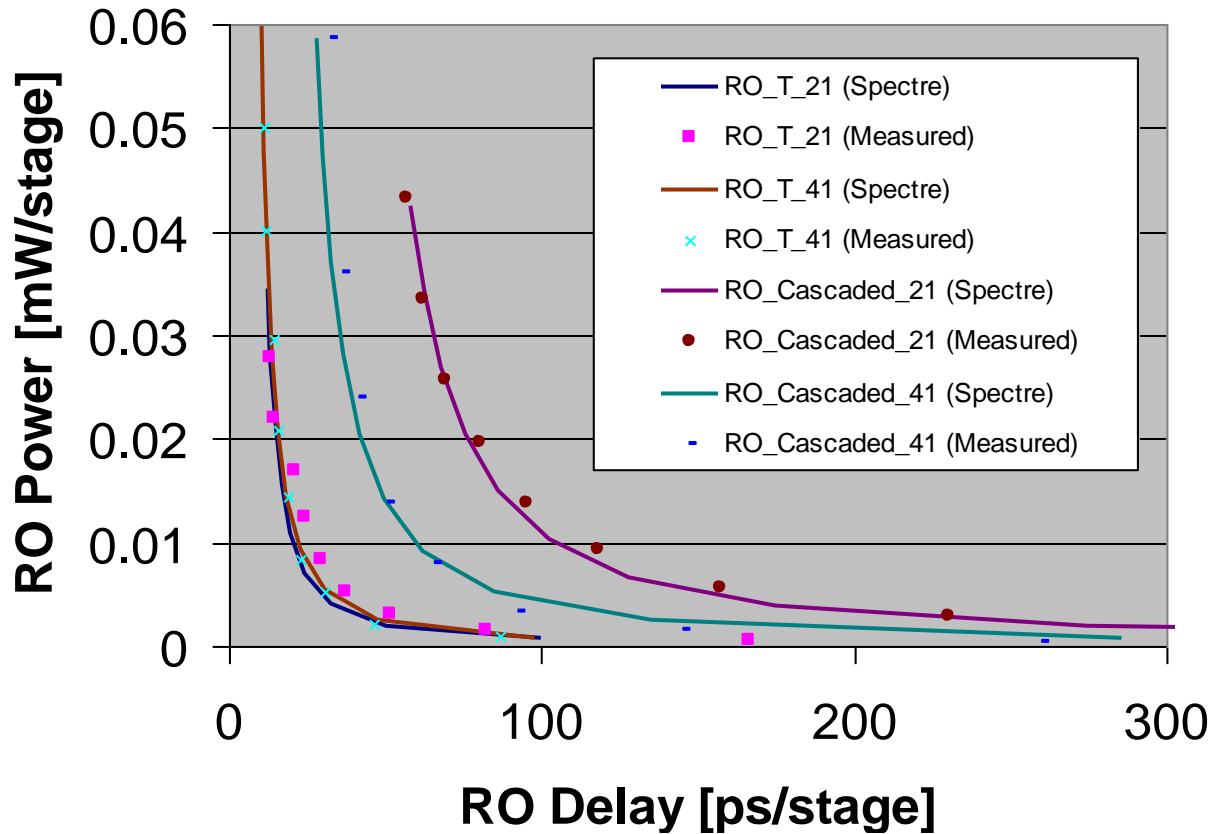
# Inverter Stages (N)	41	21
W_p/L_p	$6\mu\text{m}/0.13\mu\text{m}$	$2\mu\text{m}/0.13\mu\text{m}$
W_n/L_n	$2\mu\text{m}/0.13\mu\text{m}$	$1\mu\text{m}/0.13\mu\text{m}$
R_{TSV}	20 m Ω	
C_{TSV}	37 fF	

Purpose:

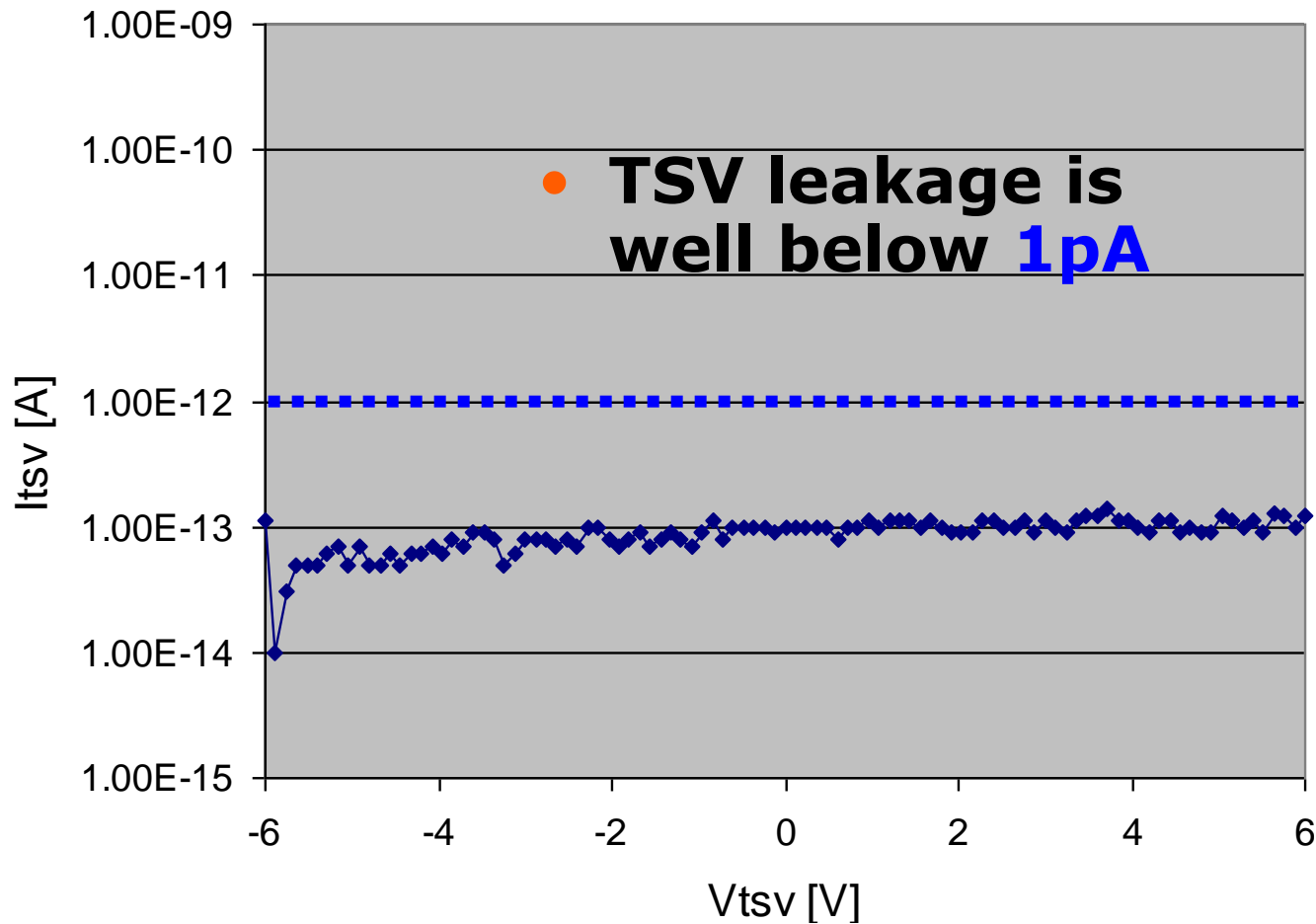
- 3D RO functionality check
- Verification of measured R_{TSV} and C_{TSV}

POWER-DELAY IN RING OSCILLATORS

2D/3D RO Power-Delay Characteristics



TSV LEAKAGE CURRENT TO SUBSTRATE



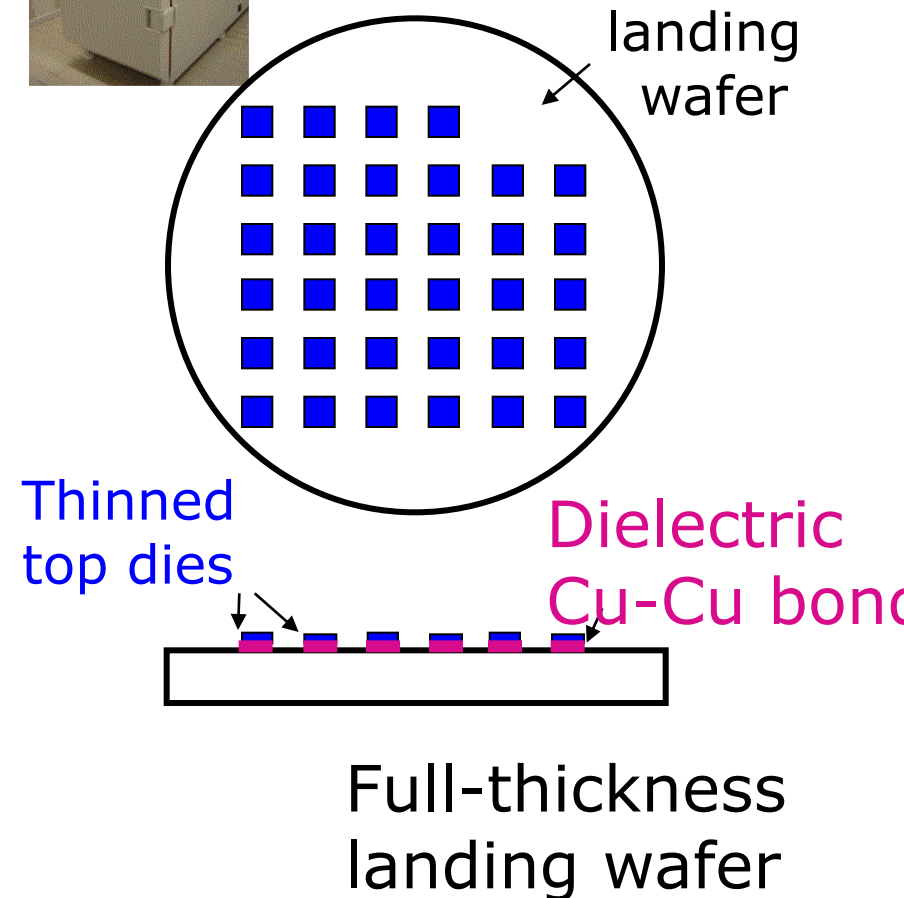
TSV RELIABILITY: STACKED-WAFER THERMAL CYCLING

Thermal cycling of Full wafer with electrical measurements

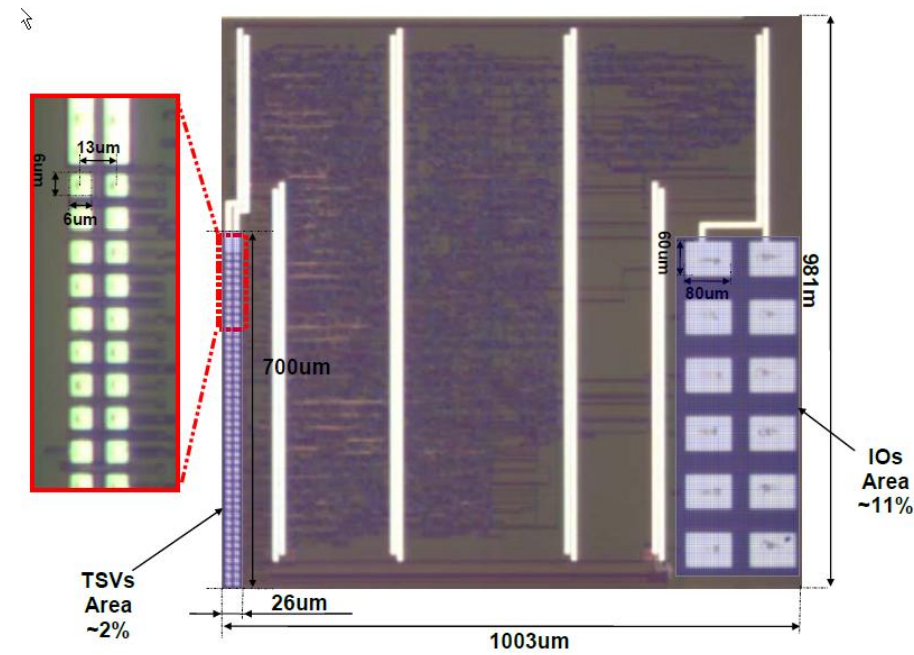
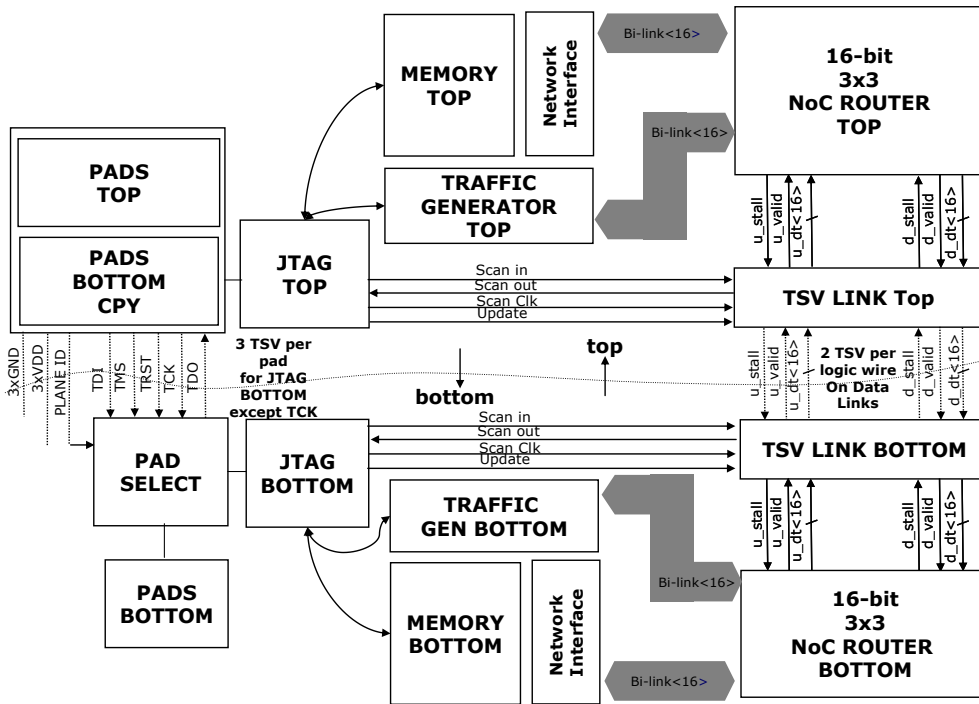
What:

- ▶ Thermal cycling is applied with cycle-time 30min, $T_L = -55^\circ\text{C}$ and $T_H = 125^\circ\text{C}$ (two chamber oven)
- ▶ Electrical measurement at $t=0$ cycles, 10c, 150c, 450c, 1000c
- ▶ Test structures detecting *delamination, leakage and connectivity* of TSV

Results: no reliability problems detected



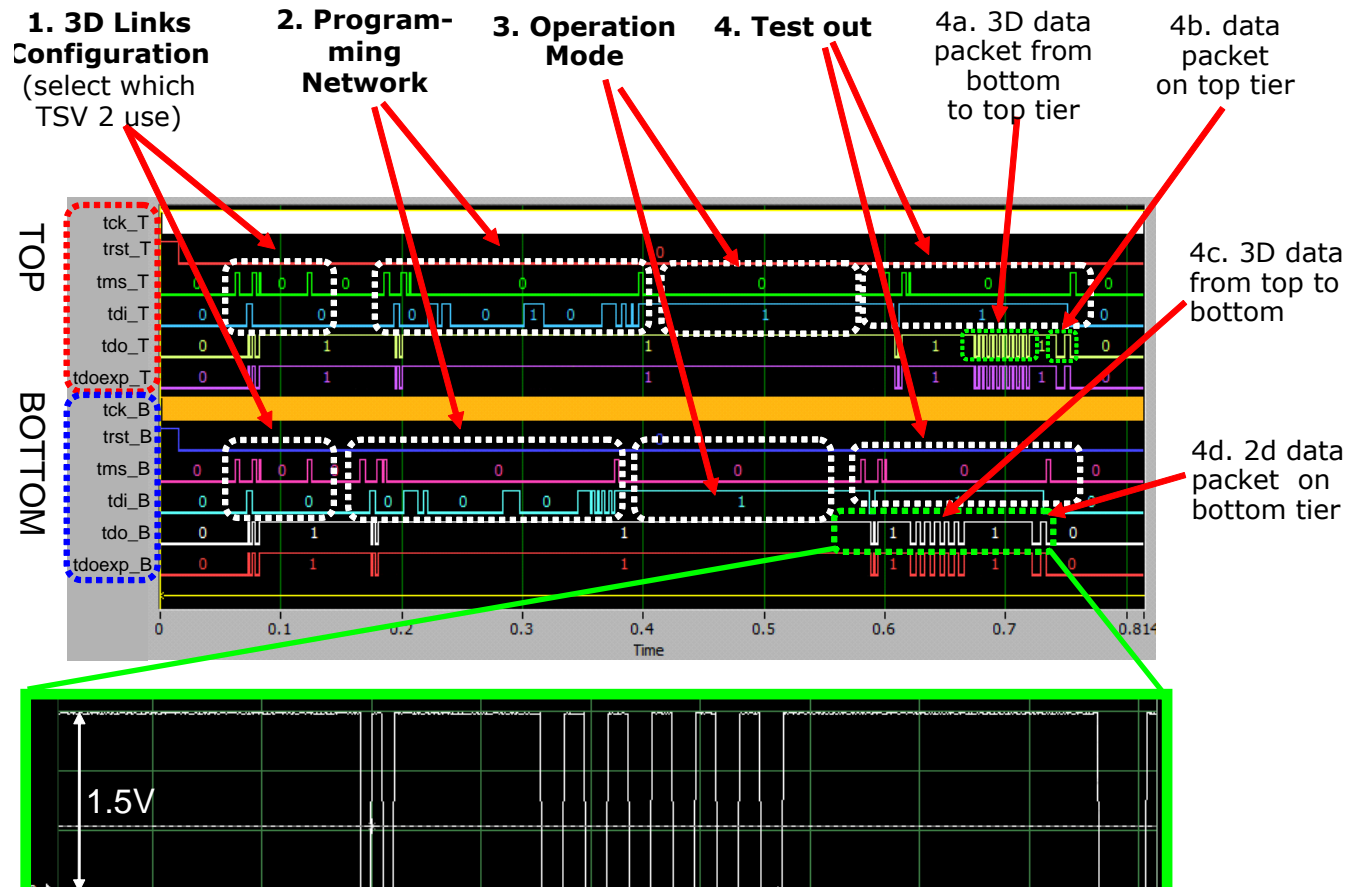
A 3D NOC – DEMONSTRATING CIRCUIT-LEVEL FEASIBILITY OF 3D TSV TECHNOLOGY



Two tiers using 100 TSVs 5 μ m diameter and 13 μ m pitch

*I. Loi et al., "A Low-overhead Fault Tolerance Scheme for TSV-based 3D Network on Chip Links", ICCAD 08, pp. 598-602

SILICON – OUTPUT OF LOGIC ANALYZER



Functional at 25Mhz@0.6-1.5V in 130nm/2M
 Measurement limited by inline test equipment

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3D - ELECTRO-THERMO-MECHANICAL SYSTEM

Yield & reliability of micro-bumps & low-k materials in stacked wafers

Thermal – hot spots

Global Mechanical stress

TSV impact neighboring devices

TSV BONDING YIELD – TEST STRUCTURE

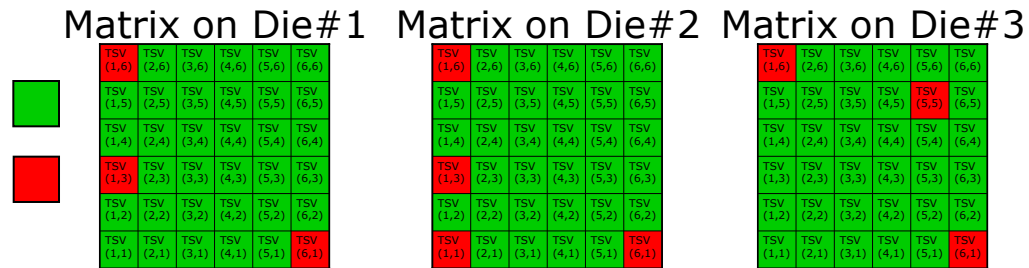
Each TSV is identified by its integer coordinates x and y TSV(x,y)

- ▶ Example: 6x6 TSV matrix
- ▶ 6x6 values of resistance $R_{meas}(x,y)$

TSV (1,6)	TSV (2,6)	TSV (3,6)	TSV (4,6)	TSV (5,6)	TSV (6,6)
TSV (1,5)	TSV (2,5)	TSV (3,5)	TSV (4,5)	TSV (5,5)	TSV (6,5)
TSV (1,4)	TSV (2,4)	TSV (3,4)	TSV (4,4)	TSV (5,4)	TSV (6,4)
TSV (1,3)	TSV (2,3)	TSV (3,3)	TSV (4,3)	TSV (5,3)	TSV (6,3)
TSV (1,2)	TSV (2,2)	TSV (3,2)	TSV (4,2)	TSV (5,2)	TSV (6,2)
TSV (1,1)	TSV (2,1)	TSV (3,1)	TSV (4,1)	TSV (5,1)	TSV (6,1)

- $R_{meas}(x,y)$ is measured on each stacked die

- If $R_{meas} \leq 150\Omega$, the TSV is good \rightarrow
- If $R_{meas} > 150\Omega$, the TSV is bad \rightarrow
- Example: 3 stacked dies



- The yield of each TSV(x,y) in N samples of stacked dies is

$$Y(x,y) = N_{\text{good_TSV}(x,y)} / N$$

- Example: Matrix yield of 3 stacked dies

0	1	1	1	1	1
1	1	1	1	0.66	1
1	1	1	1	1	1
0.33	1	1	1	1	1
1	1	1	1	1	1
0.66	1	1	1	1	0

Matrix yield

TSV BONDING YIELD – FEASIBLE

Yield		TSV pitch=15um			
0.35	0.53	0.53	0.71	0.53	0.35
0.65	0.88	1.00	1.00	0.88	0.65
0.71	1.00	1.00	1.00	1.00	0.76
0.71	1.00	1.00	1.00	1.00	0.82
0.47	1.00	1.00	1.00	1.00	0.53
0.29	0.47	0.65	0.35	0.24	0.24

- @ pitch 15um yield of TSV at edges is poor, center is excellent

Yield		TSV pitch=20um			
0.76	0.88	0.88	0.82	0.94	0.76
0.94	0.88	1.00	1.00	0.88	0.94
0.94	1.00	1.00	1.00	0.94	1.00
0.94	1.00	1.00	1.00	1.00	1.00
0.82	1.00	1.00	1.00	1.00	1.00
0.65	0.65	0.76	0.82	0.82	0.71

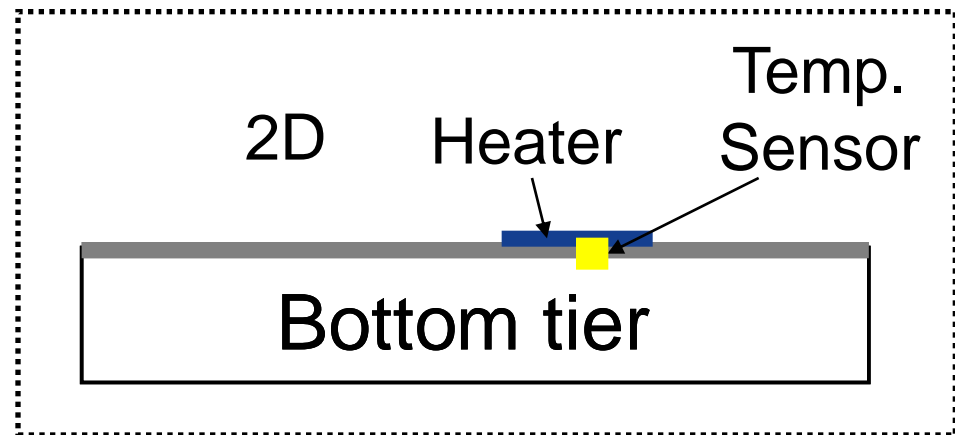
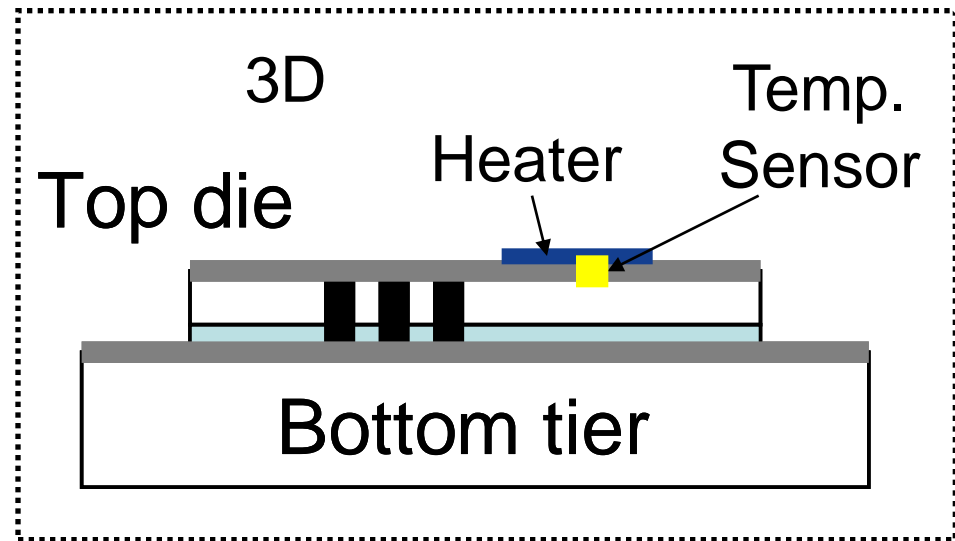
- @ pitch 20um yield of TSV at edges is limited, center is excellent

THERMAL BEHAVIOR OF 3D CHIP-STACK

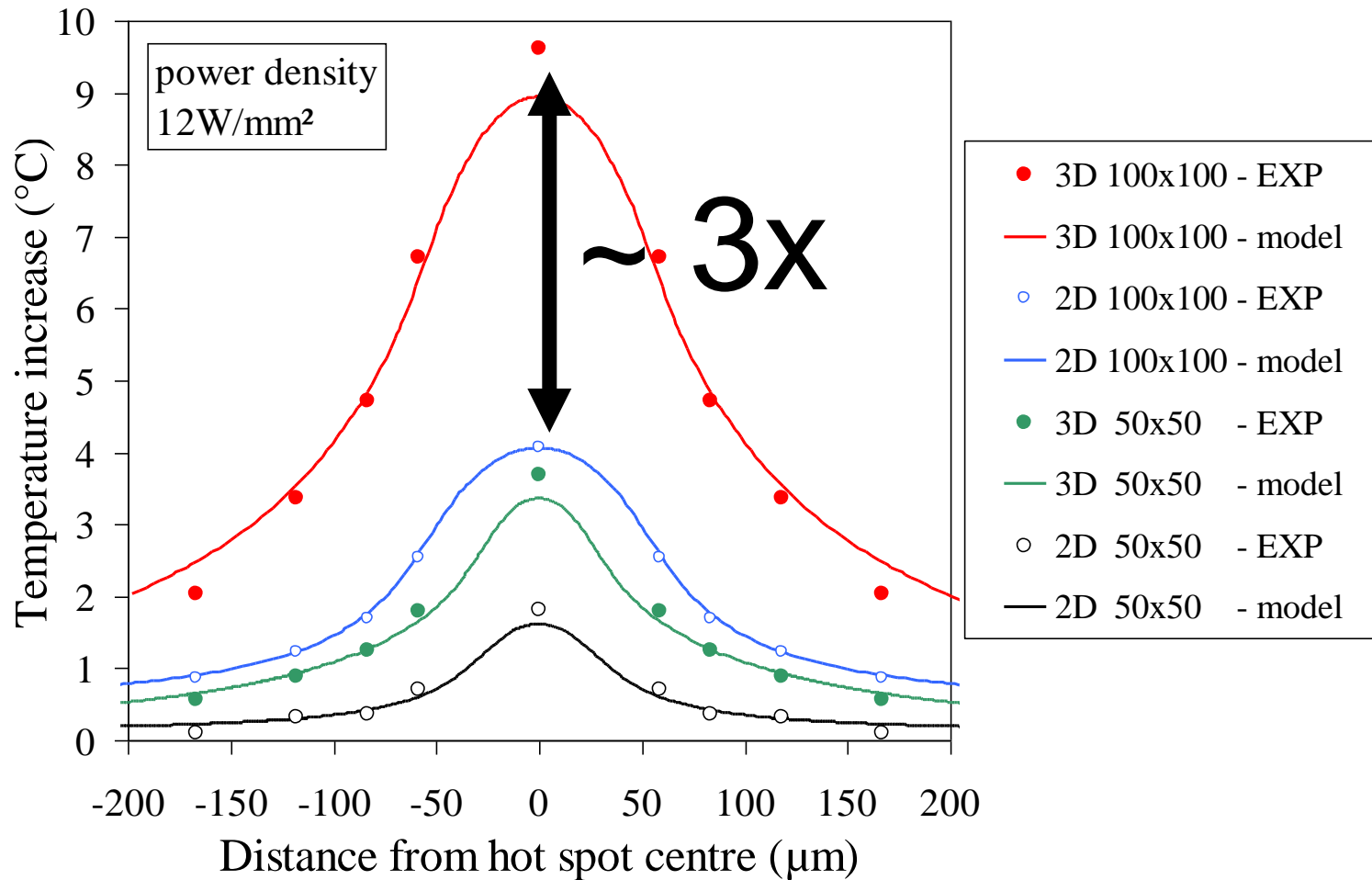
Heaters are included on top die in 3D chip-stack, with temperature sensors

- ▶ two sizes of heaters:
50x50um & 100x100um

Identical heaters are included in 2D die with temperature sensors



3D VS 2D THERMAL HOT SPOTS



MUST ACCOUNT FOR THERMAL HOTSPOTS DURING DESIGN

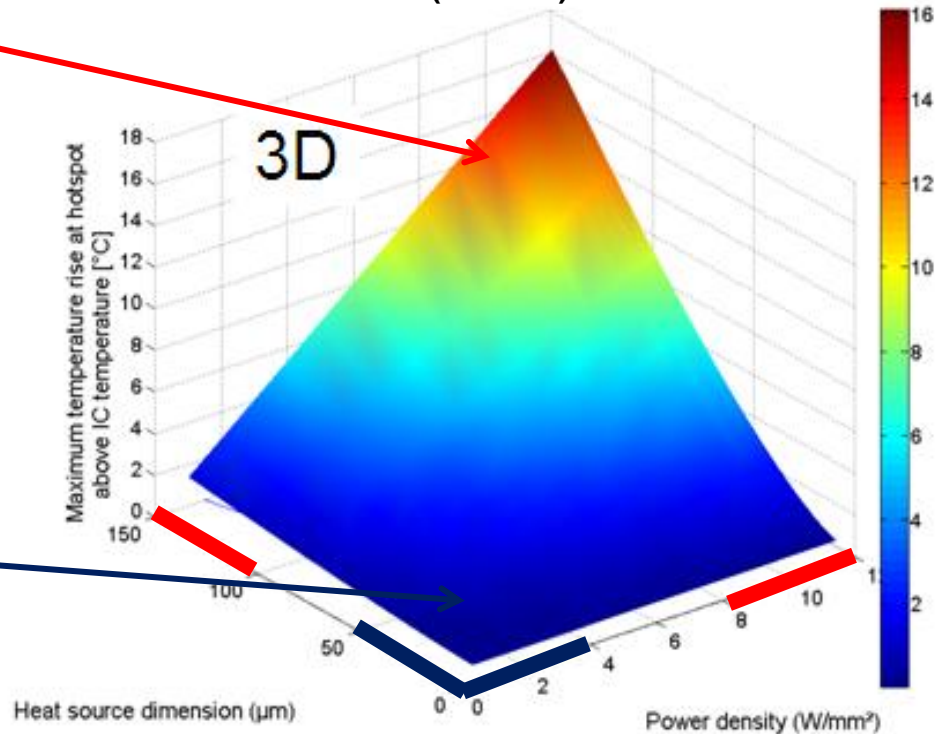
High Performance

high power densities, big heat sources, big thermal issues

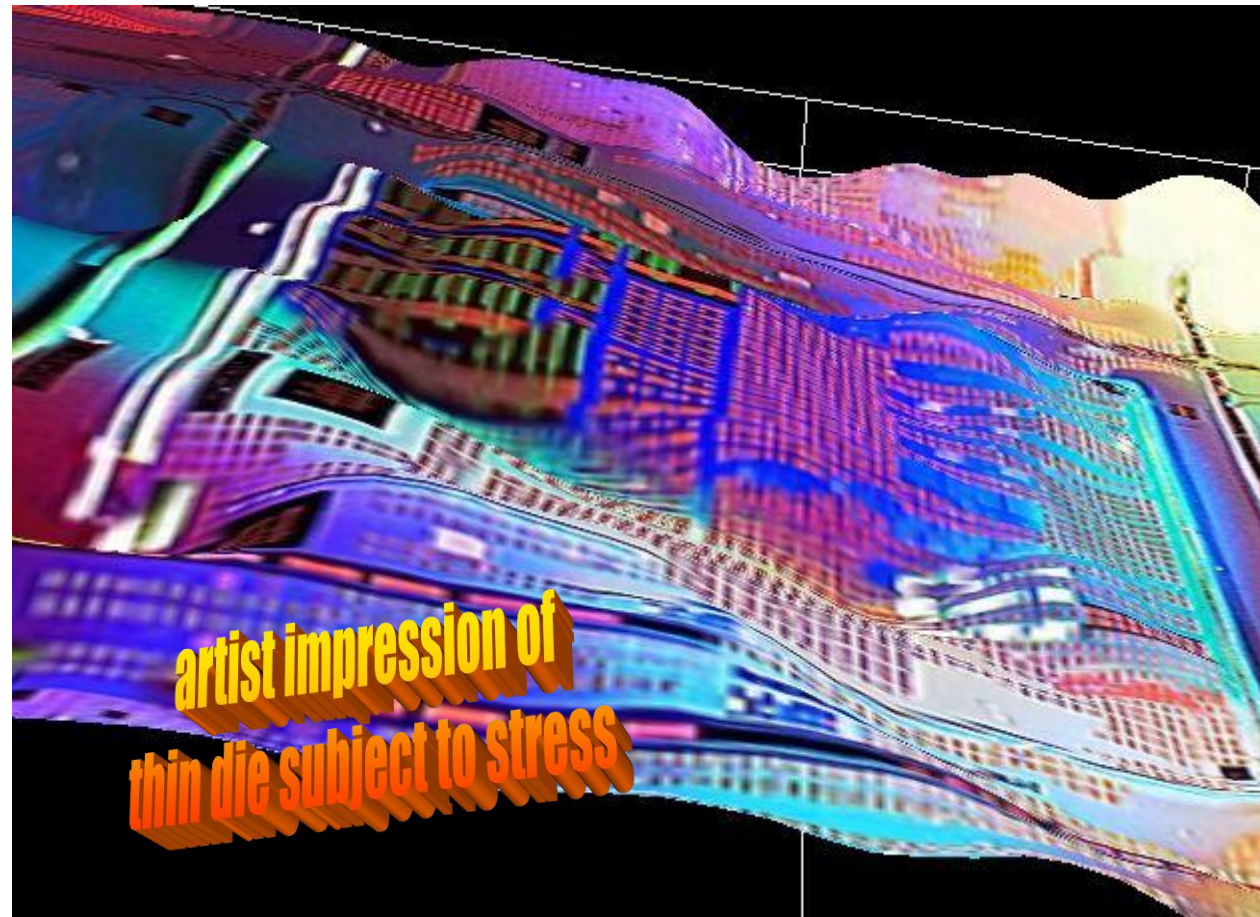
Mobile consumer

small heat sources, low power densities, minor thermal issues

Thermal gradients on thinned top die of a 3D stack (3D130C)



GLOBAL MECHANICAL STRESS IN A 3D STACK



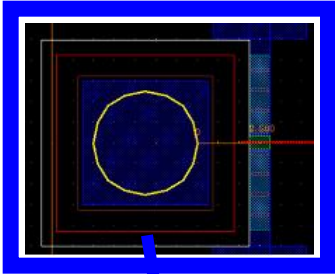
You don't want this to happen when stacking a thin die on top of a thick bottom die

How to avoid it?

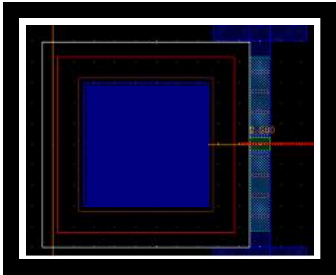
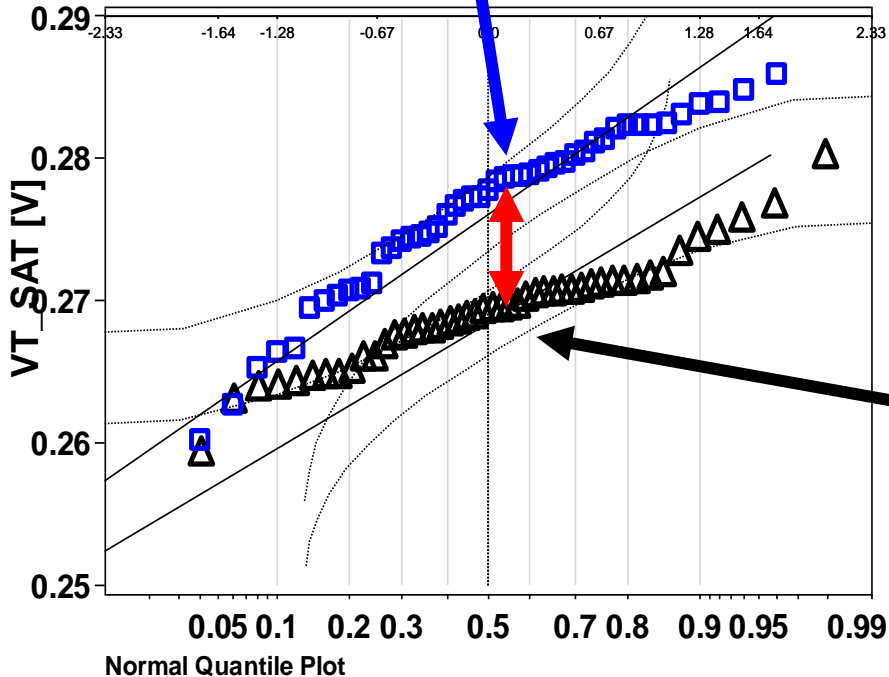
How to design for this?

LOCAL STRESS – TSV PROXIMITY ON 130nm LONG-CHANNEL CMOS DEVICE – 10 mV

nMOSFET
W/L=1 μ m/1 μ m



□ TSV
△ no TSV



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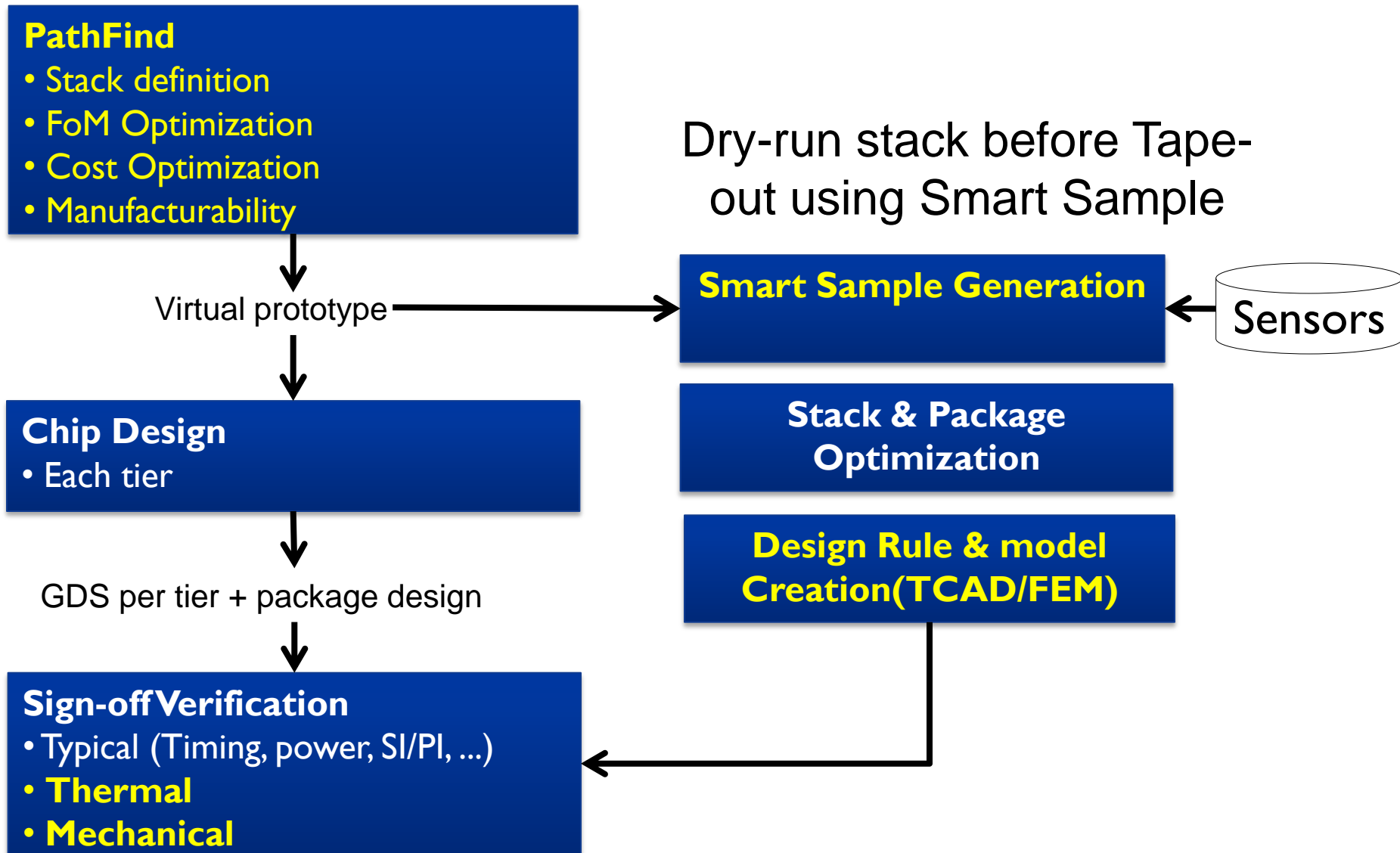
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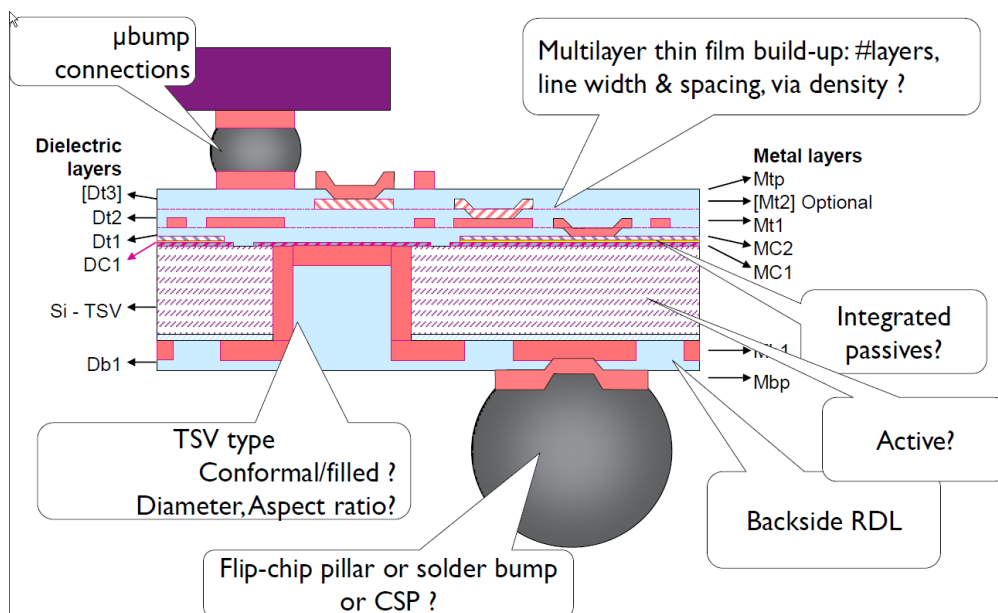
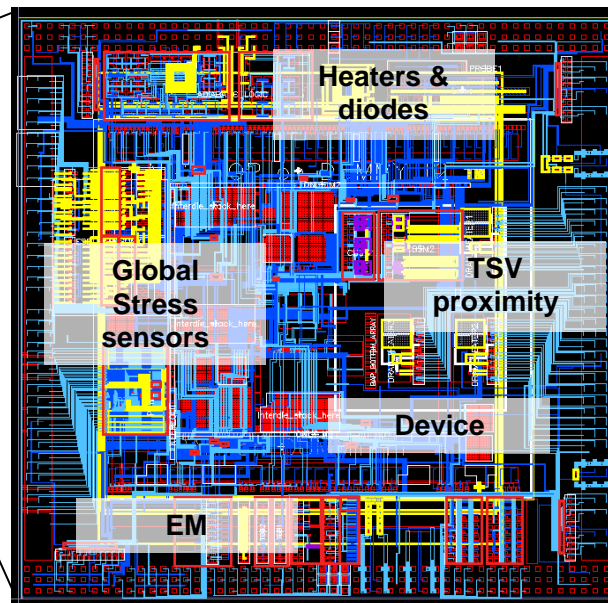
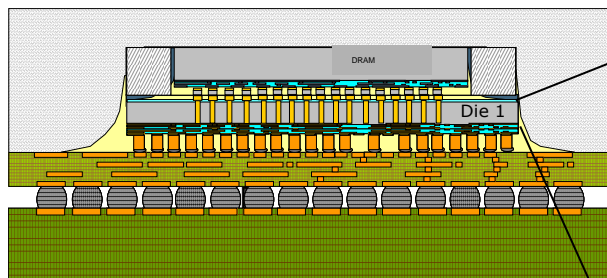
Conclusions

AUGMENTING THE DESIGN FLOW



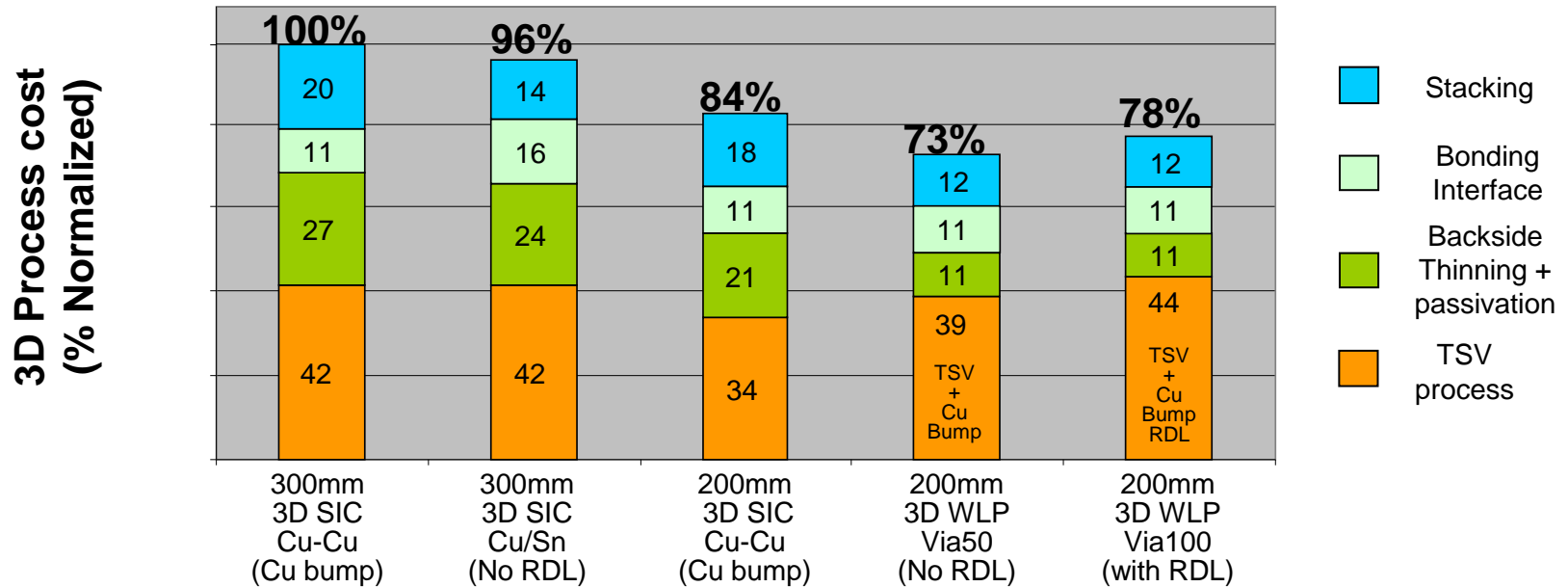
SMART SAMPLE DESIGN – AN EXAMPLE, DRAM ON TOP OF LOGIC DIE

Pathfinding defined
Stack configuration



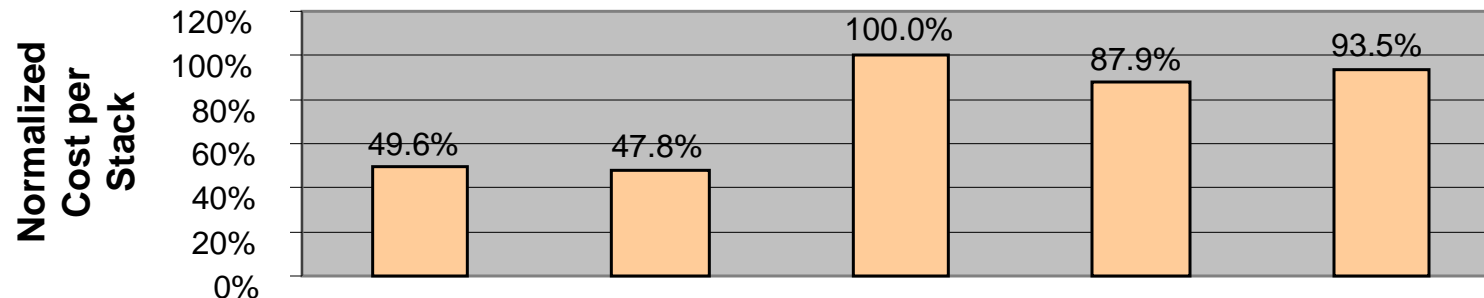
Designed 'smart sample'
(>mechanical sample)

COST OF 3D ON 200mm/300mm WAFERS ASSUMING 100% YIELD

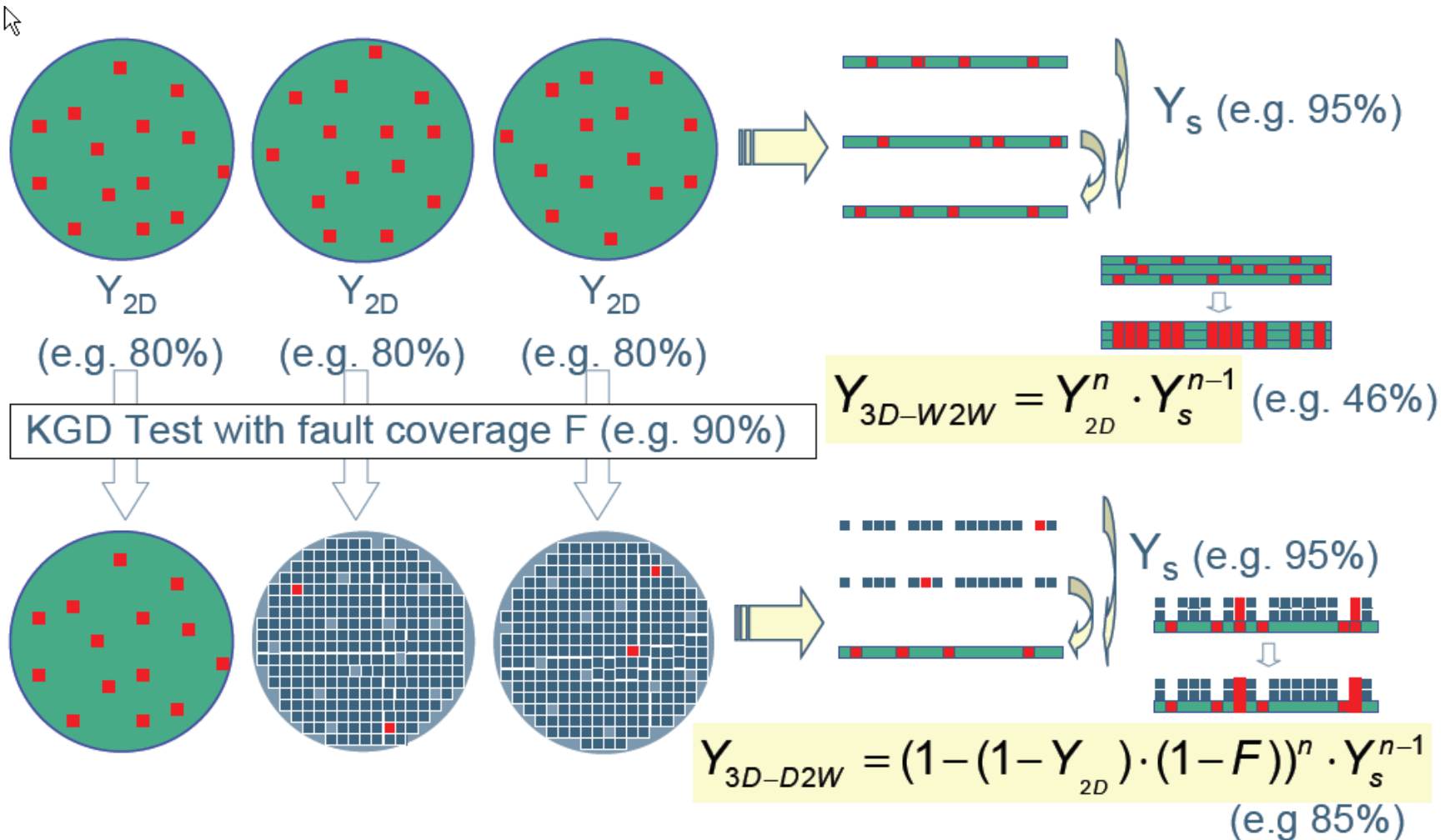


3D stacks per wafer

840 840 348 348 348

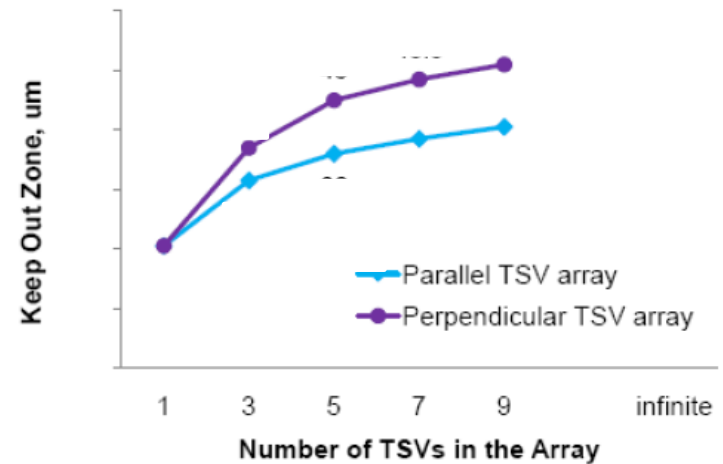
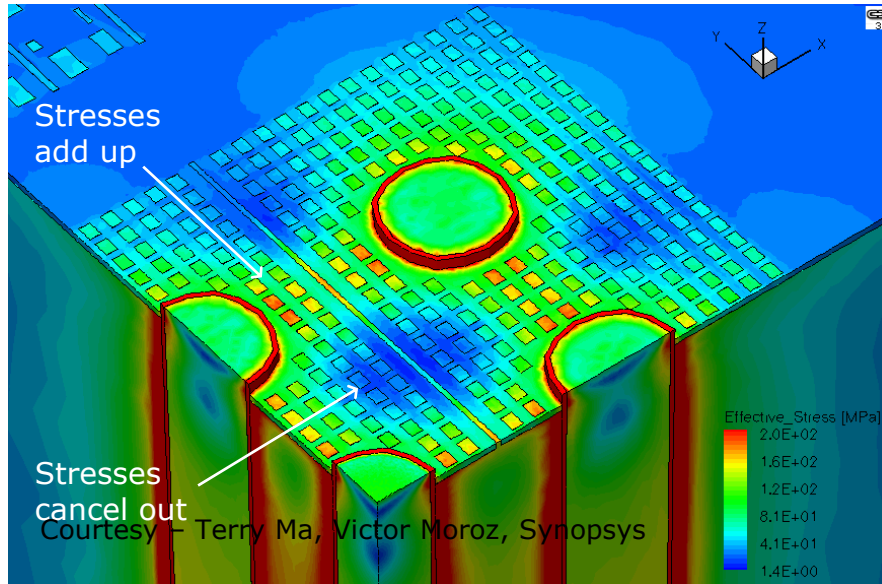


YIELD MODEL MUST BE INCLUDED TO THE OPTION SELECTED



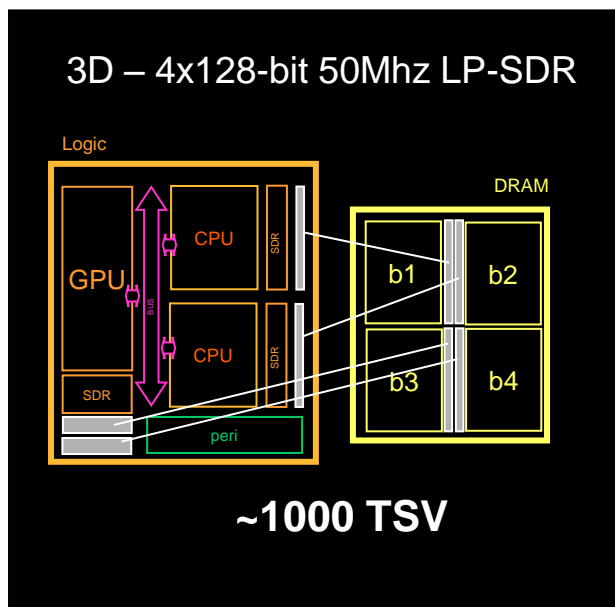
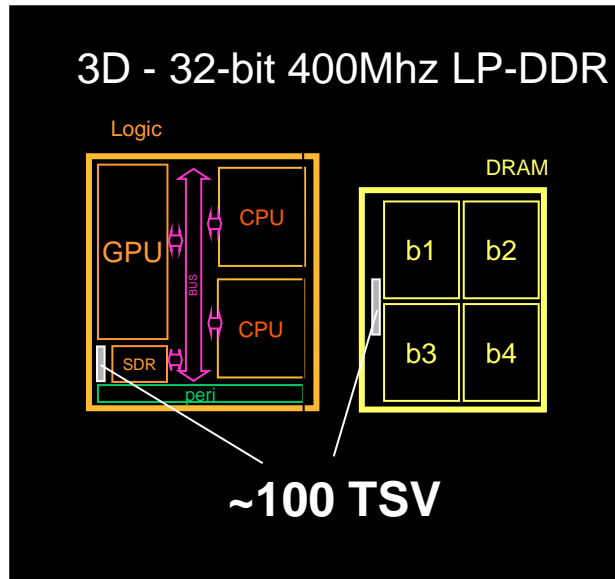
DERIVING DESIGN RULES AND MODELS – TSV & DEVICE PROXIMITY

TSV interactions: von Mises stress pattern



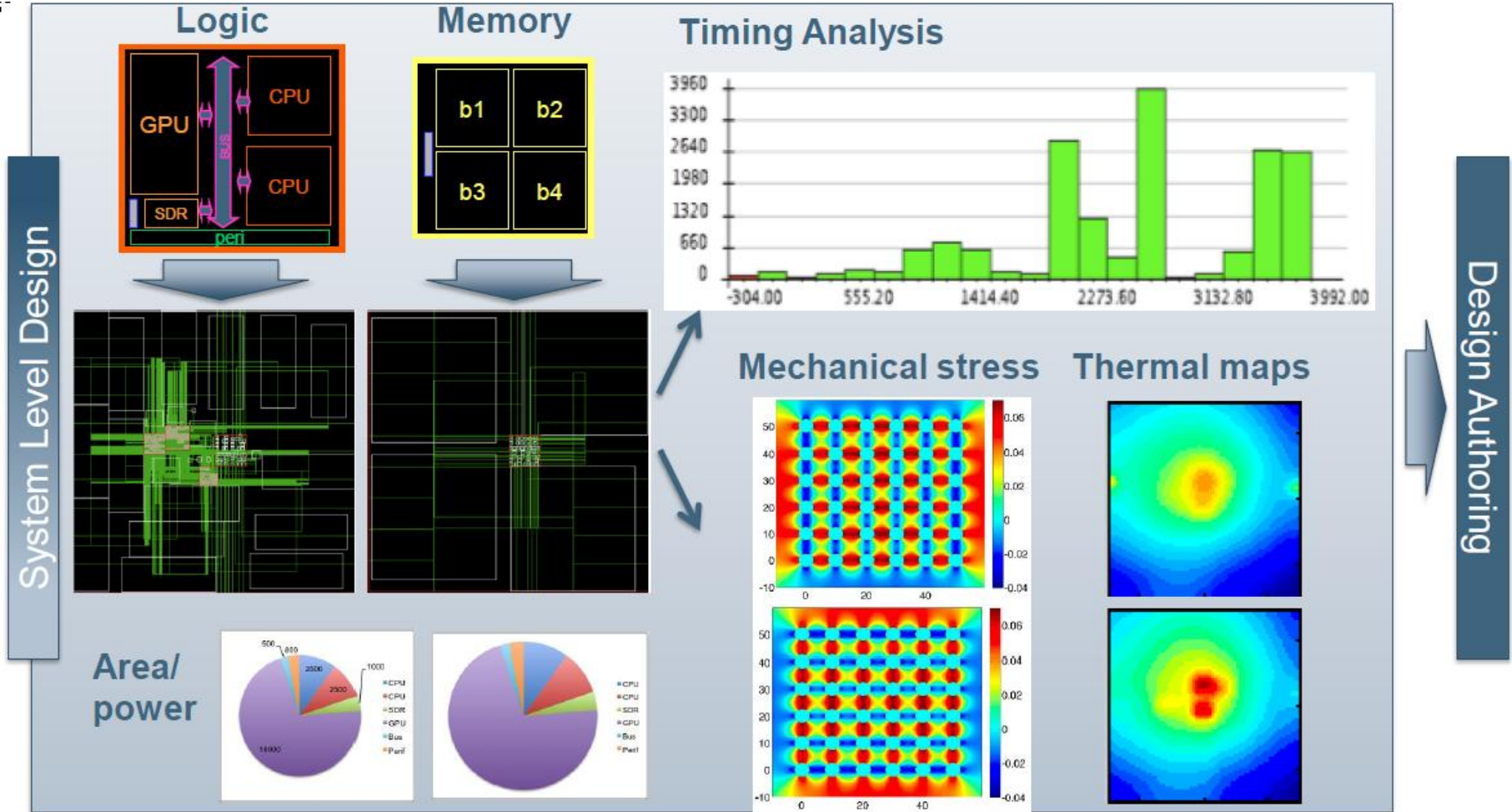
Calibrated TCAD simulations with Test silicon
Derived Design rules

PACKAGE-CHIP CO-DESIGN: PATHFINDING

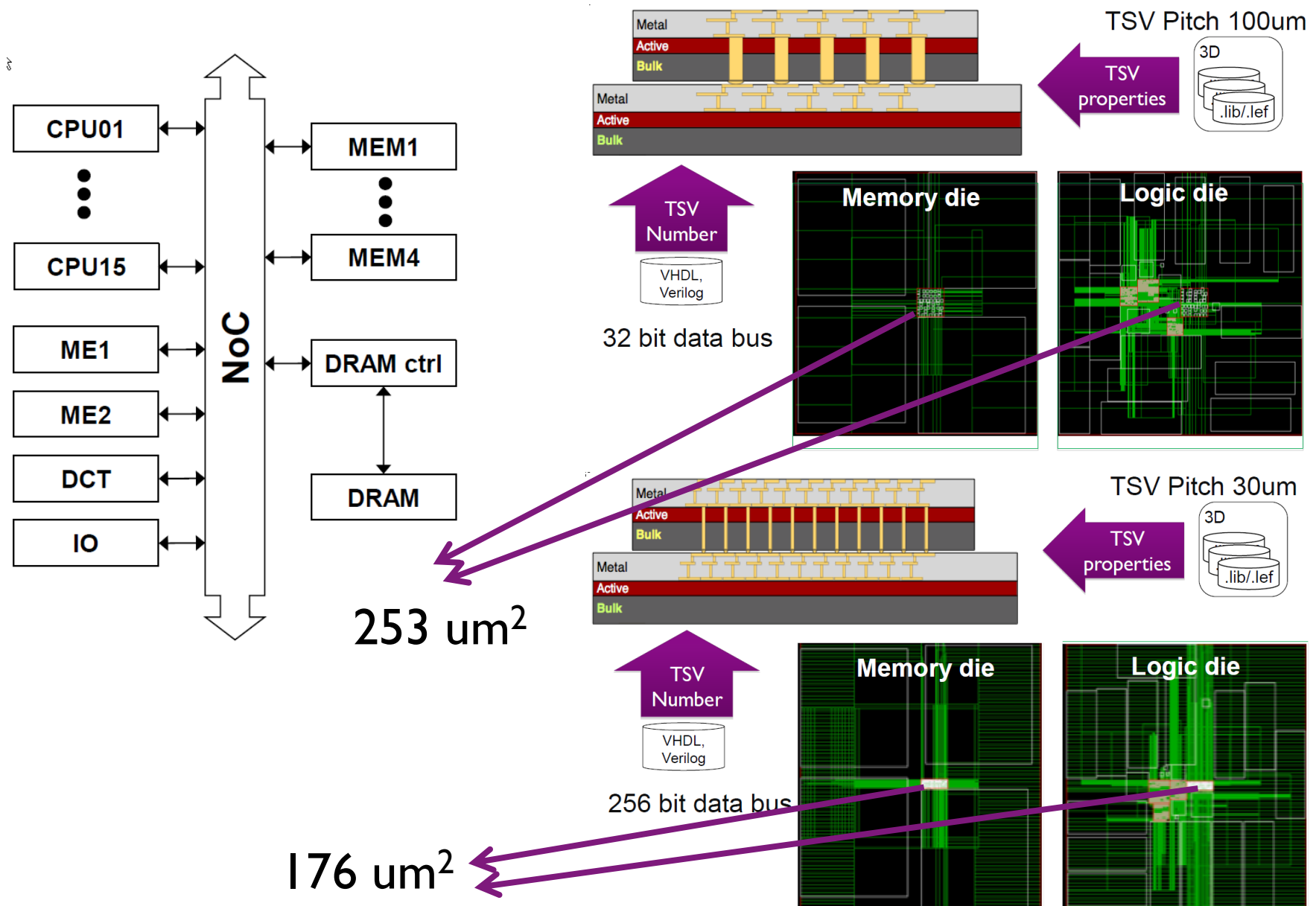


- What is the optimal architecture?
- TSV placement?
- RDL required?
- Performance (delay, latency)?
- Power?
- Thermal management?
- Mechanical behavior?
- Cost? (Test+Thinning+Stacking+Yield)

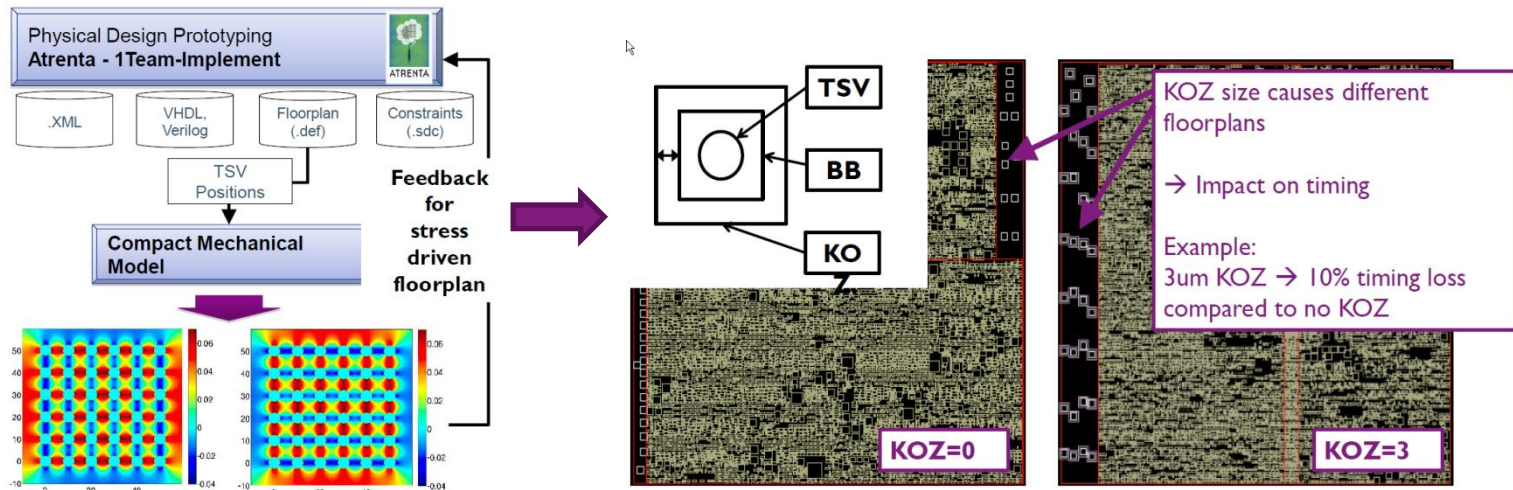
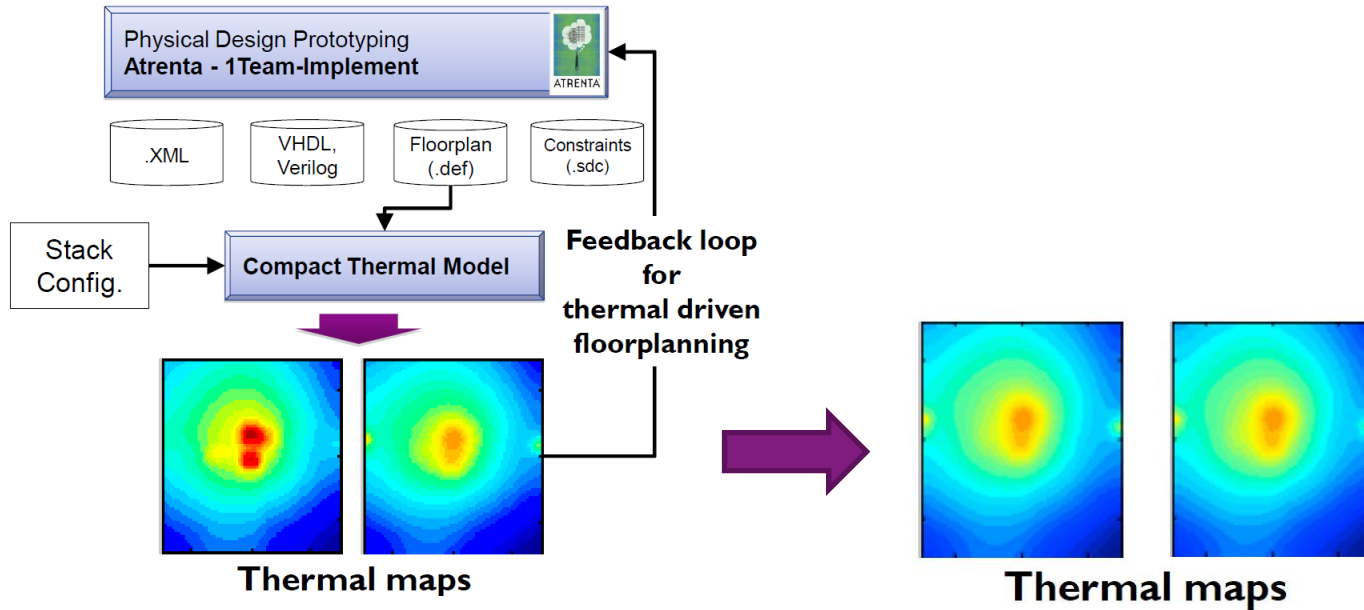
SOLUTION: PATHFINDING FLOW & TOOLS



TSV PITCH - AREA IMPACT



THERMO-MECHANICAL-AWARE LAYOUT



CONCLUSIONS

3D Integration is becoming reality

- ▶ Products in volume for 3D WLP
- ▶ Demo circuits available for 3D SIC
- ▶ Experimental data for enabling 3D SIC Platforms

PathFinding to uncover the ample system opportunities of 3D Technology

- ▶ Definition of stack design thru co-optimization of design/technology
- ▶ Cost/performance/power evaluation

Must re-visit design flow to incorporate new design rules and models for thermo-mechanical modeling

- ▶ Calibration of simulation & models required
- ▶ Standardization of technology data