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DVFS in Presence of Process Variations

Diana Marculescu

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ISCA-2010 Tutorial #2

DVFS in Presence of Process Variations

Diana Marculescu
Carnegie Mellon University
dianam@cmu.edu



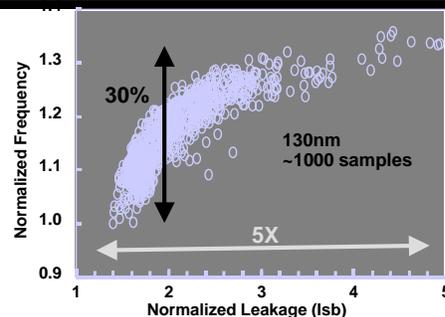
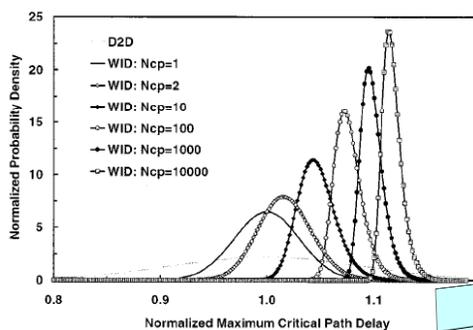
Energy Aware Computing Research Group



Performance – Energy – Variability interactions

- System performance and leakage power severely affected by variability

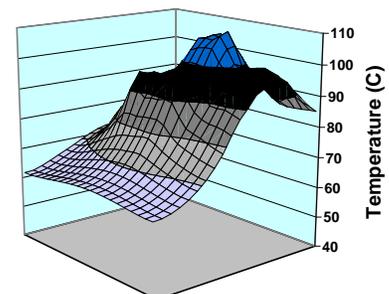
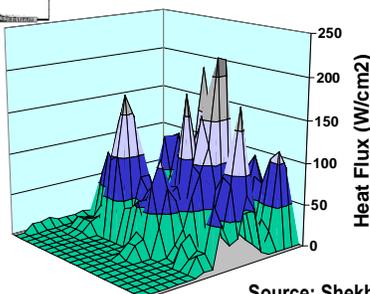
Source: Shekhar Borkar, Intel, DAC 2004

Frequency
~30%Leakage Power
~5-10X

- A whole generation of performance could be lost due to variability

Source: Bowman et. al., JSSC 2002

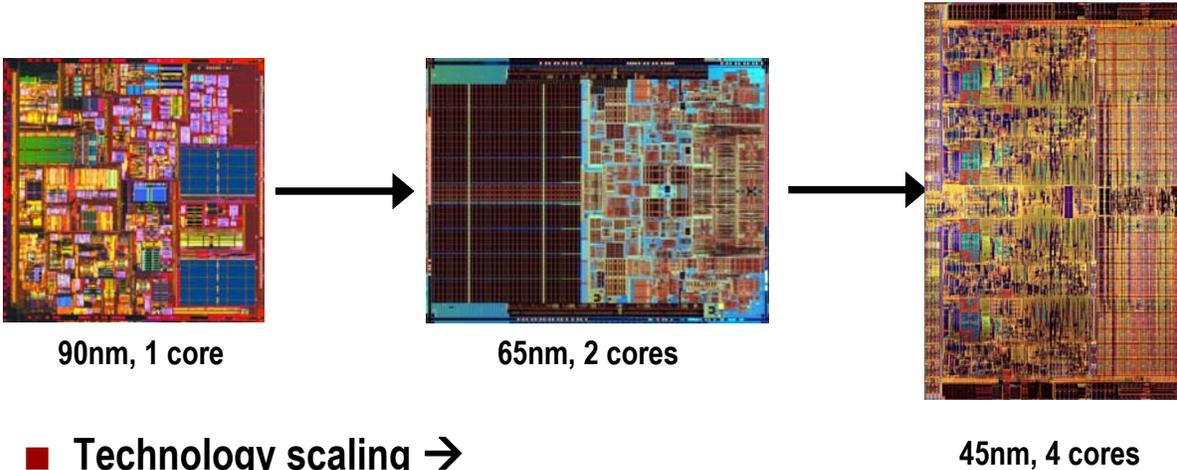
- Increased power density creates hotspots → negatively impacts variability further



Source: Shekhar Borkar, Intel, DAC 2004

Multi-Core, Variations, and Power Management

- Chip-multiprocessor is here → New use of Moore's Law: 2x number of cores every technology generation



- Technology scaling →
 - + Smaller cores (more cores per die)
 - Increased process variability
- Designs moving toward local clock/voltage control → power management per core/DVFS per voltage-frequency island (VFI)

Design Variability and Power Management

- Existing power management techniques
 - ▼ Oblivious to manufacturing process induced uncertainty...
 - ▼ ... while relying exclusively on workload-induced variations, without considering design variations
- To be able to cope with increased design variability, power management mechanisms need to:
 - ▼ Incorporate reliable models for design variability early in the process
 - ▼ Be able to work with variability models for *system components* to determine system behavior
 - ▼ Allow for *seamless adaptation* to hardware characteristics, while relying on existing dynamic power management

Outline

✓ Motivation

■ Variability and Power Management

- ▼ Variation-aware DVFS
- ▼ Body-Biasing and interaction with DVFS
- ▼ Limits for dynamic power management

■ Summary

Core-to-Core Variations

■ Variations in physical/electrical parameters

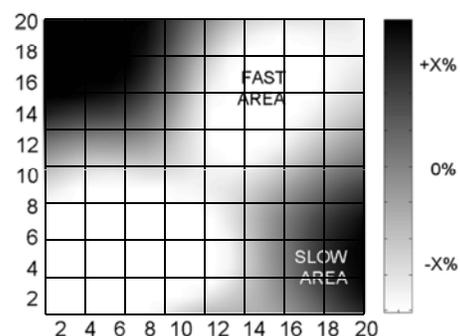
- ▼ Channel length, threshold voltage, oxide thickness
- ▼ Can be lot-to-lot, wafer-to-wafer, die-to-die, *within-die*
- ▼ Can be random and uncorrelated, *random and correlated, systematic*

■ Traditionally, die-to-die component dominated

- ▼ Handled with margins, speed-binning

■ Core sizes decreasing and core counts increasing

- ▼ Intra-die process variations manifest as core-to-core frequency variations



Source: Abulafia et al., TVLSI'06

Dynamic Voltage/Frequency Scaling

- **Dynamic voltage/frequency scaling**
 - ▼ Reduces both dynamic and static power
 - ▼ Control algorithm attempts to lower performance cost

- **Current algorithms are unaware of variations**
 - ▼ [Juang et al. ISLPED'05], [Ischi et al. MICRO'06], [Herbert and Marculescu ISLPED'07]
 - ▼ Treat all cores as being identical
 - ▼ Result in wasted power
 - ▼ Single software-based exception [Teodorescu ISCA'08]

- **Variability-aware DVFS attempts to improve energy-efficiency**
 - ▼ Reduce power while maintaining performance [Herbert and Marculescu HPCA'09]

Possible Solutions

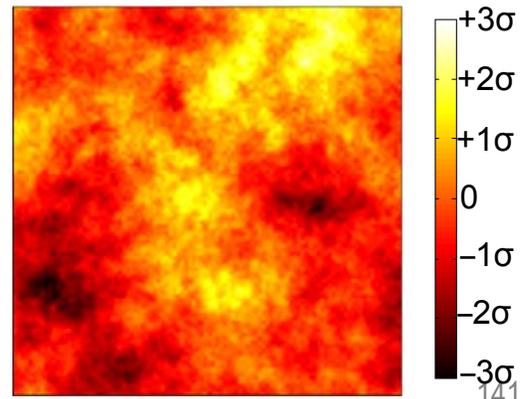
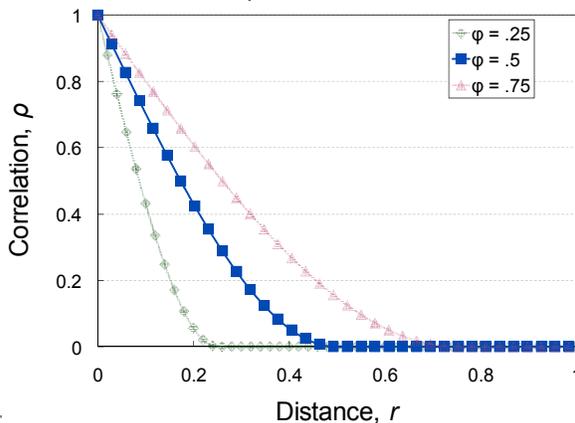
- **Develop dynamic control algorithms from scratch**
 - ▼ Characterize each die separately post-manufacturing
 - ▼ Include those characteristics in newly developed algorithms
 - + Attacks the problem with a specific solution
 - May make a wealth of already existing algorithms potentially unusable
 - Requires pre-characterization at test/post-manufacturing

- **Adapt existing dynamic control algorithms to including variations**
 - ▼ Modify existing algorithms to include per core/per VFI models for process variations
 - + Easy to reuse existing control algorithms
 - Some pre-characterization at test/post-manufacturing required

Physical Parameter Modeling

- Model of spatially-correlated intra-die V_{th} and L_{eff} variation
- Multivariate normal with spherical correlation function [Sarangi TSM'08]

$$\rho(r) = \begin{cases} 1 - \frac{3r}{2\phi} + \frac{1}{2} \left(\frac{r}{\phi} \right)^3 & r \leq \phi \\ 0 & r > \phi \end{cases}$$



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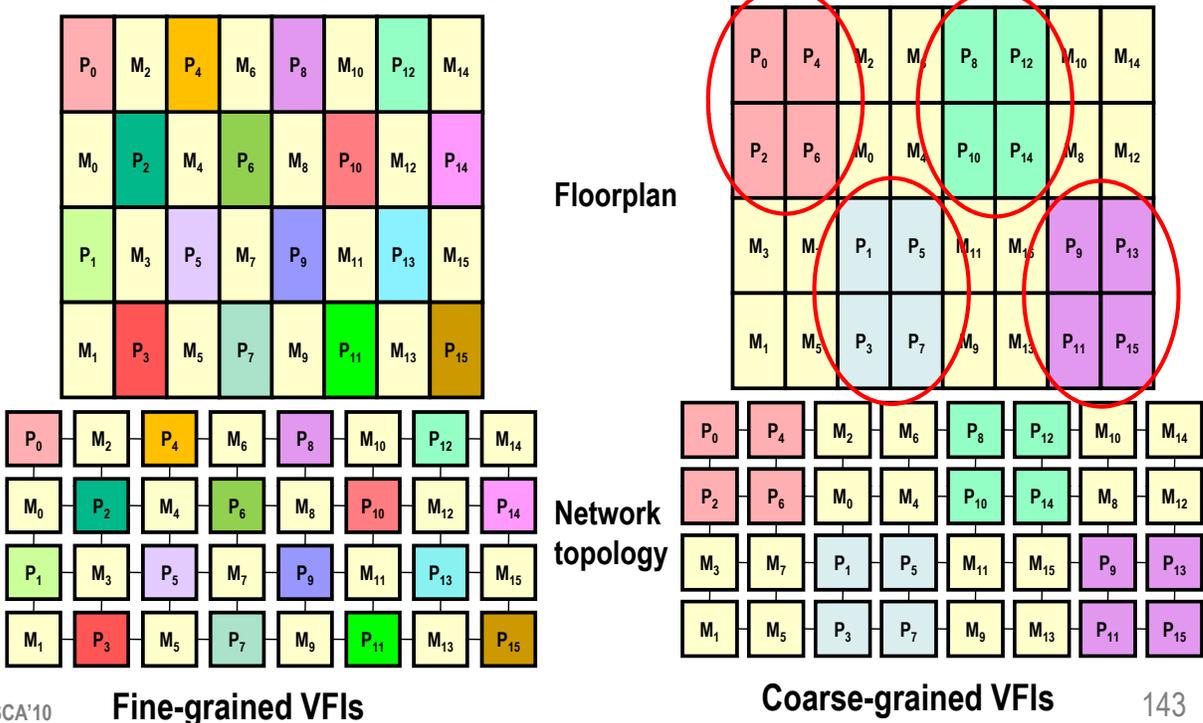
Core Power/Performance Modeling

- Fit response surface models to SPICE data [Herbert and Marculescu HPCA'09, TCOMP'09]
 - ▼ 22nm hi-K metal gate PTM models [Zhao TED'06]
 - ▼ Lump L_{eff} and V_{th} variation into process variation parameter $\rho \rightarrow$ capture correlations
- Models for frequency and leakage
 - ▼ As functions of ρ , V_{dd} and temperature T
 - ▼ Model form is $e^{\text{polynomial}}$
 - ▼ Frequency model tracks 13-stage FO4 ring oscillator
 - ▼ Leakage model tracks I_{sd} of FETs with $|V_{ds}| = V_{dd}$ and $V_{gs} = 0$
- Models fit to minimize maximum absolute percent error
 - ▼ Iterative pruning removes coefficients until error doubles

Core-to-core Variability Characterization

■ Example: Two chip-multiprocessor designs

▼ Different voltage/frequency island granularity



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Fine-grained VFIs

Coarse-grained VFIs

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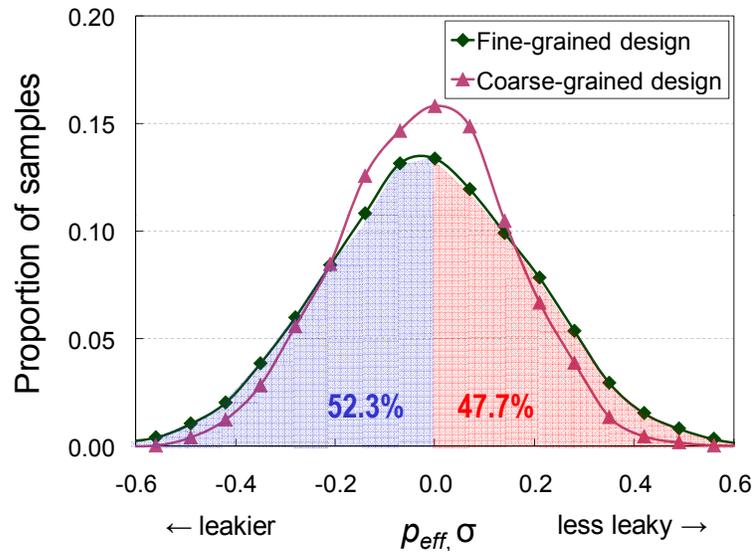
Exposing Variations to DVFS Algorithms

- Variability model has many points per VFI, each with own ρ
 - ▼ Need a simple way of aggregating and exposing this information at microarchitecture level
 - ▼ ρ_{eff} is ρ value that best tracks VFI's leakage across V_{dd} and temperature
- Computed based on four measurements of VFI leakage
 - ▼ High and low temperature and V_{dd}
 - ▼ Can be done based on IDDQ test results
- Negligible error compared to modeling many points per core
 - ▼ Tested across 1,000 dies and 13,456 (V_{dd} , T) pairs
 - ▼ Single-VFI MAPE of 0.011% for single-core VFIs
 - ▼ Single-VFI MAPE of 0.014% for quad-core VFIs

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Exploiting Variability Information



Bias towards lower V/F levels
Greater power reduction
Greater performance reduction

Bias towards higher V/F levels
Smaller power increase
Smaller performance increase

- Use frequency asymmetry to reduce performance loss
 - ▼ Run leakier cores at lower voltages, but at higher than normal frequencies for those voltages

Threshold DVFS Algorithm

- Keeps utilization in a specified range [Herbert and Marculescu ISLPED'07]
 - ▼ Utilization = (instructions retired / number of retire slots)
 - ▼ Higher VF level → lower utilization
 - ▼ Lower utilization target → higher VF level
- *Threshold-unaware* uses range of [0.2, 0.4] for all VFIs
- *Threshold-aware* sets threshold based on each VFI's variations
- Exponential scaling applied
 - ▼ VFI i thresholds set to $[e^{P_{eff,i} \cdot T_{down}}, e^{P_{eff,i} \cdot T_{up}}]$
 - ▼ Target band [0.279, 0.558] for core in 5th percentile of p distribution (most leaky)
 - ▼ Target band [0.139, 0.278] for core in 95th percentile of p distribution (least leaky)

Greedy DVFS Algorithm

- Attempts to minimize power/throughput (energy per instruction)
 - ▼ [Herbert and Marculescu ISLPED'07] based on [Magklis et al. ISLPED'06]
 - ▼ Performs greedy search to find the optimal VF level
 - ▼ Upon overshooting, moves back to optimal and holds for H intervals
- *Greedy-aware* scales energy per instruction (EPI) to bias VFIs
- Exponential scaling applied
 - ▼ VFI i metric for interval n is $SEPI_{n,i} = EPI_{n,i} \cdot (e^{D_{eff,i}})^{-n}$

VF level, L	V_{dd}	<i>SEPI</i> scaling for 5 th percentile (leakier)	<i>SEPI</i> scaling for 95 th percentile (less leaky)
0	0.9 V	1.00	1.00
1	0.8 V	0.70	1.39
2	0.7 V	0.49	1.94
3	0.6 V	0.34	2.71

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Custom Solution: Linear Optimization (*LinOpt*)

- **Linear programming:**
 - Maximize objective function: $f(x_1, \dots, x_n)$, with x_1, \dots, x_n independent
 - Subject to constraints such as: $g(x_1, \dots, x_n) < C$
 - f, g are linear functions
- **Unknowns:** voltages V_1, \dots, V_n for all cores
- **Objective function:** maximize CMP throughput
 - Throughput (MIPS) = Frequency \times IPC = $f(V_1, \dots, V_n)$
- **Constraint:** keep power under P_{target}
 - Power = $g(V)$

- Possible issue: functions f and g are NOT linear; worst-case complexity is exponential [Teodorescu et al. ISCA'08]

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Experimental Setup

- **SimFlex infrastructure [Hardavellas et al. SIGMETRICS'04]**

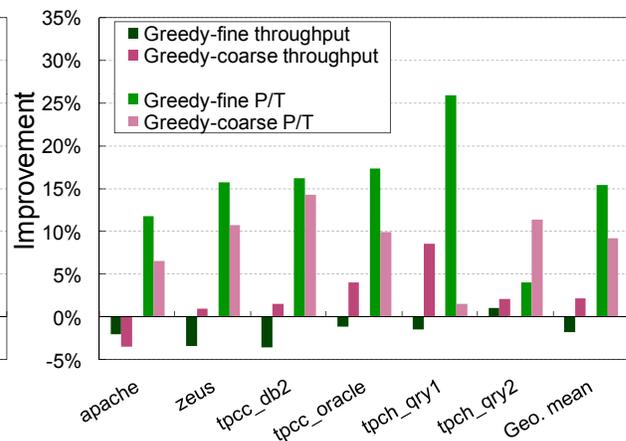
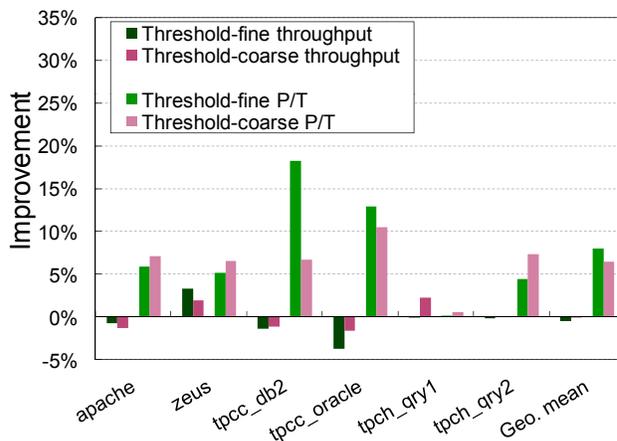
- ▼ Flexus CMPFlex.OoO simulator
- ▼ SMARTS statistical sampling
- ▼ Modified to include power, thermal, variability models, plus a full mesh for on-chip communication

- **Commercial multithreaded workloads**

- ▼ **Web server**
 - SPECweb99 on Apache & Zeus
- ▼ **Online Transaction Processing**
 - TPC-C on Oracle and DB2
- ▼ **Decision Support Systems**
 - TPC-H queries 1 & 2 on DB2

Parameter	Value
Number of cores	16
Nominal frequency	3.0 GHz
Pipeline configuration	8 stages deep 4 instructions wide
ROB/LSQ size	128
Store buffer size	64
L1-I/D cache	Private, 64 KB
L2 cache	Shared, 16 × 1 MB
Main memory	60 ns random access
DVFS interval	50 μs (150K cycles @ 3GHz)

Power-Performance



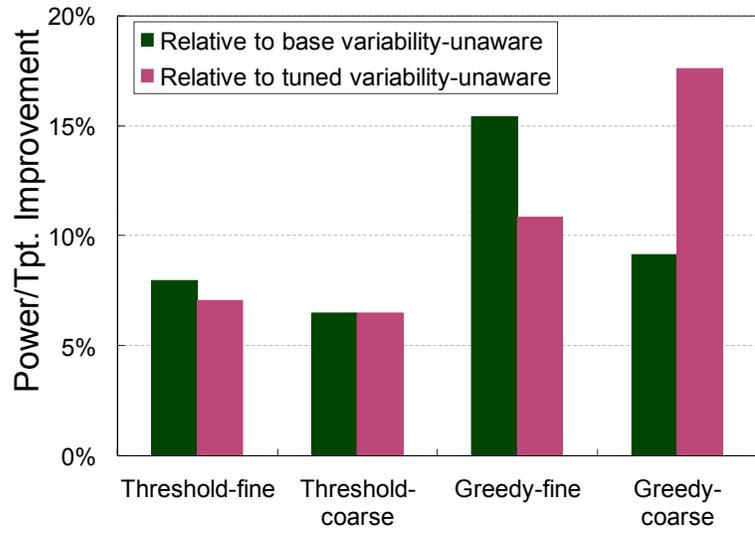
- **Low throughput loss**

- ▼ Worst-case throughput loss under 4%

- **Significant improvement in power/throughput**

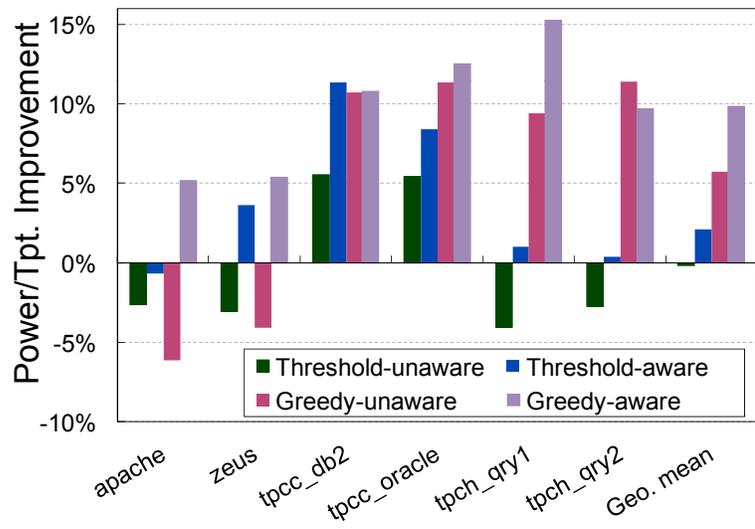
- ▼ 8.0%/6.5% for fine-/coarse-grained VFIs on *Threshold*
- ▼ 15.4%/9.2% for fine-/coarse-grained VFIs on *Greedy*

Comparison at Iso-throughput



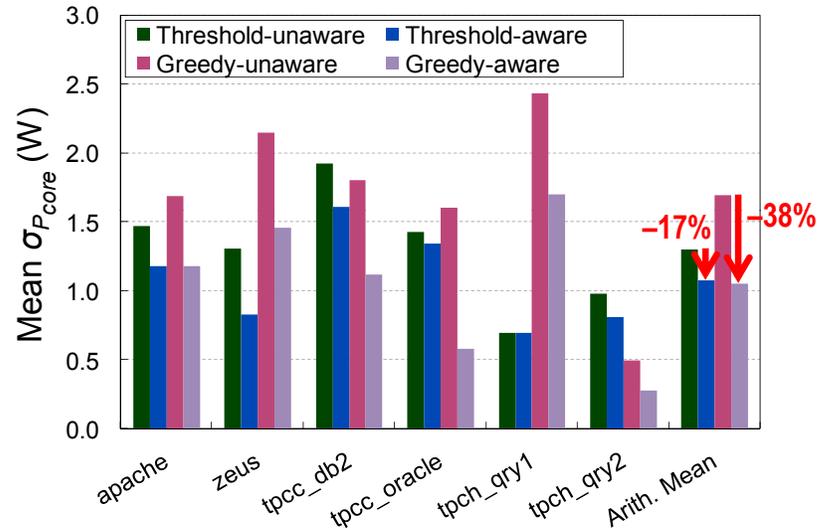
- Tweaked p_{eff} values to achieve iso-throughput between variability-aware scheme and tuned variability-unaware → to quantify the effect of including variability effects when throughput is matched
- Lose some benefit for fine-grained VFIs, gain for coarse-grained

Var.-aware Threshold or Greedy vs. LinOpt



- *LinOpt* power budget set equal to power used by alternate scheme
- Variability-awareness mean benefits up to 10%
- *LinOpt* performance highly dependent on linearizing accuracy

Power Profile Results



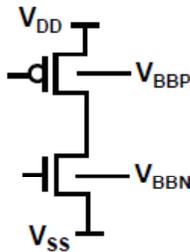
- Variability-awareness smoothes power profile
- Reduces standard deviation of per-core power distribution
 - 17% reduction in mean for *Threshold*
 - 38% reduction in mean for *Greedy*

Outline

- ✓ Motivation
- ✓ Variability and Power Management
 - ✓ Variation-aware DVFS
 - ▼ Adaptive Body-Biasing and interaction with DVFS
 - ▼ Limits for dynamic power management
- Summary

Adaptive Body-Biasing (ABB)

- Powerful technique to mitigate variations in leakage power dissipation [Tschanz et al. JSSC'02]



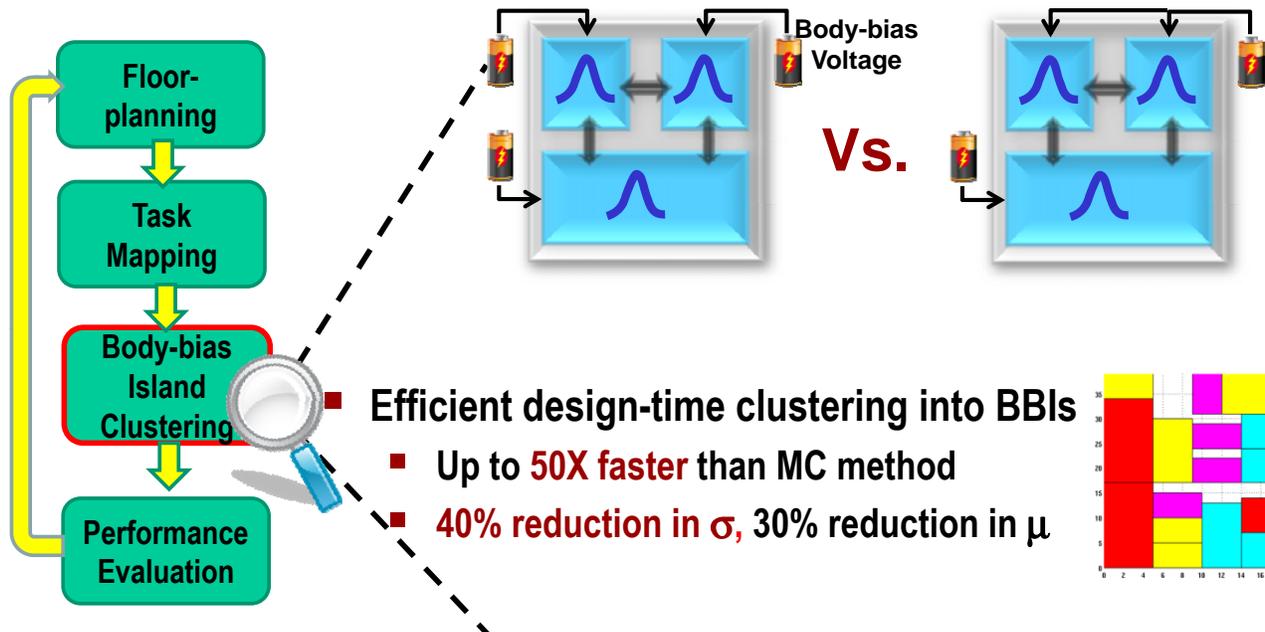
$V_{BBN} > 0$ (Forward Body-bias): ↑ leakage, ↓ delay

$V_{BBN} < 0$ (Reverse Body-bias): ↓ leakage, ↑ delay

- Each fabricated die tested and assigned appropriate body-bias voltage based on measured leakage current
 - ▼ **Global Body-bias** : single body-bias voltage for entire die
 - ▼ **Multiple Body-bias** : die partitioned into “body-bias islands”

Methodology for a Good Static Solution

- System-level Adaptive Body-bias with Multiple Body-Bias Islands (BBIs) [Garg and Marculescu CODES-ISSS'08]

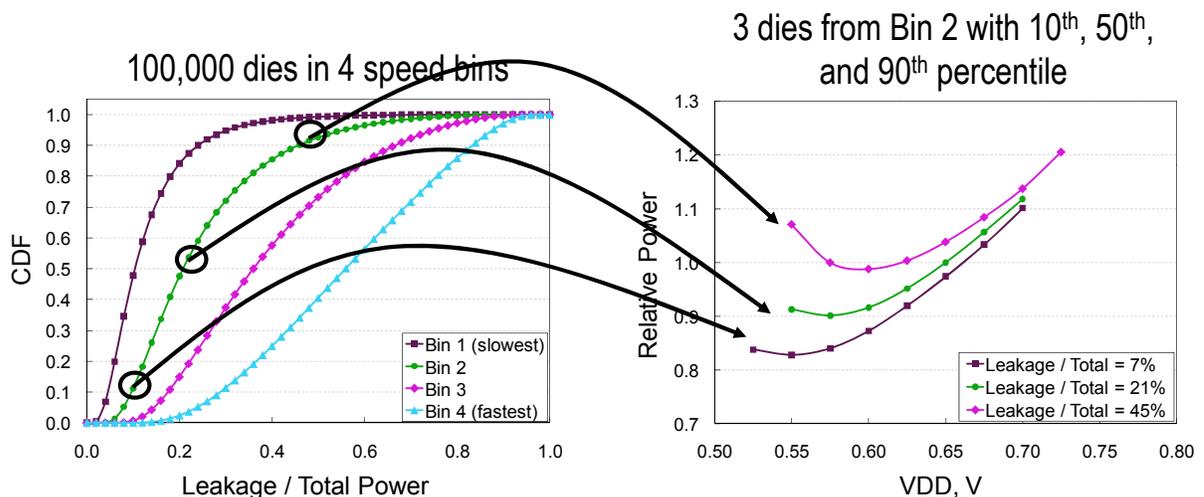


How About Combining Body Biasing & DVFS?

- V_{DD} and body biasing provide two power/performance knobs
 - ▼ Nominal V_{DD} with RBB may not yield best power for given frequency
 - ▼ V_{DD} has stronger effect on dynamic power, BB has stronger effect on static power
- Independent implementation of DVFS and body biasing
 - ▼ DVFS algorithms may stay unchanged
 - ▼ Reclaim frequency margin by adjusting body bias until frequency is exactly met
- *Integration of DVFS and body biasing*
 - ▼ The system specifies desired frequency
 - ▼ Goal is to choose the V_{DD} / BB combination with the lowest total power

Main Motivation

- Large variation in leakage as percent of total power
- Leads to large variation in optimal V_{DD} / BB combination
 - ▼ Lower % leakage needs lowest V_{DD} for minimum power
 - ▼ Higher % leakage needs highest V_{DD} for minimum power



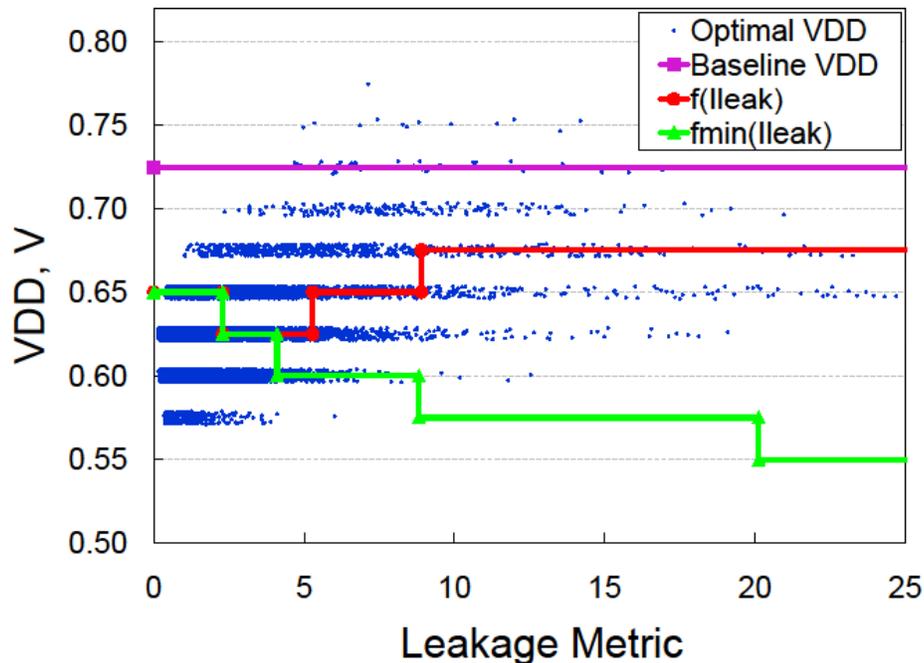
Proposed Approach

- Delay the $\{ V_{DD}, f \}$ mapping until test-time [Bonnoit et al. ISLPED09]
 - ▼ Exploit variability information for each core (or VFI)
- Available frequency levels are chosen as usual
- V_{DD} for each f is chosen at test based on a single leakage measurement
- Function mapping leakage to V_{DD} for each f defined once per technology / product
- Body biasing used to reclaim performance margin

Determining leakage to V_{DD} mapping $f(I_{LEAK})$

- Need to consider both optimal and minimum V_{DD}
 - ▼ Need to ensure most dies can meet frequency with V_{DD} at worst-case temperature
 - ▼ Want to get as close to optimal V_{DD} as possible at typical temperature
 - ▼ Two dies might have same leakage, but optimal V_{DD} of one is lower than minimum V_{DD} of the other
- Methodology – determine :
 - ▼ For each chip
 - Speed bin
 - For each core
 - Leakage @ typical temperature, highest V_{DD} , zero BB
 - For each frequency level
 - » Optimal V_{DD} @ typical temperature, with body biasing
 - » Minimum V_{DD} @ highest temperature, full FBB

Example Mapping

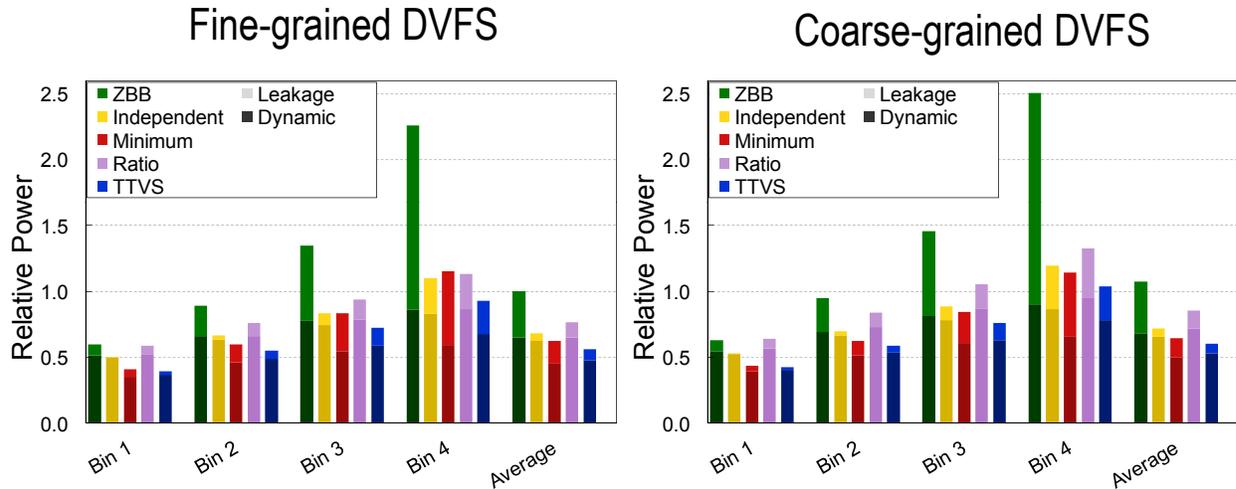


- For each speed bin and frequency level, find Vdd by minimizing the overall error from the optimal Vdd across all cores

Example Schemes

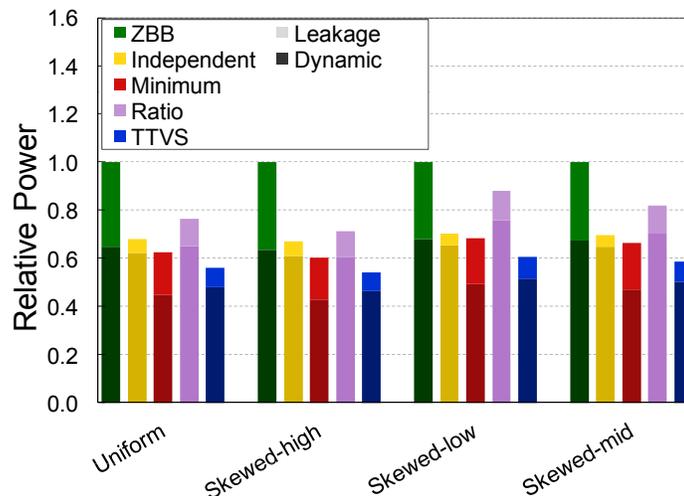
- *ZBB*: Traditional DVFS with no body-biasing
- *Independent*: Independent ABB and DVFS
- *Minimum*: ABB and DVFS, run each core at its minimum V_{DD}
 - ▼ Assume this could be found at test (even though cost would be prohibitive)
- *Ratio*: V_{DD} and BB set to meet f , achieve target ratio of switching to total power [Nomura JSSC'06]
 - ▼ Ratio chosen to minimize total power across all frequency levels in Monte Carlo
- *TTVS*: Proposed scheme

Results by Speed Bin and DVFS Granularity



- **Minimum** generally reduces power, but not when leakage is high
- **Ratio** does poorly because optimal power ratio highly variable
- **Results very consistent**
 - ▼ **TTVS** saves 18% / 16% of power relative to *Independent*
 - ▼ **TTVS** saves 11% / 7% of power relative to *Minimum*

Results by DVFS Time Distribution



- **Same trends hold across various distributions of time per voltage level**
 - ▼ **Uniform** → the amount of time spent at each voltage level is uniformly distributed
 - ▼ **Skewed-high, low or mid** → time spent at each level is proportional to the level i , $n-i$, or $\min(n, n-i)$ (n = total number of levels)

Outline

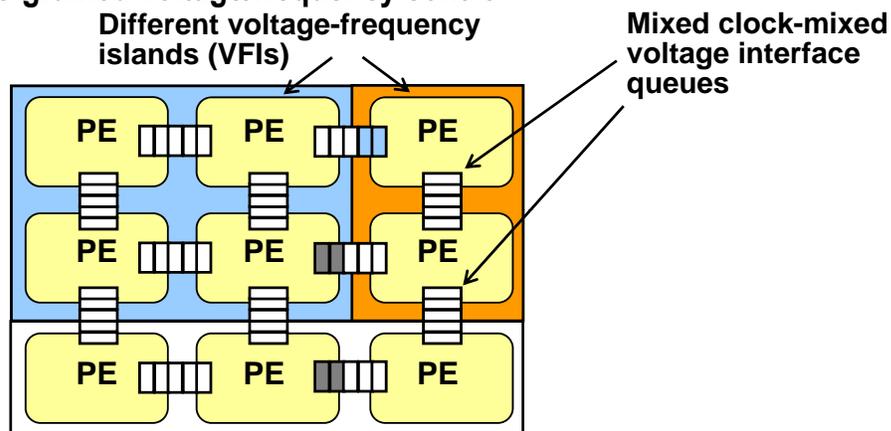
- ✓ Motivation

- ✓ Variability and Power Management
 - ✓ Variation-aware DVFS
 - ✓ Body-Biasing and interaction with DVFS
 - ▼ Limits for dynamic power management

- Summary

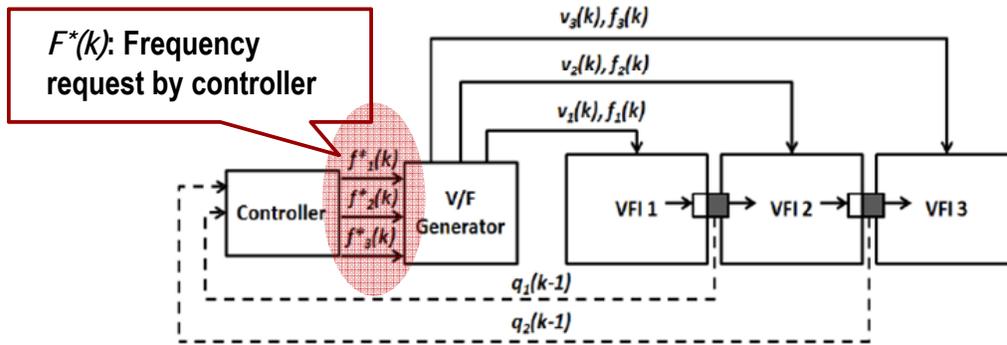
What Are the Limits of Controllability?

- Consider the case of systems with on-chip network-based communication and multiple VFIs
 - ▼ Increased scalability
 - ▼ Reduced design complexity
 - ▼ Fine-grained voltage/frequency control



- What are the limits in controlling such systems *in the presence of variations?*

Technology-driven Limits



- Due to technology constraints, V/F controller cannot always ensure $F^*(k) = F(k)$

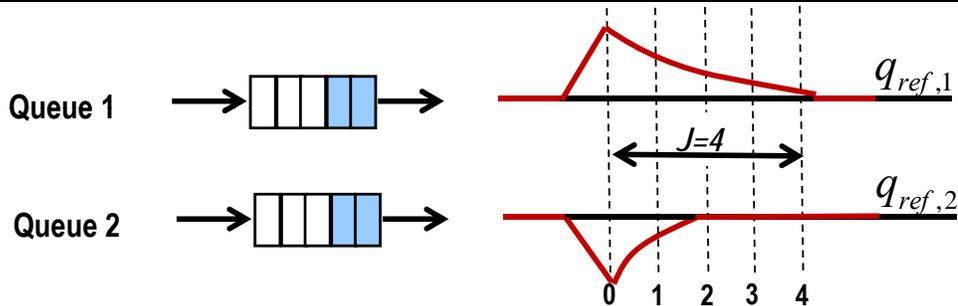
- ▼ Reliability driven upper limit on voltage/frequency

$$F(k) \leq F_{\max}$$

- ▼ Inductive noise and voltage-regulator speed limited constraint on maximum frequency increment

$$|F(k+1) - F(k)| \leq F_{\text{step}}$$

Performance Specification



- Reference queue occupancies: $Q_{\text{ref}} \in \mathbb{R}^N$
- Assume $Q(0) \neq Q_{\text{ref}}$ at control interval 0
- The controller must bring the queues back to the reference value in **at most** J control intervals: $Q(J) = Q_{\text{ref}}$

How do technology-driven factors impact DVFS control performance?

Time-optimal Control

- Queue occupancies after J steps can be written as:

$$Q(J) = Q(0) + TB \sum_{k=0}^{J-1} F(k) \quad (1)$$

- Technology-driven constraints from before:

$$F(k) \leq F_{\max} \quad (2)$$

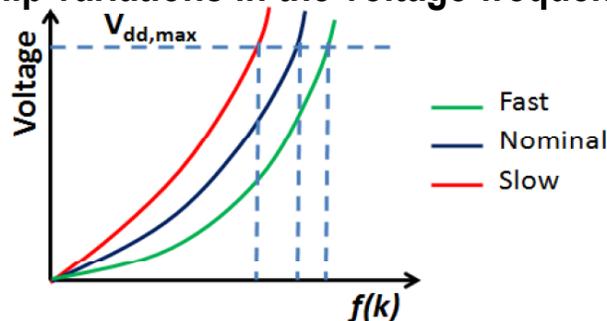
$$|F(k+1) - F(k)| \leq F_{\text{step}} \quad (3)$$

- (1), (2) and (3) define a Linear Program (LP)

- ▼ If the LP is *feasible* the solution $[F(0), F(1), \dots, F(J-1)]$ is a time-optimal control strategy
- ▼ If the LP is *infeasible* the performance specification cannot be met, irrespective of the control algorithm

Process Variations

- Impact of process variations on DVFS controller performance [Garg et al. DAC09]
- Chip-to-chip variations in the voltage-frequency curves of VFIs



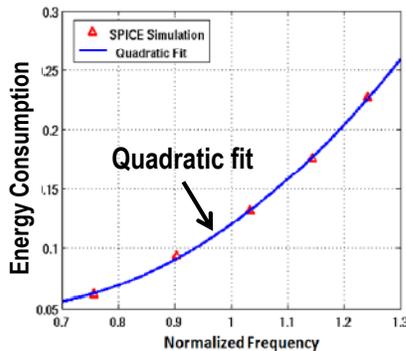
- Assuming maximum supply voltage is fixed, F_{\max} will be different for each manufactured die
- Probability of Controllability (PoC): % of manufactured die that meet performance specification

Explicit Energy Minimization

- Objective: minimize energy spent by controller to reach the steady state

$$E_{total} = \sum_{i=1}^M \sum_{k=1}^J TC_i V_i(k)^2 f_i(k)$$

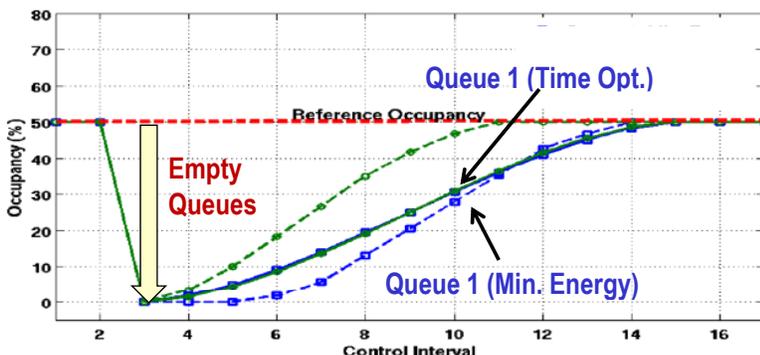
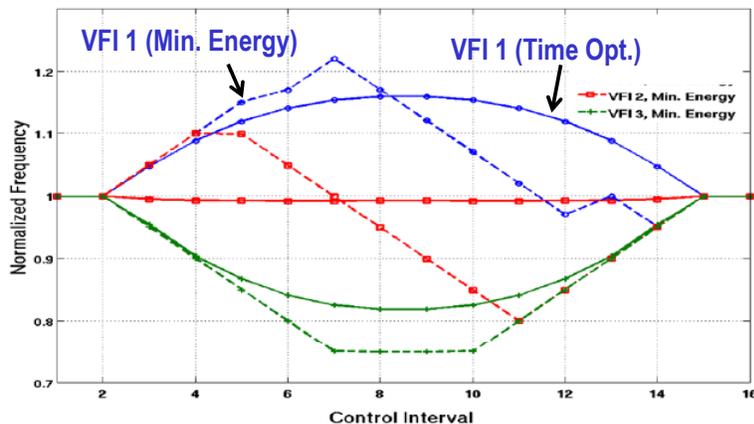
- Approximate E_{total} only as a function of $f_i(k)$ since constraints are also functions of the VFI frequencies



$$E_{total} \approx \sum_{i=1}^M \sum_{k=1}^J \alpha_i f_i(k)^2 + \beta_i f_i(k) + \lambda_i$$

Previous Linear Programming (LP) problem converted to a Quadratic Program (QP)

Experimental Results



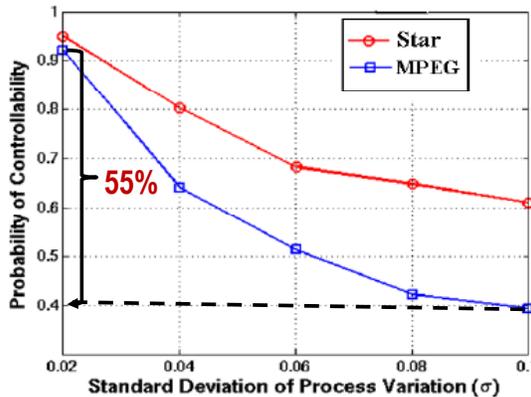
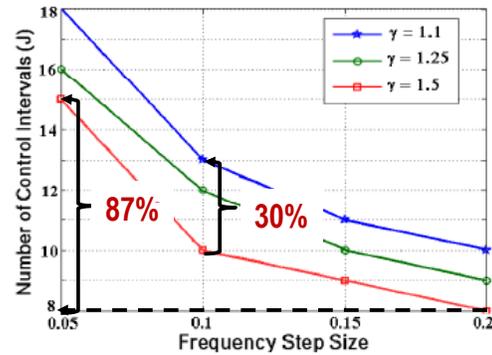
- Controller response for MPEG-2

- Both queues empty
- $J = 10$
- $\gamma = f_{max}/f_{nom} = 1.5$
- $f_{step} = 10\% f_{nom}$

- Observed about 9% energy savings for minimum energy controller

Experimental Results

- Up to **87% loss in performance** as step size is reduced
 - ▼ Up to **30% loss in performance** as γ is reduced



- ◆ Up to **55% reduction in PoC** for increasing magnitude of process variations

Summary

- Including process variation information in power control algorithms is essential
 - ▼ Lose significant power savings at iso-throughput or performance at iso-power
 - ▼ Customized algorithms suboptimal \rightarrow best bet are variation-aware versions of already existing dynamic control algorithms
- Scalability and controllability of dynamic power management algorithms are key
 - ▼ Especially with increased number of cores ...
 - ▼ ... and increased impact of variations multi-core systems

Conclusions

- **Multiple voltage and clock domains are widely used in modern processor design to manage power and process scaling issues**
 - ▼ Increased use of GALS clocking for large SoC designs
- **NOCs are for large SoCs**
 - ▼ Large SoCs = multiple clock domains
 - ▼ NoCs should be asynchronous
- **Dynamic V/F control yields significant power savings over static approaches while being robust to workload variations**
 - ▼ Precise controllability/stability conditions can be defined for DVFS control
- **Including process variation information in power control algorithms is essential**
 - ▼ Lose significant power savings at iso-throughput or performance at iso-power
- **Great research area to work on!**

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