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Abstract: In this document, we describe an interface called MAI. This interface allows developers to manage memory affinity in NUMA architectures. The affinity unit in MAI is a variable or an object of the parallel application. A set of memory policies implemented in MAI can be applied to these variables/objects in a easy way. High-level functions implemented in MAI minimize developers work when managing memory affinity in NUMA machines. MAI's performance was evaluated on two different NUMA machines using three different parallel applications. Results obtained with MAI present important gains when compared with the standard memory affinity solutions.

Key-words: multi-core architecture, memory affinity, static data, performance evaluation, programming

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MAI: Interface pour la Affinité de Mémoire

Résumé : Ce document décrit MAI, une interface pour contrôler l'affinité de mémoire sur des architecture NUMA. L'unité d'affinité utilisé par MAI est une variable ou un objet de l'application. MAI dispose d'un ensemble de politiques de mémoire qui peuvent être appliquées pour la variable/objet du une application d'une façon simple. Fonctions de haut-niveau mis en œuvre en minimiser les travaux des programmeurs. Les performance de MAI sont évaluée sur deux différents NUMA machines utilisant trois applications parallèles. Les résultats obtenus avec cette interface présente d'importants gains par rapport aux solutions standard.

Mots-clés : architectures NUMA, affinité mémoire, données statiques, étude de performances

1 Introduction

Parallel applications are generally developed using message passing or shared memory programming models. Both models have their advantages and disadvantages. The message passing model scales better, however, is more complex to use. In the other hand, shared memory programming model is less scalable but easier to be used by the developer. The latter programming model can be used in parallel applications development with libraries, languages, interfaces or compilers directives. Some examples are Pthreads [1], OpenMP [2], TBB [3] etc.

Shared memory programming model is the ideal model for traditional UMA (Uniform Memory Access) architectures, like symmetric multiprocessors. In these architectures the computer has a single memory, which is shared by all processors. This single memory often becomes a bottleneck when many processors accesses it at the same time. The problem gets worse as the number of processors increase, where the single memory controller does not scale.

The limitation of classical symmetric multiprocessors (SMP) parallel systems can be overcome with NUMA (Non Uniform Memory Access) architectures. These architectures have as main characteristics, multiple memory levels that are physically distributed but, seen by the developer as a single memory [4]. NUMA architectures combine the efficiency and scalability of MPP (Massively Parallel Processing) with the programming facility of SMP machines [5]. However, due to the fact that the memory is distributed between the machine nodes, the time spent to access it is conditioned by the distance between the processor and data. The memory access by a given processor could be local (data is close) or remote (it has to use the interconnection network to access the data) [5, 6] .

As these machines are being used as servers for applications that demand a low response time it is important to assure memory affinity on them. Memory affinity is the guarantee that processing units will always have their data close to them. So, to reach the maximum performance on NUMA architectures it is necessary to minimise the number of remote access during the application execution. Which is, processors and data need to be scheduled so as the distance between them are the smallest possible [5, 6, 7, 8].

To reduce this distance and consequently increase the application performance in these architectures, many different solutions were proposed. These solutions are based in algorithms, mechanisms and tools that do memory pages allocation, migration and replication to guarantee memory affinity in NUMA systems for an entire process [5, 9, 6, 7, 10, 11, 12, 4, 13, 14, 15, 4, 16]. However, none of these solutions provides variable/object as memory affinity control unit. In these solutions, memory affinity is assured applying a memory policy for an entire process. Thus, developers can not express the different data access patterns of their application. This can result in a not ideal performance, because memory affinity are related with the program most important variables/objects (importance in means of memory consuption and access).

Thus, to allow different memory policies for each most important variable/object of an application and consequently a better control of memory affinity we developed MAI (Memory Affinity Interface). In this repport we introduce MAI, an interface developed in C that defines some high level functions to deal with memory affinity in NUMA architectures. The main advantages of MAI are:

allow different memory policy for each most important object/variable of the application, provide several standard and new memory policies and is an easy way to control memory affinity in parallel applications. In order to evaluate MAI performance we made some experiments with some memory-bound applications (MG from benchmark NAS [17], Ondes 3D [18] and ICTM [19]) in two different NUMA machines. We then compared the results obtained with MAI with Linux standard policy for NUMA machines [11] and the solution most used by developers of parallel application for NUMA machines [17]. This last solution is based in parallel initialization of data, threads and processes touch data to place it close to them (in this work we will call this solution Parallel-Init).

The repport is structured as follows. In section 2 we describe the previous solutions in memory affinity management for NUMA architectures. Section 3 depicts our interface and its main functionalities. In section 4 we present and discuss the performance evaluation of MAI. In the last section we present our conclusions and future works.

2 Memory Affinity Management Solutions

A lot of work has been donne in memory affinity management for NUMA architectures. Most of them are proposals of new memory policies that have some intelligent mechanism to place/migrate memory pages. Other types of works are proposal of new directives to OpenMP and some support integrated in the operating system. In this section we present these three groups of related works.

2.1 Memory Affinity Policies

In the work [9], authors present a new memory policy called *on-next-touch*. This policy allows data migration in the second time of a thread/process touch it. Thus, threads can have their data in the same node, allowing more local access. The performance evaluation of this policy was donne using a real application that has as main characteristic irregular data access patterns. The gain obtained with this solution is about 69% with 22 threads.

In [20], the authors present two new memory policies called skew-mapping and prime-mapping. In the first one, allocation of memory pages is donne skipping one node per round. As example, suppose that we have to allocate 16 memory pages in four nodes. The first four pages will be placed in nodes 0,1,2,3, the next four in nodes 1,2,3,4 and so on. The prime-mapping policy works with virtual nodes to allocate data. Thus, after the allocation on the virtual nodes there is a re-allocation of the pages in the real nodes. As scientific applications always work in power of 2, for data distribution, these two policies allows better data distribution. The gains with this solutions are about 35% with some benchmarks.

The work [16] present two algorithms to do page migration and assure memory affinity in NUMA machines. These algorithms use information get from kernel scheduler to do migrations. The performance evaluation show gains of 264% considering existed solution as comparison.

2.2 Memory Affinity with OpenMP Directives

In [21], authors present a strategy to assure memory affinity using OpenMP in NUMA machines. The idea is to use information about schedule of threads and data and made some relations between them. The work do not present formal OpenMP extensions but shows some suggestions of how this can be donne and what has to be included. All performance evaluation was donne using tightly-coupled NUMA machines. The results show that their proposal can scale well in the used machines.

In the work [11], authors present new OpenMP directives to allow memory allocation in OpenMP. The new directives allows developers to express how data have to be allocated in the NUMA machine. All memory allocation directives are for arrays and Fortran programming language. The authors present the ideas for the directives and how they can be implemented in a real compiler.

2.3 Memory Affinity with Operating System Support

NUMA support is now present in several operating systems, such as Linux and Solaris. This support can be found in the user level (with administration tools or shell commands) and in the kernel level (with system call and NUMA APIs) [4].

The user level support allows the programmer to specify a policy for memory placement and threads scheduling for an application. The advantage of using this support is that the programmer does not need to modify the application code. However, the chosen policy will be applied in the entire application and we can not change the policy during the execution.

The API NUMA is an interface that defines a set of system calls to apply memory policies and processes/threads scheduling. In this solution, the programmer must change the application code to apply the policies. The main advantage of this solution is that we can have a better control of memory allocation.

The use of system calls or user level tools to manage memory affinity in NUMA machines can generate some gains. However, developers must know the application and architecture characteristics. To use system calls, developers need to change the application source code and make the memory management by themselves. This is a complex work and depending on the application we can not achieve expressive gains. User level solutions require from developers several shell commands and do not allow fine control over memory affinity.

2.4 Conclusion on Related Works

MAI is the solution that allows variable/object as unit of memory affinity management in an easy way. None of the solutions presented let developers manage memory affinity in NUMA machines using the most important variable/object. Also, MAI is an easy way to develop applications considering memory affinity, no complex code or modification are necessary to do it.

3 MAI

In this section we describe MAI and its features. We first describe the interface proposal and its main contributions. Then, we explain its high level functions and memory policies. Finally, we describe its implementation details and usage. MAI can be download from [22]

3.1 The Interface

MAI is a library developed in C that defines some high level functions to deal with memory affinity in applications executed in NUMA architectures. This library allows developers to manage memory affinity considering the most importnat variable/object of their applications (importance in terms of memory consuption and access). This characteristic makes memory management easier for developers because they do not need to care about pointers and pages addresses like in the system call APIs for NUMA (libnuma in Linux for example [4]). Furthermore, with MAI it is possible to have a fine control over memory affinity; memory policies can be changed through application code (different policies for different phases). This feature is not allowed in user level tools like numactl in Linux.

The library has four memory policies: *cyclic*, *cyclic_block*, *bind_all* and *bind_block*. In *cyclic* policies the memory pages that contain the variable/object data are placed in physical memory making a round with the memory blocks. The main difference between *cyclic* and *cyclic_block* is the amount of memory pages used to do the cyclic process. In *bind_all* and *bind_block* policies the memory pages that contain the variable/object data are placed in memory blocks specified by the application developer. The main difference between *bind_all* and *bind_block* is that in the latter, pages are placed in the memory blocks that have the threads/process that will make use of them.

These memory policies can be combine during the application steps to implement a new memory policy. Variables/objects generally are accessed in different ways during the application. Thus, it is important give to the developer the opportunity to develop/create a memory policy for his application. The majority of the new proposed memory affinity algorithms do not allows memory policies changes during the applications execution. Also, in MAI it is also possible to do memory migration to optimize any incorrect memory placement.

3.2 High-Level Functions

To develop applications using MAI the programmer just have to use some high-level functions. The functions are divided into five groups: system, allocation, memory, threads and statistic.

System Functions: the system functions are dived in functions to configure the interface and functions to see some information about the platforms. The configuration functions must be called in the begin (init()) and end (final()) of the application code. The function init() is responsible for setting the nodes and threads Ids that will be used for memory/thread policies and for the interface start. This function can receive as parameter a file name. The file is an environment configuration file that gives information about the memory blocks and

processors/cores of the architecture. If no file name is give the interface chose which memory blocks and processors/cores to use. The final() function is used to finish the interface and free any data that was allocated by the developer.

```
void init(char filename[]);
void final();

int get_num_nodes();
int get_num_threads();
int get_num_cpu();
unsigned long* get_nodes_id();
unsigned long* get_cpus_id();
void show_nodes();
void show_cpus();
```

Allocation Functions: these functions allows the developer allocate arrays of C primitive types (CHAR, INT, DOUBLE and FLOAT) and not primitive types, like structures. The functions need the number of items and the C type. Their return is a void pointer to the allocated data. The memory is always allocated sequentially, like a linear (1D) array. This strategy allow better performance and also make easer to define a memory policy for an array. Example presented in (Figure 1).

```
void* alloc_1D(int nx,size_t size_item,int type);
void* alloc_2D(int nx,int ny,size_t size_item,int type);
void* alloc_3D(int nx,int ny,int nz,size_t size_item,int type);
void* alloc_4D(int nx,int ny,int nz,int nk,size_t size_item, int type);
void free_array(void *p);
```

Memory Policies Functions: these functions allows the developer to select a memory policy for an application and to migrate data between the nodes. There are four differents policies: *cyclic*, *cyclic_block*, *bind_all* and *bind_block*. It is also possible to migrate pages between the nodes of the NUMA system using the functions migrate_*. Example presented in (Figure 2).

```
void cyclic(void *p);
void cyclic_block(void *p);
void bind_all(void *p);
void bind_block(void *p);
void migrate_page(void *p,unsigned long node);
void migrate_all_scatter(void *p,unsigned long mask);
void migrate_all_gather(void *p,unsigned long mask);
void migrate_pages(void *p,int np,unsigned long node);
```

Thread Policies Functions: these functions allows the developer to bind or migrate a thread to a cpu/core in the NUMA system. The functions get_thread_id must be called before bind_threads to set the threads Ids in the interface data structure. The function bind_threads use these Ids and the cpu/core mask (giving in the configuration file) to bind threads.

```
#include <communs.h>
#include <memory_policies.h>
#include <alloc_memory.h>

int main(int argc, char* argv[])
{
  int i,j;
  char **t; //pointer to 2D array

  //Alloc a 2D array - Need the X and Y dimensions and the C type
  t = (char**) alloc_2D(64,64,sizeof(char),CHAR);

  //using the allocated array
  for(i=0;i<64;i++)
    for(j=0;j<64;j++)
    t[i][j]=0;

 //free memory
 free_array(t);
}
```

Figure 1: Alloc functions example

```
void bind_threads();
void migrate_thread(pid_t id,unsigned long cpu);
```

Statistics Functions: these functions allows the developer to get some information about the application execution in the NUMA system. There are statistics of memory and threads placement/migration and overhead from migrations.

```
void print_pagenodes(unsigned long *pageaddrs,int size);
int number_page_migration(unsigned long *pageaddrs,int size);
double get_time_pmigration();
int number_thread_migration(unsigned int *threads,int size);
double get_time_migration();
```

3.3 Implementation Details

MAI interface is implemented in C for Linux based NUMA systems. Developers who wants to use MAI have to program their applications using shared memory programming model. The allowed shared memory libraries are: Posix threads or OpehMP. To use this interface, *libnuma* must be installed in the NUMA system. Figure 3 present the architecture of the interface.

```
#include <communs.h>
#include <memory_policies.h>
#include <alloc_memory.h>

int main(int argc, char* argv[])
{
  int i,j;
  char **t; //pointer to 2D array

  //Alloc a 2D array - Need the X and Y dimensions and the C type
  t = (char**) alloc_2D(64,64,sizeof(char),CHAR);

  //function get the informations from a configuration file
  // and set in the interface
  init(argv[1]);

  //The memory pages of t will be place in a cyclic in the NUMA nodes
  //The cyclic starts in the node that first do a page fault
  cyclic(t);

  //using the allocated array
  for(i=0;i<64;i++)
    for(j=0;j<64;j++)
    t[i][j]=0;

  final();

}
```

Figure 2: Memory policies functions example

To guarantee memory affinity, all memory management is donne using MAI structures. These structures are loaded in the initialization of the interface (with the init() function) and are used in the rest of application execution. All allocations and memory policies algorithms consider the NUMA architecture before do any allocation and placement of memory pages in the memory blocks. A memory policy set for a variable/object of the application can be changed during the application steps. To do this developers just have to call the memory policy function for the variable/object and MAI will change it.

Threads scheduling in MAI is donne using one thread per processor/core strategy. This minimizes memory contention problem that exists in some NUMA architectures. If the number of threads are bigger then the number of processors/cores then, more threads per processor/core will be used.

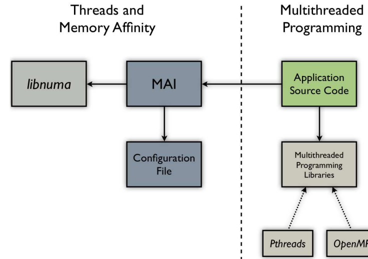


Figure 3: MAI Architecture

4 Performance Evaluation

In this section we present the performance evaluation of MAI. We first describe the two NUMA platforms used in our experiments. Then, we describe the applications and their main characteristics. Finally, we present the results and their analysis.

4.1 NUMA Platforms

In our experiments we used two different NUMA architectures. The first NUMA architecture is an eight dual core AMD Opteron with 2.2 GHz of frequency and 2 MB of cache memory for each processor. The machine is organized in eight nodes and has in total 32 GB of main memory. This memory is divided in eight nodes (4 GB of local memory) and the system page size is 4 KB. Each node has three connections which are used to link with other nodes or with input/output controllers (node 0 and node 1). These connections give different memory latencies for remote access by nodes (NUMA factor from 1.2 to 1.5). A schematic figure of this machine is given in Figure 4. We will use the name Opteron for this architecture.

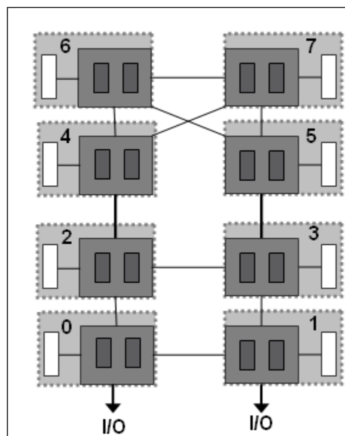


Figure 4: AMD Opteron NUMA architecture.

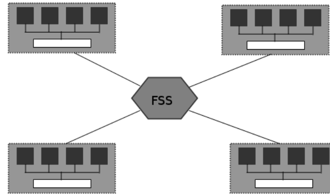


Figure 5: Itanium 2 NUMA architecture.

The operating system that has been used in this machine is Linux version 2.6.23-1-amd64 and the distribution is Debian with support for NUMA architecture (system calls and user API numactl). The compiler that has been used for the OpenMP code compilation was the GNU Compiler Collection (GCC).

The second NUMA architecture used is a sixteen Itanium 2 with 1.6 GHz of frequency and 9 MB of L3 cache memory for each processor. The machine is organized in four nodes of four processors and has in total 64 GB of main memory. This memory is divided in four blocks in each node (16 GB of local memory). The nodes are connected using a FAME Scalability Switch (FSS), which is a backplane developed by Bull [23]. This connection gives different memory latencies for remote access by nodes (NUMA factor from 2 to 2.5). A schematic figure of this machine is given in Figure 5. We will use the name Itanium 2 for this architecture.

The operating system that has been used in this machine was the Linux version 2.6.18-B64k.1.21 and the distribution is Red Hat with support for NUMA architecture (system calls and user API numactl). The compiler that has been used for the OpenMP code compilation was the ICC (Intel C Compiler).

4.2 Applications

In our experiments we used three different applications: one from benchmark Nas, Ondes 3D and ICTM. All the applications have as main characteristics high memory consumption, number of data access and regular and/or irregular data access patterns. A regular data access pattern is defined in this work as: thread or process of an application access the same data set during the initialization and computational steps of the application. The irregular data access patterns is the contrary. Threads or process of an application do not access the same data set during the initializations and computational steps of the application. All applications were developed in C using OpenMP to code parallelization.

One of the three applications is a kernel from NAS benchmark [17] called MG. This kernel were selected because they are representative in terms of computations and present memory important characteristics. MG is a kernel that uses a V cycle MultiGrid method to calculate the solution of the 3D scalar Poisson equation. The main characteristic of this kernel is that it tests both short and long distance data movement. Figure 6 present a schema of the application.

```
#pragma omp parallel for
    for (i=0 to i<rows)
     for (j=0 to j<columns)
       for (k=0 to k<planes)
          _mat[i][j][k] = ...

     for (i=0 to i<rows)
    #pragma omp parallel for
     for (j=0 to j<columns)
       for (k=0 to k<planes)
        _mat[i][j][k] = ...

  #pragma omp parallel for
    for (i=0 to i<rows)
     for (j=0 to j<columns)
       for (k=0 to k<planes)
        _mat[i][j][k] = mat[-+i][-+*j][-+*k]
             ...
```

Figure 6: Multi Grid

Ondes 3D is a seismology application simulates the propagation of a seismic in a 3 dimension region [18]. This application has three main steps: data allocation, data initialization and propagation calculus (operations). In the allocation step all arrays are allocated. The initialization is important because the data are touched and physically allocated in the memory blocs. The last step is composed by two big calculus loop. In these loops all arrays are accessed for write an read but, with the same access patterns of the initialization step. Figure 7 present a schema of the application.

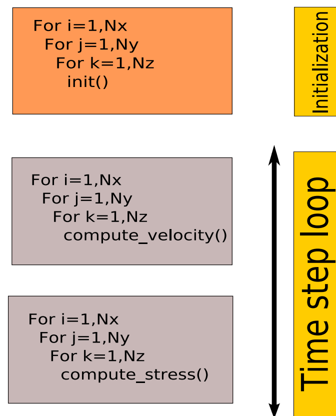


Figure 7: Ondes 3D Application

ICTM is a multi-layered and multi-dimensional tessellation model for the categorization of geographic regions considering several different characteristics (relief, vegetation, climate, land use, etc.) [19]. This application has two main steps: data allocation-initialization and classification computation. In the allocation-initialization step all arrays are allocated and initialized. The second

step is composed by four big calculus loops. In these loops all arrays are accessed for write an read but, with the regular and irregular access patterns.Figure 8 present a schema of the application.

```
for (i=0 to rows)
 for(j=0 to columns)
   init_matrices();
```

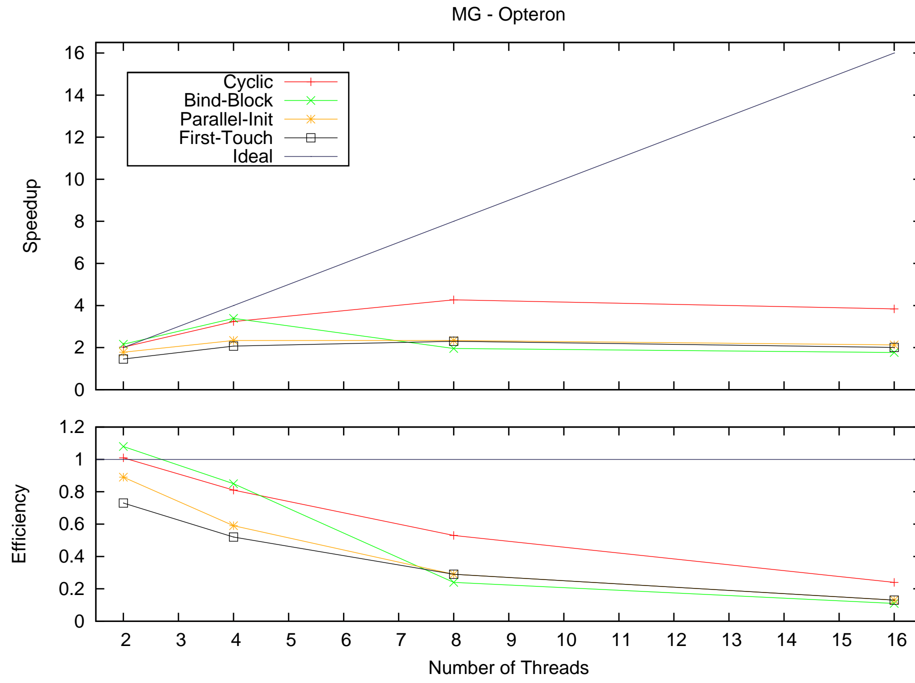
```
 function compute_relative_matrix() {
  #pragma omp parallel for
  for (i=0 to i<rows)
    for (j=0 to j<columns)
      //relative matrix computation}

function compute_interval_matrices() {
  #pragma omp parallel for
  for (i=0 to i<rows)
    for (j=0 to j<columns)
      //interval matrices computation}

function compute_status_matrix() {
  #pragma omp parallel for
    for (i=0 to i<rows)
      for (j=0 to j<columns)
      if (element is in radius)
       //status matrix computation using radius elements
        mat_stat[i][j] = mat[-+i][-+j] .....
}

function compute_limits_matrix() {
  #pragma omp parallel for
  for (i=0 to i<rows)
    for (j=0 to j<columns)
      //limits matrix computation
                             }
```

Figure 8: ICTM Application

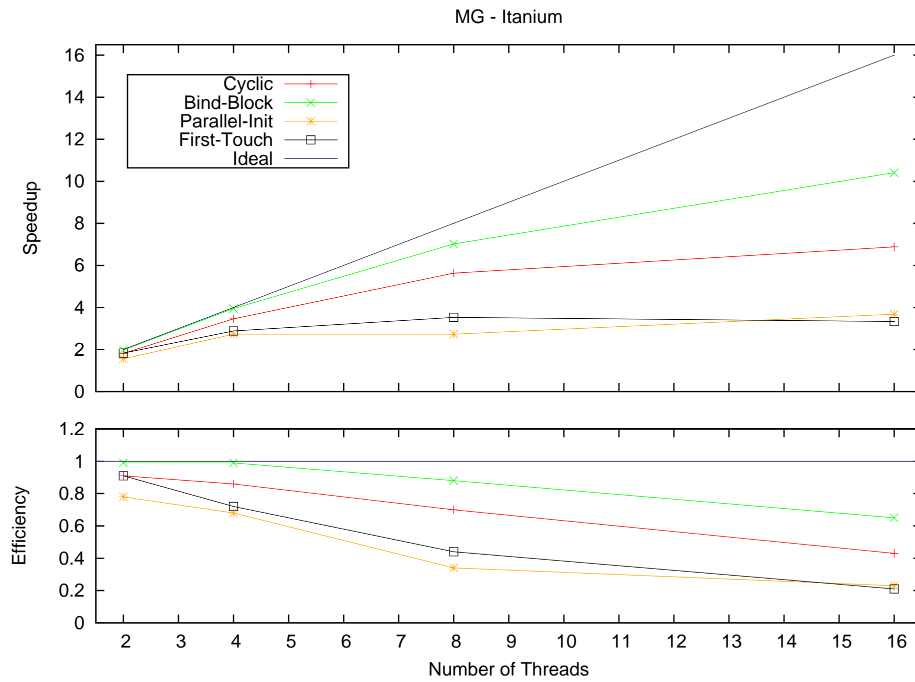
4.3 Results

In this section we present the results obtained with each application in the two NUMA machines with MAI and the two other solutions (Linux and Parallel-Init). The experiments were donne using 2,4,8 and 16 threads and a problem size of 256^2 elements fo MG, 2.0 Gbytes for ICTM and 2.4 Gbystes for Ondes 3D. As performance metrics we selected speedup (Sequential execution time/parallel execution time) and efficiency (speedup/number of threads).

In figure 9(a) we present the speedups and efficiencies for the MG application when executed in Opteron machine. As we can observe for this application and considering an Opteron NUMA machine the better memory policy is cyclic. This NUMA machine has as important caracthiristc a not so good network bandwidth. The optimization of bandwitdh in this machine is more important than the optimization of latency. As the NUMA factor in this machine is small the latency influence in this type of application is not high (irregular pattern access). Thus, distribute the memory pages in a cyclic way avoid contention and consequently the influence of network bandwidth in the application execution. The others memory policies had worst results because they try to optimize latency and as the problem in this machine is contention in network these policies do not present good results.



(a) Opteron Speedup-Efficiency



(b) Itanium Speedup-Efficiency

Figure 9: MG Application

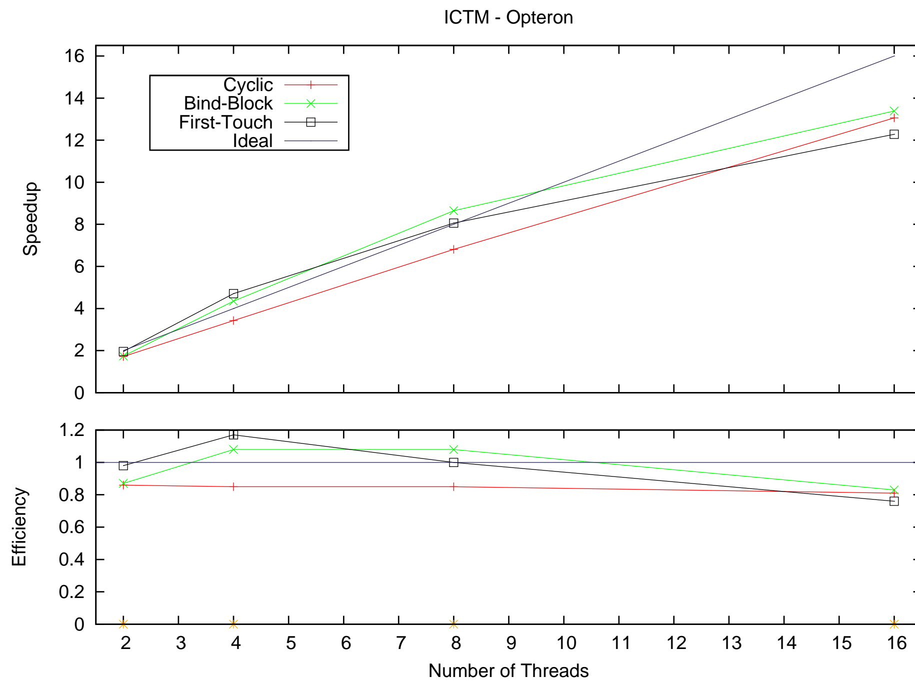
In figure 9(b) we present the speedups and efficiencies for the MG application for Itanium machine. The memory policy bind_block is the best one, as this machine has a high NUMA factor try to allocate data close to threads that use it is better. The cyclic memory policy had worst results because it try to optimize bandwidth and as the machine has a high NUMA factor this policy (optimize bandwidth)do not present good results. The other two policies, First-Touch and Parallel-Init also do not have good gains. First-touch policy centralize data in a node so, threads made a lot of remote and concurrent access on the same memory block. On the other hand, Parallel-Init try to distribute data between the machine nodes but, as the access patterns are irregular this strategy do not give good speedups and efficiencies.

In figures 10(a) and 10(b) we present the results for ICTM application considering the Opteron and the Itanium machines. For this application, as for MG, the better memory policies are cyclic for Opteron and bind_block for Itanium.

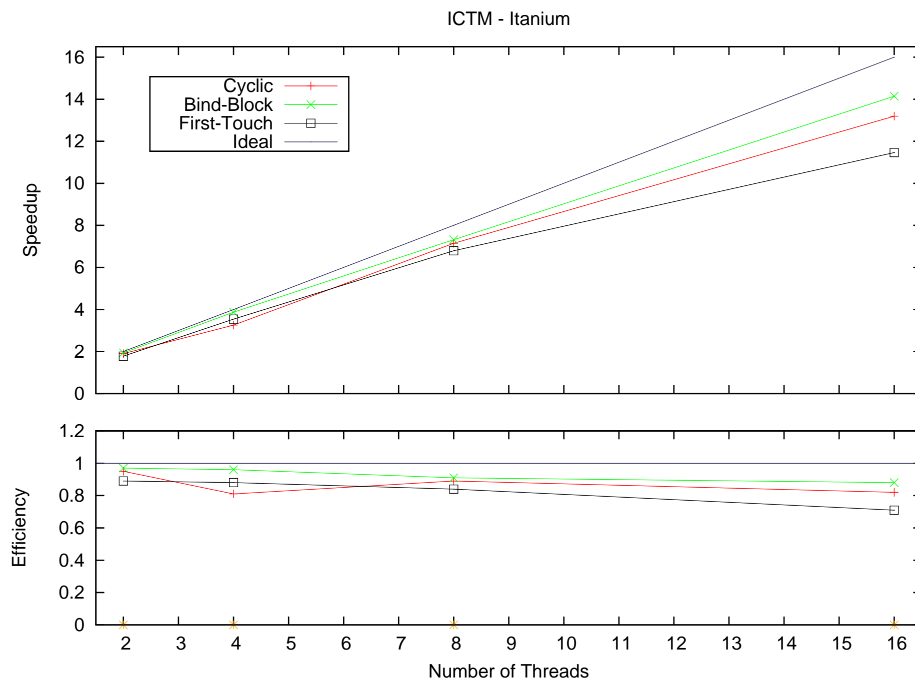
Opteron has a network bandwidth problem so, it is better to spread the data among NUMA nodes. By using this strategy, we reduce the number of simultaneous accesses on the same memory block. As a consequence of that, we can have a better performance. The *bind_all* and *bind_block* policies have presented worse speed-ups for Opteron machine. These policies allows a lot of remote access by threads and also do not consider network bandwidth in memory allocation.

We can see that the results for Itanium are quite different when we compare to those obtained over Opteron (Figure 10(b)). By allocating data closer to the threads which computes them, we decrease the high NUMA factor impact. As a result, *bind_block* was the best policy for this machine.

In figures 10(a) and 10(b) we present the results for ICTM application considering the Opteron and the Itanium machines. As we can observe the results with MAI policies, First-Touch and Parallel-Init solutions were very closer. The main reason for this is the regularity of data access patterns of this application. Threads always access the same set of memory pages. However, there is a little performance gain in the use of bind_block policy. This policy place threads and data in the same node, so it avoids remote access. In the other solutions threads can migrate or data are placed in a remote node allowing more remote access.

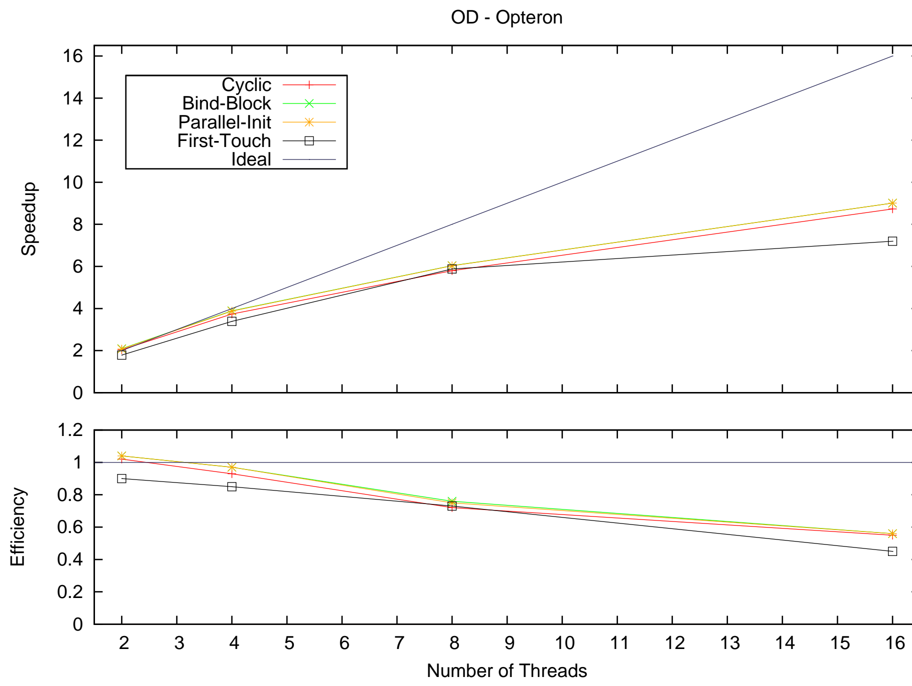


(a) Opteron Speedup-Efficiency

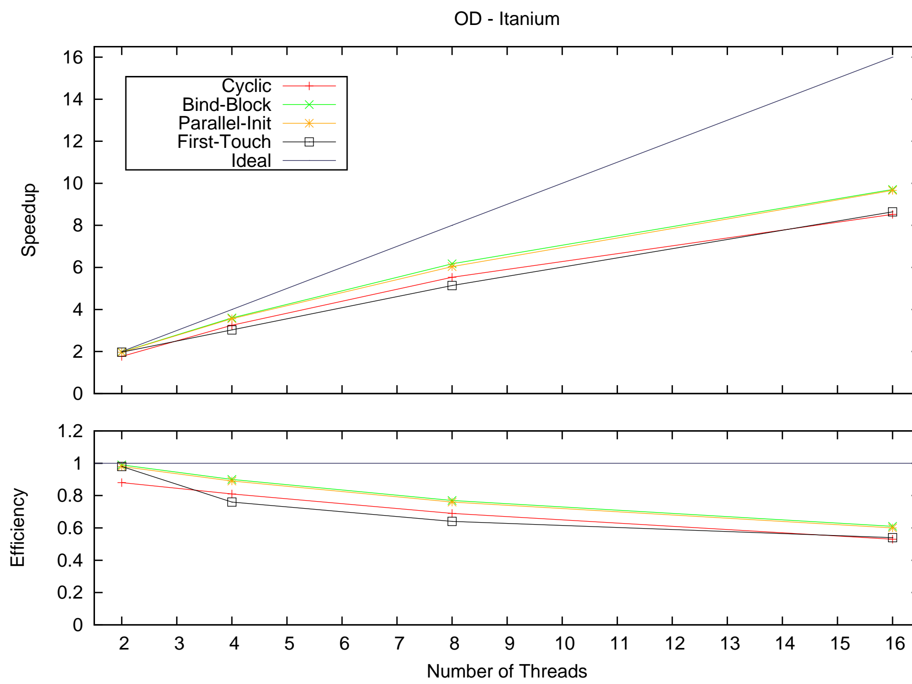


(b) Itanium Speedup-Efficiency

Figure 10: ICTM Application



(a) Opteron Speedup-Efficiency



(b) Itanium Speedup-Efficiency

Figure 11: Ondes 3D Application

5 Conclusion

In this report we presented an interface to manage memory affinity in NUMA machines called MAI. This interface has some memory policies that can be applied in the variable/objects of an application to assure memory affinity. MAI is also an easy way of manage memory in NUMA machines, high level functions allow developers to change their application with no big work.

The experiments made with MAI show that the interface has better performance than some proposed solutions. We evaluate MAI using three different applications and two NUMA machines. The results show gains of 2%-60% in relation of Linux memory policy and optimized application code version.

The work show that memory has to be manage in NUMA machines and that this management must be easy for the developer. Thus, an interface that helps developers to do this is essencial. As future works we highlight: MAI version that allows developers to implement new memory policies as plug-ins, new performance evaluation of MAI with others applications and integrate MAI in GOMP, the GCC implementation of OpenMP.

References

[1] D. R. Butenhof, "Programming with posix threads," 1997.

[2] "The openmp specification for parallel programming - http://www.openmp.org," 2008. [Online]. Available: http://www.openmp.org

[3] "Threading building blocks-http://www.threadingbuildingblocks.org/," 2008. [Online]. Available: http://www.threadingbuildingblocks.org/

[4] A. Kleen, "A NUMA API for LINUX," Tech. Rep., April 2005. [Online]. Available: http://whitepapers.zdnet.co.uk/0,1000000651,260150330p,00.htm

[5] T. Mu, J. Tao, M. Schulz, and S. A. Mckee, "Interactive Locality Optimization on NUMA Architectures," in *Software Visualization*, 2003. [Online]. Available: http://citeseer.ist.psu.edu/mu03interactive.html

[6] J. Marathe and F. Mueller, "Hardware Profile-Guided Automatic Page Placement for ccNUMA Systems," in *PPoPP '06: Proceedings of the eleventh ACM SIGPLAN symposium on Principles and practice of parallel programming*. New York, NY, USA: ACM, 2006, pp. 90–99. [Online]. Available: http://portal.acm.org/citation.cfm?id=1122987

[7] F. Bellosa and M. Steckermeier, "The Performance Implications of Locality Information Usage in Shared-Memory Multiprocessors," *J. Parallel Distrib. Comput.*, vol. 37, no. 1, pp. 113–121, August 1996. [Online]. Available: http://portal.acm.org/citation.cfm?id=241170.241180

[8] A. Carissimi, F. Dupros, J.-F. Mehaut, and R. V. Polanczyk, "Aspectos de Programacão Paralela em arquiteturas NUMA," in *VIII Workshop em Sistemas Computacionais de Alto Desempenho*, 2007.

[9] H. Löf and S. Holmgren, "Affinity-on-next-touch: Increasing the performance of an industrial PDE solver on a cc-NUMA system," in *ICS '05: Proceedings of the 19th annual international conference on Supercomputing*. New York, NY, USA: ACM, 2005, pp. 387–392. [Online]. Available: http://portal.acm.org/citation.cfm?id=1088149.1088201

[10] A. Joseph, J. Pete, and R. Alistair, "Exploring Thread and Memory Placement on NUMA Architectures: Solaris and Linux, UltraSPARC/FirePlane and Opteron/HyperTransport," 2006, pp. 338–352. [Online]. Available: http://dx.doi.org/10.1007/11945918_35

[11] J. Bircsak, P. Craig, R. Crowell, Z. Cvetanovic, J. Harris, C. A. Nelson, and C. D. Offner, "Extending OpenMP for NUMA machines," in *Supercomputing '00: Proceedings of the 2000 ACM/IEEE conference on Supercomputing (CDROM)*, 2000.

[12] L. T. Schermerhorn, "Automatic Page Migration for Linux," 2007.

[13] B. Verghese, S. Devine, A. Gupta, and M. Rosenblum, "Operating system support for improving data locality on CC-NUMA compute servers," in *ASPLOS-VII: Proceedings of the seventh international conference on Architectural support for programming languages and operating systems*. New York, NY, USA: ACM, 1996, pp. 279–289. [Online]. Available: http://portal.acm.org/citation.cfm?id=237090.237205

[14] R. Vaswani and J. Zahorjan, "The implications of cache affinity on processor scheduling for multiprogrammed, shared memory multiprocessors," *SIGOPS Oper. Syst. Rev.*, vol. 25, no. 5, pp. 26–40, 1991.

[15] R. Chandra, S. Devine, B. Verghese, A. Gupta, and M. Rosenblum, "Scheduling and page migration for multiprocessor compute servers," *SIGPLAN Not.*, vol. 29, no. 11, pp. 12–24, 1994.

[16] D. S. Nikolopoulos, T. S. Papatheodorou, C. D. Polychronopoulos, J. Labarta, and E. Ayguadé, "User-level dynamic page migration for multiprogrammed shared-memory multiprocessors," in *ICPP*, 2000, pp. 95–104.

[17] J. Y. Haoqiang Jin, Michael Frumkin, "The OpenMP Implementation of NAS Parallel Benchmarks and Its Performance," NAS System Division - NASA Ames Research Center, Tech. Rep. 99-011/1999, 1999. [Online]. Available: https://www.nas.nasa.gov/Research/Reports/Techreports/1999/PDF/nas-99-011.pdf

[18] F. Dupros, H. Aochi, A. Ducellier, D. Komatitsch, and J. Roman, "Exploiting intensive multithreading for the efficient simulation of seismic wave propagation," in *11th International Conference on Computational Science and Engineering, Sao Paulo, Brazil, July 16-18, 2008.*

[19] R. K. S. Silva, C. A. F. D. Rose, M. S. de Aguiar, G. P. Dimuro, and A. C. R. Costa, "Hpc-ictm: a parallel model for geographic categorization," in *JVA '06: Proceedings of the IEEE John Vincent Atanasoff 2006 International Symposium on Modern Computing*. Washington, DC, USA: IEEE Computer Society, 2006, pp. 143–148.

[20] R. Iyer, H. Wang, and L. Bhuyan, "Design and analysis of static memory management policies for cc-numa multiprocessors," College Station, TX, USA, Tech. Rep., 1998.

[21] D. S. Nikolopoulos, E. Artiaga, E. Ayguadé, and J. Labarta, "Exploiting memory affinity in openmp through schedule reuse," *SIGARCH Computer Architecture News*, vol. 29, no. 5, pp. 49–55, 2001.

[22] C. P. Ribeiro and J.-F. Méhaut, "Memory affinity interface," 2008. [Online]. Available: https://gforge.inria.fr/projects/mai/

[23] BULL, "Bull - architect of an open world," 2008. [Online]. Available: http://www.bull.com/

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