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## Poster: Implications of Physical Attacks on Single Chip Motes

Sara Faour, Mališa Vučinić, Paul Mühlethaler

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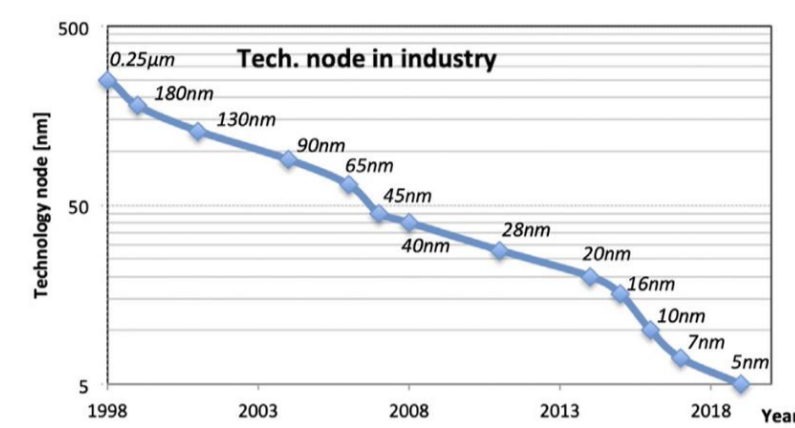
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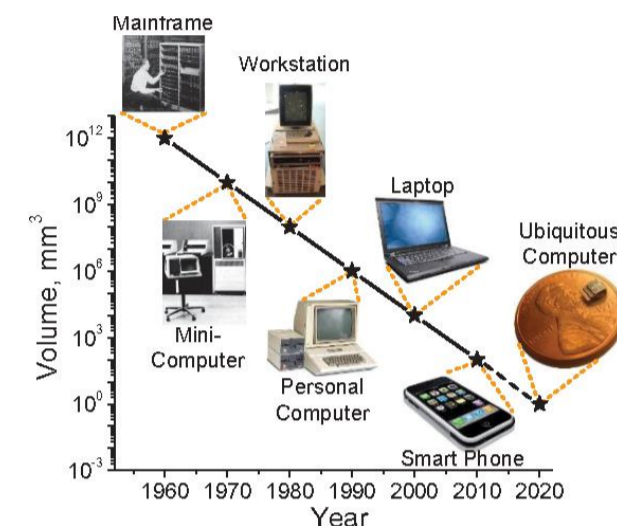
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## Background: Single Chip Motes

The advancement of the fabrication technology in the last few decades enabled decreasing the size of integrated circuits (ICs) and even eliminating the need for the assembly of individual components on a printed circuit board (PCB).



Development of technology nodes in industry (example from one factory) [1]



### 1997 - Smart Dust Vision [2]

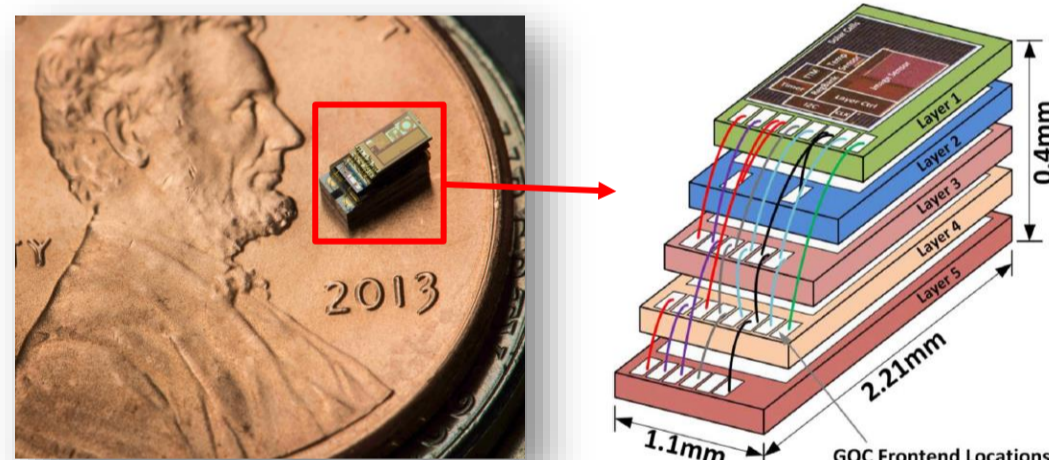
A complete system can be integrated into **1 mm<sup>3</sup>** mote !!

- Sensing
- Computation
- Communication



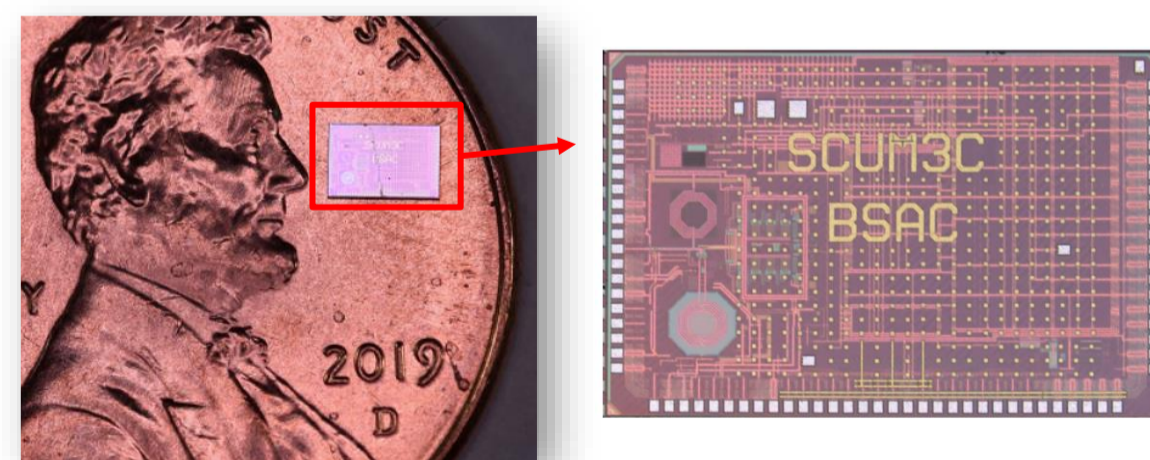
### 2012 - Michigan Micro Mote (M3) [3]

- Two ARM Cortex-M0 processors
- 3 kB retentive SRAM
- 16 kB non-retentive SRAM
- 335 kHz system clock
- Near-field radio
- Optical bootloader
- Power management
- Fabricated in three different technologies
- Includes five stacked IC dies



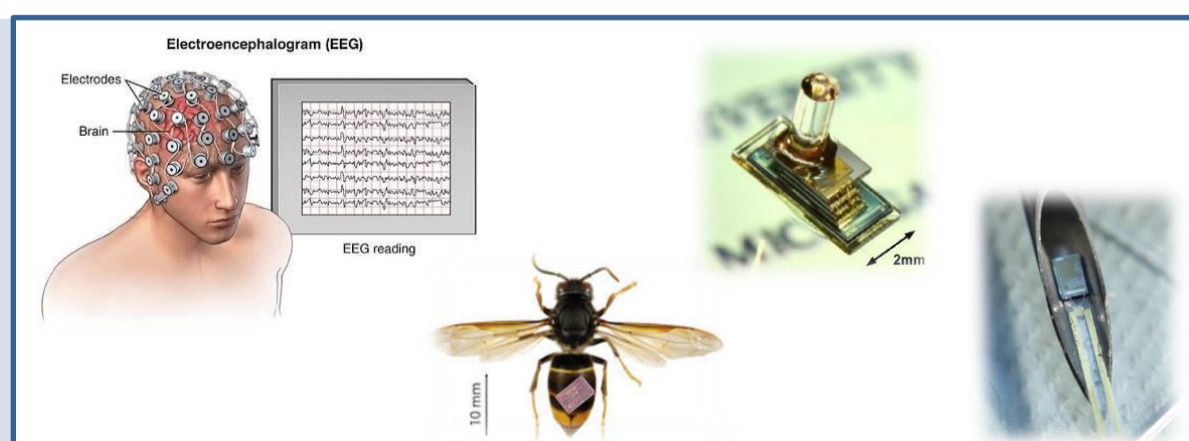
### 2019 - Single Chip micro Mote (SCμM) [4]

- ARM Cortex-M0 processor
- 64 kB each of program and data SRAM
- 20 MHz system clock
- IEEE802.15.4 and BLE compatible radio
- Optical bootloader
- Fabricated using single technology
- Single die
- External antenna and power supply (not fully integrated yet)

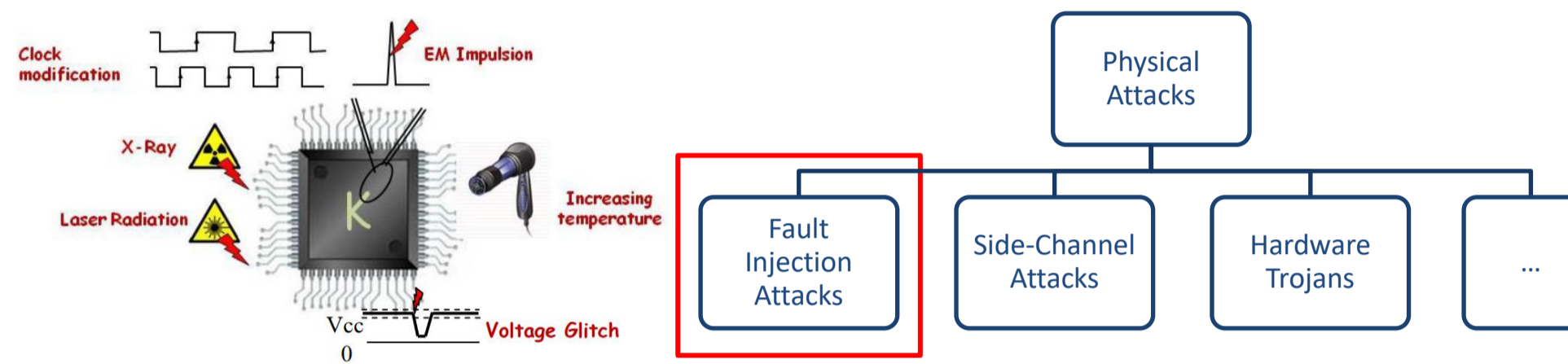


### Applications

- Wireless EEG electrodes
- Tracking insects
- Imaging system
- Injectable computer
- Actuation of microrobots

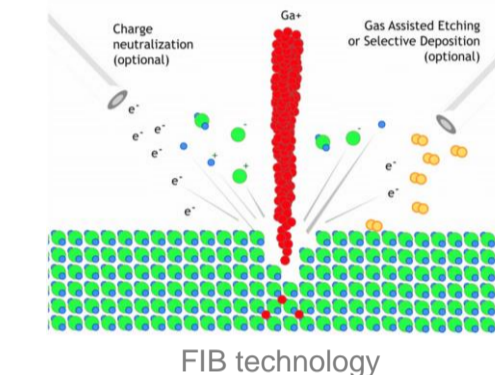


## Physical Fault Injections Attacks (FIAs)



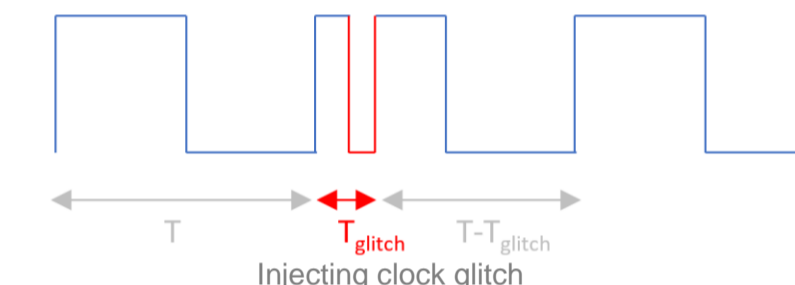
### Ion-based Fault Injection

- Two types: Focused ion beams (FIB) or heavy-ion microbeams (HIM)
- Using liquid metal ion sources (gallium, gold)
- High-resolution imaging and precision milling at the micro/nanoscale
- Very expensive (+100,000\$), but available as service for low-cost
- Invasive and destructive



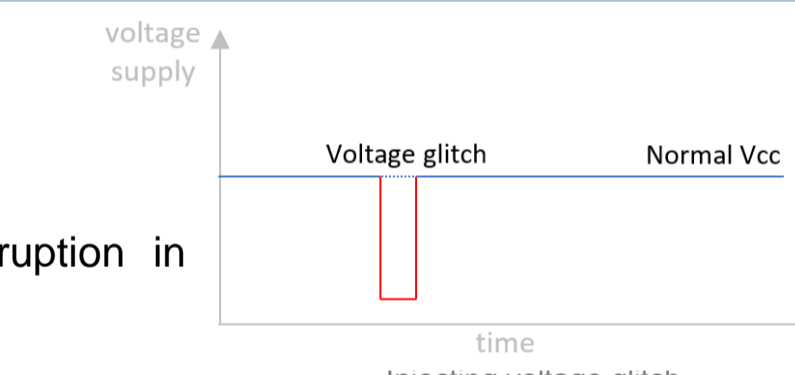
### Clock Glitching

- Manipulating the system clock signal
- Requiring access to clock line, without any special or expensive tools
- Causing instruction misses and data misreads
- Low cost and risk of damage



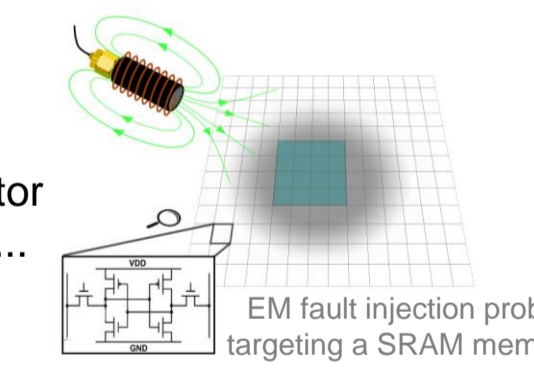
### Voltage Glitching

- Manipulating the supply voltage
- Requiring access to clock and power supply lines
- Causing delays in the setup of logic gates, corruption in memory contents, disruption in microprocessor
- Low cost and risk of damage



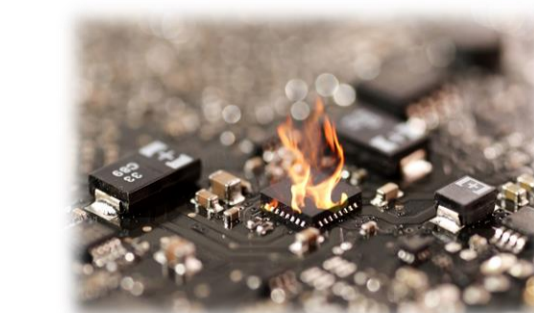
### Electromagnetic Fault Injection (EMFI)

- Injecting strong electromagnetic disturbances near the device
- Requiring near-field injection probe connected to an EM pulse generator
- Causing data perturbation in CPU registers, caches, external memory...
- Moderate cost and risk of damage



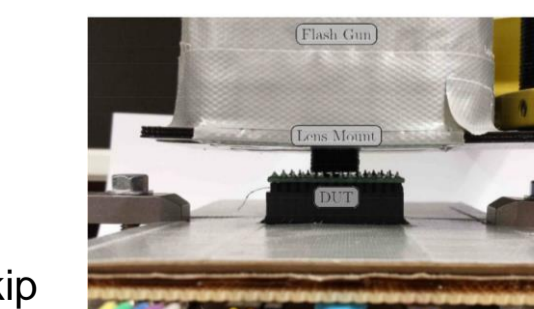
### Heating Attacks

- Altering the ambient temperature
- Can be done using a simple setup: light bulb and thermometer
- Causing bit errors in DRAM memory
- Causing read/write threshold mismatches in non-volatile memory
- Low cost and risk of damage



### Optical Fault Injection

- Exposure to high energy light source
- Requiring UV lamp or camera flash with magnification lens, laser, or nanofocused X-ray beam
- Allowing to probe and change memory content, target registers and skip instructions



## Implications of FIAs on Single Chip Motes [5]

Technique	Invasiveness	Precision (space)	Precision (time)	Technical skill	Cost
Clock glitch	non-invasive	low	high	moderate	low
Underfeeding*	non-invasive	low	high	moderate	low
Voltage spike*	non-invasive	low	high	moderate	low
EM pulse	invasive	moderate	moderate	moderate	moderate
Heat*	non-invasive	low	low	low	low
Light radiation	semi-invasive	moderate	moderate	moderate	moderate
Laser pulse	semi-invasive	high	high	high	high
Laser beam	invasive	complete	complete	complete	complete
FIB	invasive	complete	complete	complete	complete
HIM	invasive	complete	complete	complete	complete

\* Internal oscillators of single chip motes are less stable than crystal oscillators when the supply voltage or the temperature change.

Table 1: Summary of FIAs on board-based systems and single chip motes according to our work. Gray color highlights the differing criteria

✓ **Clock and voltage glitching attacks are easier to perform on PCB systems**

- **Traces scale:** To perform these attacks, we need to access the clock or the power-supply line trace. On a PCB system, these printed traces can be seen using naked eye. However, on a single chip mote, the traces are at a micro scale, since on-chip voltage regulators and internal oscillators are used.
- **Required equipment:** Accessing the traces on a PCB requires a simple equipment. However, on a single chip mote, the attacker needs to be able to create tiny channels or access points on the chip surface through which a probing wire can be attached or connected. This setup involves a much more advanced, expensive and spatially precise tool, known as FIB.

⚠ **The exposure to Electromagnetic, optical and ion-based injections have about the same level of threat regardless if the target is a single chip mote or a PCB system**

- **Fabrication process:** The process used to fabricate a chip plays an important role in making this kind of attack successful or not. The more advanced (smaller) the process is, the less the spatial resolution of the attack is, regardless if it is a PCB-based system or a single chip mote.

✗ **Single chip motes can be easily affected by any variations in the ambient temperature**

- **Temperature sensitivity:** It is one of the main characteristics of single chip motes. Any variation in the ambient temperature will affect the frequency of the internal crystal-free oscillators if no calibration algorithm is implemented. Hence, heating attacks can present a higher level of threat.
- **Risk of damage:** Board-based systems are exposed to the risk of damage in earlier stages of heating compared to single chip motes. The reason is simple: a CMOS die has a much higher maximum temperature (approx 350 °C) than PCBs.

## Ongoing Research

- Studying the implications of other physical attacks on single chip motes, including side-channel attacks and hardware trojans.
- Adopting security solutions that are more resistant to physical attacks, i.e. Physical Unclonable Functions (PUFs). Also, customizing these solutions to respect single chip mote constraints.

## References

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