A First Approach in Using Super-Steep-Subthreshold-Slope Field-Effect Transistors in Ultra-Low Power Analog Design

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Abstract. The benefits of steep-*Subthreshold Swing* (SS) devices, though plentiful at the device-level, have yet to be fully exploited at the circuit-level. This is evident from a look at the *Three-Independent-Gate Field-Effect Transistor* (TIGFET), a device renowned for its ability for polarity reconfiguration. At the same time, its demonstrated dynamic control of the subthreshold slope beyond the thermal limit has only been studied at the device-level. This latter benefit is referred to as *Super-Steep Subthreshold Slope* (S4) operation and can lead to unprecedented gain, which is ideal for use in an amplifier circuit. In this book chapter, we investigate the impact of S4 operations when designing differential-amplifier circuits while using TIGFET technology. We demonstrate the benefits of our implementation both from a theoretical standpoint and through circuit-level analyses. More specifically, we show that the TIGFET -based amplifier gain is 95.5× better, and that the gain-bandwidth product is improved by 13.8×, compared to an equivalent MOSFET-based design at the 90 nm node. Besides, we show that at equivalent gains, the TIGFET-based amplifier decreases the area and power by 22.8× and 7.2×, respectively, against its MOSFET counterpart. Further investigations prove that TIGFETs could be used in bio-sensing application where noise and power consumption are crucial. We have demonstrated that the use of TIGFETs could improve the thermal noise of low-power, *Low-Noise Amplifiers* (LNA) by 83% and the noise efficiency factor (NEF) by 58%.

Keywords: low-power analog design, Schottky barrier field-effect transistors, steep-subthreshold slope, three-independent-gate field-effect transistors

1 Introduction

The ever-increasing signal and data processing performance demand is driven by the semiconductor industry and its work in scaling down standard technologies such as the *Metal-Oxide-Semiconductor Field-Effect Transistor* (MOSFET) and its Fin-variant [1].

One way to characterize a device's performance is through its *Subthreshold Swing* (SS), which refers to the gate-to-source voltage needed to change the

drain current by one order of magnitude [2]. Based on this definition, a small SS value corresponds to a faster switching speed in the digital domain and defines a large intrinsic gain in terms of analog benefits. The minimum subthreshold swing (SS_{min}) in a MOSFET is limited to approximately 60 mV/decade at room temperature (300 K) because the carriers follow the Fermi-Dirac distribution, and their energy is bounded such that only the carriers with enough thermal energy to exceed the source-channel potential barrier will contribute to the ON-current (I_{ON}) of the device [3]. Due to this, MOSFETs are limited in their use for applications requiring fast switching, such as in signal processing applications.

A solution to this MOSFET-limited problem is the use of alternative devices which are not thermal-conduction-limited. These include tunnel FETs [3], Nano-Electro-Mechanical FETs [4], Impact-ionization MOSFETs [2], and Feedback FETs [5]. The alternative device we will consider in this study is not originally intended as a steep-subthreshold-slope device: *Three-Independent-Gate Field-Effect Transistor* (TIGFET) [6]. The TIGFET is best known for its dynamic channel reconfiguration to n- or p-type that gives it a higher expressive capability at the circuit-level than a typical transistor, enabling compact and efficient logic gates [6,7]. This device was also found to be capable of *Super-Steep-Subthreshold-Slope* (S4) operation with an SS_{min} of 3.4 mV/dec and an SS_{avg} of 6.0 mV/dec over 5 decades of current as demonstrated in [8]. This operation is enabled by an effective body biasing, which in turn is enabled by a positive feedback process based on weak impact ionization. By definition, subthreshold swing defines the gate voltage required to change the drain current by an order of magnitude.

The TIGFET and other steep-subthreshold-slope devices are optimal for use in analog circuits, as evidenced by the longstanding use of devices in their subthreshold region, with applications ranging from biological (such as in cochlear implants) [9–11] to microcontrollers [12, 13], to improved signal acquisition for ADCs applications [14–16]. Additionally, TIGFET technology can bring benefits in the context of amplifiers. In a regular *Common-Source* (CS) amplifier design, one transistor acts as a Voltage-Controlled CS while the other acts as a resistor, converting the current back to a voltage [16, 17]. The value of the subthreshold swing defines the gain of the amplifier in very low current amplifier designs. Overcoming the thermal conduction limits of regular MOSFETs for extremely low current amplifier design applications offers new horizons regarding area reduction, power consumption, and performance improvement. Operation in the subthreshold region results in low power and high gain, resulting in improved performance-to-power consumption efficiency. This is facilitated by the diffusion and tunneling-based carrier movement in the subthreshold limit.

One of the most challenging applications in analog design is biological sensing and implementable electronics. The co-integration of electronics near living tissue requires rigorous constraints on power consumption [28, 29] as thermal dissipation from the electronics can cause damage to the cells. Brain implant electronics also suffer from noise and the general expected input referred noise of the analog front-end is within $2\mu V_{RMS}$. With the performance increase of S4 devices, TIGFET devices could potentially provide new standards for *Brain-*

Computer Interface (BCI). The potential power reduction can greatly increase the number of interfaceable neurons and the noise reduction can benefit the measurement quality.

In this book chapter, we extend our previous work [32] and introduce an amplifier design using TIGFET devices operating in S4 mode and highlight their benefits compared to standard MOSFET transistors. We study the advantages of our implementation both from a theoretical perspective and through circuit-level analyses. In particular, we demonstrate a 95.5× improved gain and a 13.8× higher *Gain-Bandwidth Product* (GBP) for our TIGFET design, compared to an equivalent MOSFET-based design using a 90 nm technology node. Additionally, we show that at equivalent gains, the TIGFET-based amplifier decreases the area and power by 22.8× and 7.2×, respectively, against its MOSFET counterpart. We also show how the use of TIGFET devices in biological sensing applications could improve *the Noise Efficiency Figure* (NEF) by 58% and input referred noise by 83% for the input recording amplifiers.

The remainder of this chapter is as follows: Section 2 reviews various SS devices and TIGFET technology. Section 3 introduces our proposed TIGFET-based amplifier circuit and provides theoretical gain and bandwidth analyses. Section 4 presents our circuit-level experimental results. Section 5 presents the noise and performance analysis of a typical bio-sensing TIGFET-based amplifier. Finally, Section 6 concludes this chapter.

2 Technical Background

In this section, we introduce the necessary background behind sub-60 mV/decade technology, including TIGFET technology and its operations.

2.1 Steep-Subtreshold Devices

Multiple devices have been proposed as candidates to replace MOSFETs with an ability for sub-60 mV/decade SS operation. These include the tunnel FET that has been fabricated with OFF-current down to the pA/μm scale and a small *SS* of 52.8 mV/dec [3]. These benefits are mostly neutralized by the low ON-current of approximately 50 μA/μm exhibited by TFETs fabricated with large band-gap semiconductors such as silicon; the massive loss in current drive makes this device practically unusable for standard designs. Note that the TFET results in an onset strength (ON-OFF current ratio) that is almost the same as that of a conventional MOSFET. Another alternative device capable of steep-substhreshold characteristics is the Nano-Electro-Mechanical FET [4]. This device is limited in operation and device reliability by the mechanical gate with which it realizes its abrupt SS. Besides, impact-ionization MOSFETs are devices that have been shown to achieve less than 5 mV/dec *SS* and high ON-state currents through avalanche breakdown, but constantly being operated using this mechanism leads to reliability issues at the device-level [2]. The Feedback FET has similar benefits to the impact-ionization MOS device, but it is not CMOS-compatible, requires

initial programming to set the device states, and suffers from reliability problems [2, 3, 5].

2.2 The TIGFET as a Standalone Device

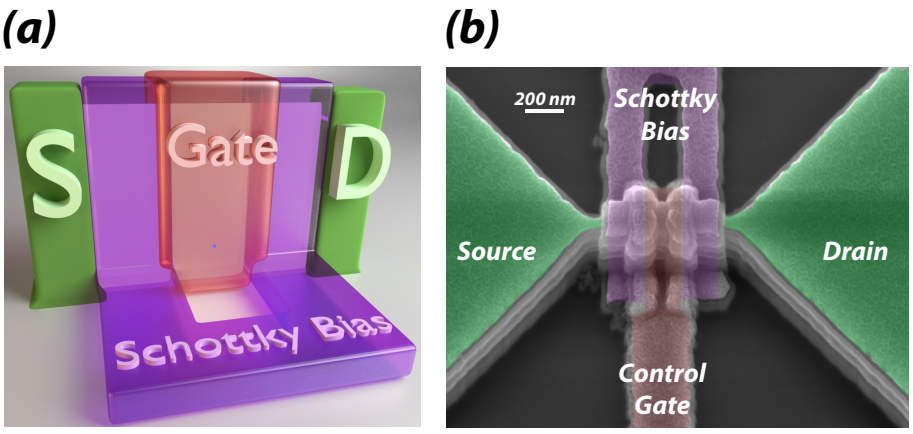


Fig. 1: Schottky-barrier FET: (a) general structure; (b) SEM image of a fabricated fin-based device [8].

Fig. 1 (a) depicts the general structrue of a Schottky-barrier FET. Such device requires a channel made of a semiconductor material, metallic source and drain contacts, and a minimum of two independent gate electrodes: the *Control Gate* (CG) and a polarity gate at the drain (PG_D) to act as electrostatic doping means at the Schottky barrier interfaces [19, 20]. Fig. 1 (b) depicts a *Scanning Electron Microscopy* (SEM) of a fabricated fin-based Schottky-barrier device [8]. The TIGFET is an enhanced Schottky-barrier FET with a CG and two independent polarity gates: one added at the source (PG_S) and another at the drain (PG_D) [19]. The control gate controls whether the device is ON or OFF. The polarity gate at the drain induces a band-bending opposite to the source band-bending, suppressing the reverse junction leakage. This allows for device reconfigurability between n-type and p-type behaviors after fabrication. Besides, much lower leakage floor values can be reached due to the Schottky-barrier cutoff provided by the individually-gated nanojunctions. The dominant carrier is chosen by the potential on the polarity gate [20]: if the PGs are increased to the supply voltage (V_{DD}), the device will be n-type (electron) carrier-dominated, whereas if the PGs are grounded (0 V), the device will be p-type (hole) carrier-dominated.

Besides its ability for polarity reconfiguration, TIGFETs have demonstrated two additional operation modes: the dynamic control of the threshold voltage [6]

and the dynamic control of the subthreshold slope beyond the thermal limit [8]. The latter makes the TIGFET uniquely suited for amplifier applications. This effect, referred to as S4 operation, is enabled by an effective body biasing that is permitted by a positive feedback process based on weak impact ionization.

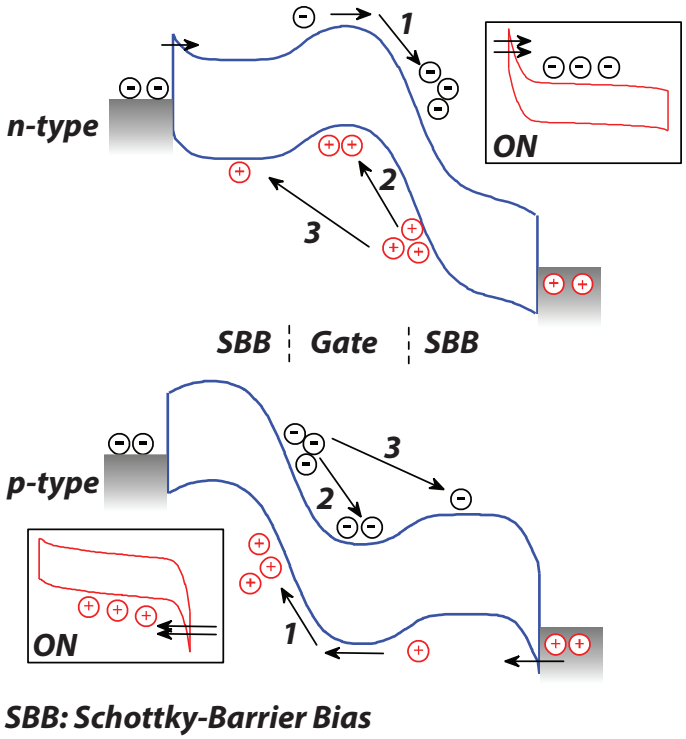


Fig. 2: Energy band diagrams of the TIGFET being operated in steep-subthreshold-slope during the transition from OFF to ON. The inset diagrams show that impact ionization and potential wells vanish when the device is ON [8].

When the device is biased in the subthreshold region, the electrons diffuse from source to drain, and the resulting impact ionization causes the holes to be collected at the potential minimum in the body, thus raising the body potential (V_{BS}) and enhancing the electron supply from the source. This body biasing causes the electron concentration and therefore current in the channel to be much higher than would otherwise be possible in a conventional MOSFET. The increase in I_{DS} and more impact ionization initiates a positive feedback, resulting in an abrupt increase in subthreshold current [2,5]. Fig. 2 shows a TIGFET being operated in this steep-subthreshold mode. The benefits reaped are substantial, as seen in the TIGFET device demonstrated in [8]: SS_{min} of 3.4 mV/dec, SS_{avg}

of 6.0 mV/dec over 5 decades of current, an onset strength of 10^7, and an OFF-current of 0.06 pA/μm.

3 Proposed TIGFET Differential Amplifier

In this section, we start by introducing the differential amplifier based on MOSFET and TIGFET devices. We then provide a theoretical comparison of the gain of MOSFET and TIGFET devices. This serves as the backbone for our simulation work.

3.1 The Differential Amplifier

The differential pair is the most widely used structure in analog design [16, 17], as it is the input stage of every operational amplifier. The two main reasons for the widespread use of differential amplifiers are that they mitigate interference and do not require bypass or coupling capacitors when biasing the amplifier or coupling amplifier stages together. The performance of the differential pair depends on the matching between the two sides of the circuit. Fig. 3 (a) shows a basic MOSFET-based differential pair.

V_G and V_{CM} are the biasing voltages; their values set the operating point of our amplifier and define the transconductance of the transistors. I_{tail} defines the DC current going through the transistors and thus also defines the transconductance. I_{tail} is chosen to set the transistor in the subthreshold region so that I_{DS} is at approximately 20 nA while V_G is set by a Widlar current source [16, 17].

3.2 The TIGFET-based Differential Amplifier

As explained in Section 2.2, connecting the polarity gates to V_{DD} configures the top TIGFETs as n-types, while connecting the polarity gates to GND configures the bottom devices as p-types. As such, the MOSFET amplifier shown in Fig. 3 (a) can be designed with TIGFET devices, as illustrated in Fig. 3 (b). V_G, V_{CM}, and I_{tail} are the same biasing sources as in Fig. 3 (a) and have the same impact on the amplifier performance. However, since the TIGFET operates at a much higher V_{DS}, the current I_{DS} is lowered to 5 nA to keep the power consumption equal to the standard MOSFET amplifier. While both MOSFET and TIGFET amplifiers employ the same schematic, significant gain improvements are expected by using TIGFET device due to their S4 behavior.

3.3 Theoretical Equations

In this section, we provide theoretical equations for both MOSFET and TIGFET cases. When considering a 90 nm MOSFET technology with a biasing point of 0.6 V for V_{DS} and 20 nA, discussed in Section 3.1, the resistance r_0 is defined as [16, 17]:

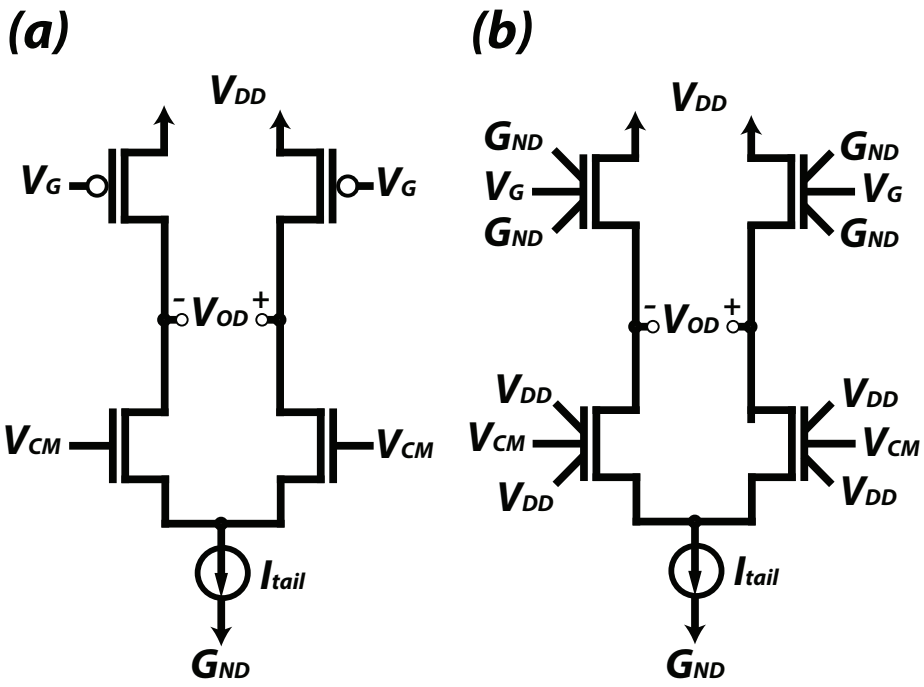


Fig. 3: Transistor-level schematic of a differential pair using: (a) standard MOSFETs; (b) TIGFETs.

$$r_{0-CMOS} = \frac{V_{DS}}{I_{DS}} = \frac{0.6V}{20nA} = 30M\Omega$$

The 90 nm CMOS device has a slope of 80 mV/dec around this previous biasing point. Using the definition of SS, we calculate the transconductance by picking an order of magnitude of I_{DS} around its operation point of 20 nA. This gives us a transconductance of:

$$g_{m-CMOS} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{40nA - 4nA}{80mV} = 0.45\mu S$$

Thus, the gain of the differential pair is given by:

$$A_{V-CMOS} = g_{m-CMOS} \cdot R_{0-CMOS}$$

$$\implies A_{V-CMOS} = g_{m-CMOS} \cdot (r_{0-CMOS} // r_{0-CMOS})$$

$$\implies A_{V-CMOS} = 0.45\mu S \cdot 15M\Omega = 6.75V/V$$

Based on the fabricated devices of [6], for the TIGFET operating in S4, the hero device operates at a V_{DS} of 5 V and with an I_{DS} current of 5 nA:

$$r_{0-TIG} = \frac{V_{DS}}{I_{DS}} = \frac{5V}{5nA} = 1000M\Omega$$

The transconductance g_m of the TIGFET is derived using the same approach as for the CMOS; we pick an order of magnitude of current around the biasing point and use the SS definition:

$$g_{m-TIG} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{10nA - 1nA}{3.4mV} = 2.647\mu S$$

Similarly, the gain A_V of the amplifier is:

$$\begin{aligned} A_{V-TIG} &= g_{m-TIG} \cdot R_{0-TIG} \\ \implies A_{V-TIG} &= g_{m-TIG} \cdot (r_{0-TIG} // r_{0-TIG}) \\ \implies A_{V-TIG} &= 2.647\mu S \cdot 500M\Omega = 1323V/V \end{aligned}$$

The TIGFET exhibits a 196× higher theoretical gain than its MOSFET counterpart, which is particularly appealing for amplifier designs. This improved gain will be verified in the experimental results section.

4 Experimental Results

In this section, we demonstrate the benefits of using an S4-TIGFET device when designing a differential amplifier. First, we describe our experimental methodology, and then we compare this proposed design to a conventional MOSFET implementation using a commercial 90 nm technology.

4.1 Experimental Methodology

To compare the different amplifier designs, we employ a commercial 90 nm technology node for the MOSFET case. For the TIGFET devices, we consider 100 nm gate transistors based on fabricated devices from [8]. We study the performances of differential amplifiers using minimum-sized MOSFET and TIGFET devices through electrical simulations. Besides, both circuits are biased in the subthreshold region with the same power consumption [18]. TIGFETs are modeled using small-signal models of *n-type* and *p-type* transistors, as shown in Fig. 4. DC characteristics such as the transconductance (gm) and intrinsic capacitances are extracted from [8]. Note that the S4 behavior was demonstrated for both *n-type* and *p-type* [8]. As this small-signal model is originally meant to describe MOSFETs, the three TIGFET gate capacitances are assumed to be equivalent as a large single one. The goal of our paper being to showcase a new application for TIGFET technology thanks to their S4 behavior, we believe that this still provides a first good approximation for our study. This model provides accurate performance analysis for small signal AC operations. Large-signal information has not been included for distortion analysis. In a second study, we compare the area and power of both designs while achieving the same gain.

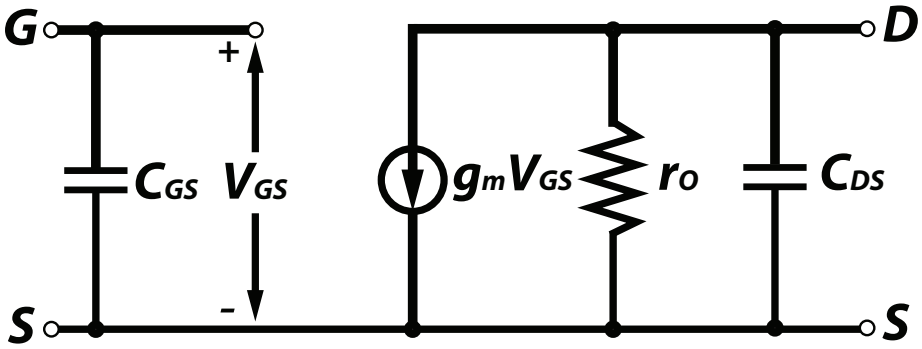


Fig. 4: Small signal model of a TIGFET device.

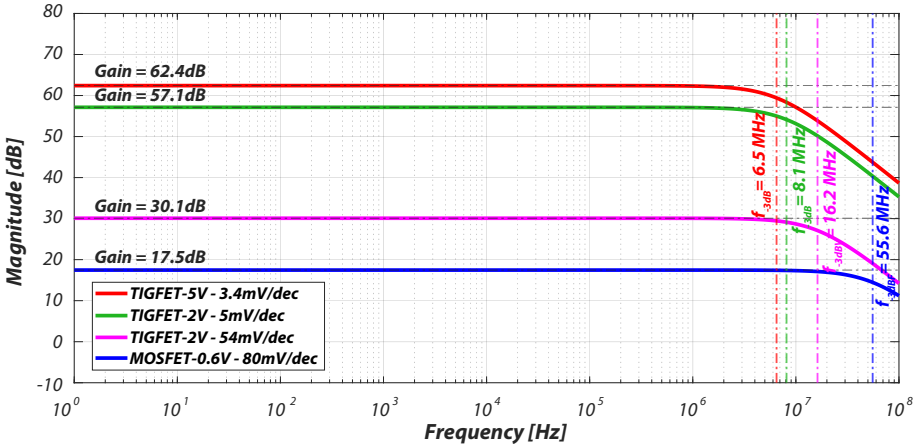


Fig. 5: Frequency responses for differential pairs, considering a 90 nm MOSFET case and different 100 nm TIGFET configurations.

4.2 Frequency and Gain Comparison for Minimum Sized Devices

Fig. 5 shows the magnitude responses of differential pairs using conventional MOSFET devices and using TIGFET devices under different configurations. The first TIGFET configuration (*TIGFET-5V-3.4mV/dec*) we studied uses the experimental hero device TIGFET S4 value reported in [19]. This configuration is not easily comparable to the others due to the large V_{DS} biasing voltage of 5 V; this would not be fair as the amplifier would require a V_{DD} of 10 V. However, it results in the best performance due to having an SS_{min} of 3.4 mV/dec. The voltage gain and bandwidth are 62.4 dB, and 6.5 MHz, respectively, as shown in the red plot in Fig. 5. The low bandwidth is a result of the low current used in the design. The second TIGFET configuration (*TIGFET-2V-5mV/dec*) uses the hero TCAD-predicted device characteristics and biases the device with

$V_{DS} = 2\ V$ and reaches 5 mV/dec of subthreshold slope [8]. As V_{DD} is reduced, the amplifier can be powered with 5 V. As expected, the gain suffered from the 5 mV/dec slope and is only 57.1 dB, though the current can be increased to match the power consumption of the *TIGFET-5V-3.4mV/dec* case while achieving a 8.1 MHz bandwidth. The last TIGFET configuration studied (*TIGFET-2V-54mV/dec*) uses the lower-performance S4 device from [19] with a measured SS of 54 mV/dec. As shown in Fig. 5, the gain is decreased to 30.1 dB. In comparison, the MOSFET (*MOSFET-0.6V-80mV/dec*) suffers in performance due to its thermally-limited SS and only achieves a gain of 17.5 dB. MOSFETs can, however, operate at 1.2 V with higher current and achieve better bandwidth than the TIGFET cases (55.6 MHz). Table 1 summarizes the results of all four cases.

Table 1: Performance results for MOSFET- and TIGFET-based amplifiers.

	Gain (V/V)	**Bandwidth** (MHz)	**GBP** (GHz)
MOSFET-0.6V-80mV/dec	7.5	55.6	0.42
TIGFET-5V-3.4mV/dec	1318.3	6.5	8.57
TIGFET-2V-54mV/dec	32.0	16.2	0.52
TIGFET-2V-5mV/dec	716.1	8.1	5.80
Comparison*	**+95.5**×	−6.9×	**+13.8**×

* When comparing the *TIGFET-2V-5mV/dec* case against the *MOSFET-0.6V-80mV/dec* case.

The *TIGFET-2V-5mV/dec* results in a 95.5× better gain and a 13.8× higher GBP than the MOSFET case. Besides, even the worst TIGFET case (*TIGFET-2V-54mV/dec*) still achieves a larger gain when biased in the subthreshold than its MOSFET counterpart.

4.3 Area and Power Comparisons

Our second study aims at comparing the area of a TIGFET-based amplifier and a MOSFET-based amplifier of the same performance [16,21]. TIGFET devices are generally larger than MOSFET devices at the same node due to their additional polarity gates. However, to get the same gain from the MOSFET amplifier, a cascoded version of the differential pair shown in Fig.6 must be used, and requires additional transistors [16, 17, 22].

This architecture keeps the power consumption low using only 2 branches, similar to the original amplifier in Fig. 3. However, the extra added common-gate transistors are required to increase the gain of the MOSFET-based amplifier to 57 dB to match the TIGFET performance. Both MOSFET- and TIGFET-based amplifiers are shown in Fig. 7 (a) and (b), respectively. For a fair comparison, the

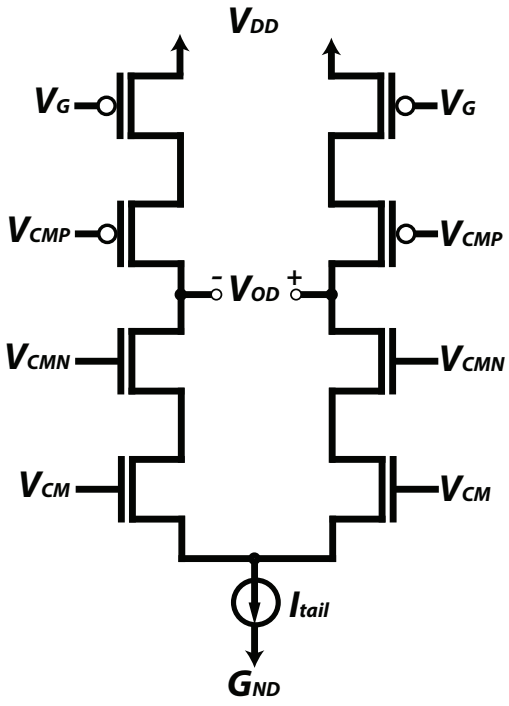


Fig. 6: Schematic of a MOSFET-based cascoded differential pair.

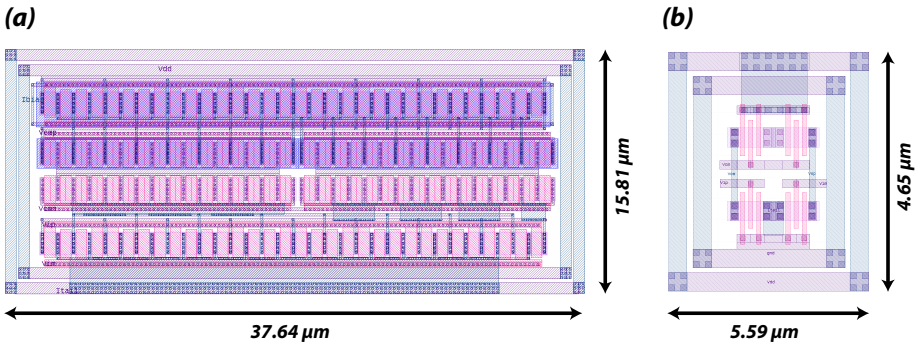


Fig. 7: Layouts of differential amplifiers achieving a same gain of 57 dB: (a) MOSFET-based; (b) TIGFET-based.

TIGFET amplifier layout is drawn from fully-custom TIGFETs designed using a commercial 90 nm *Process Design Kit* (PDK) and both designs were verified using the same *Design Rule Check* (DRC) rules. The MOSFET-based amplifier has a total area of 595.36 μm^2. In comparison, the TIGFET-based amplifier area

is 26.04 μm^2, a 22.8× reduction compared to the MOSFET case, as shown in Table 2.

Table 2: Performance results of MOSFET- and TIGFET-based amplifiers, at the same gain of 57 dB.

	90 nm MOSFET	**100 nm TIGFET**	**TIGFET Benefits**
Area (μm^2)	595.36	26.04	**-22.8**×
Power (nW)	360	50	**-7.2**×

The significant area reduction is due to the TIGFET S4 intrinsic gain being significantly higher compared to a conventional MOSFET gain, as explained in Section 2. As a result, the TIGFET devices do not need to employ larger sizes to reach a gain of 57 dB, as in the MOSFET case. Besides, the TIGFET-based amplifier reduces the power consumption by 7.2× compared to the MOSFET implementation. This is because the TIGFET implementation employs smaller devices while achieving the same performance than its MOSFET counterpart.

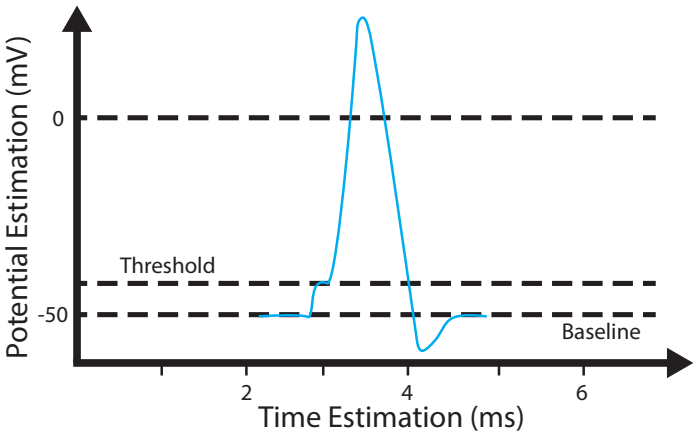
5 The Benefits of TIGFETs in Biosensing Applications

In this section, we first introduce the concept of bio-sensing and typical design constraints. We then compare a typical CMOS amplifier for bio-sensing applications with its TIGFET-based counterpart and conclude about the potential of TIGFETs for such bio-sensing applications.

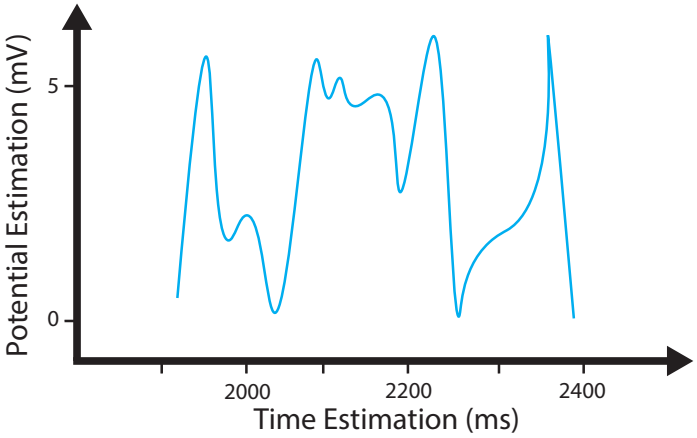
5.1 Brain Computer Interfaces Requirements

Neuronal activity can be recorded *in-vivo* through an implanted neural electrode array. The useful information from such electrodes typically consists of two different types of signals, as shown in Fig. 8. The first and most common type is the *Extracellular Neural Action Potential* (ENAP), referred to as spikes and shown in Fig. 8a. Spikes are "short" and biphasic pulses that typically last between $100\mu s$ and $1ms$ with peak amplitude of tens of μV to tens of mV. They are the results of firing a neuron in the region near the electrode and the signal of interest is within $500 - 5,000Hz$. The second type of signal is called a *Local Field Potential* (LFP), shown in Fig. 8b which is a very slow oscillation of $< 200Hz$ up to $5mV$ peak amplitude. This signal is the result of many neurons firing in the same large area and affects the "DC" potential of this wide area of tissue. Typically, state-of-the-art bio-sensing ASICs dedicate fewer channels to record LFPs while most of the channels record neuron spikes. LFP recording channels require a $0.1 - 250Hz$ bandwidth and ENAP recording channels require a $300 - 10,000Hz$ bandwidth. Recording high quality signals typically

constrains the input referred noise, and commercial state-of-the-art ASICs limit the maximum input referred noise on the analog front-end to $< 3\mu V_{rms}$, with a 10kHz bandwidth and a 12bits resolution ADC. In a nutshell, brain machine interfaces are low-frequency monitoring system with rigid requirements on noise.



(a) Typical signal from a neuron firing close to an electrode.



(b) Typical low frequency signal from the field potential induced by the firing of surrounding neurons.

Fig. 8: Typical signals recorded from bio-sensing electronics: a) High-frequency spikes; b)Low-frequency LFP.

We have introduced the recording requirements of the BCIs and their expected performance in term of bandwidth and input referred noise. These BCIs are also subject to very challenging constraints regarding thermal dissipation, and thus power consumption. All BCI devices require either continuous or tran-

sient transcutaneous power delivery, and this power dissipates as heat or radiates as electromagnetic radiation. As the implanted device is recording or stimulating, it is dissipating heat into the tissue; the magnitude of this temperature difference is critically important to the safety of the surrounding cells. The recommended specific absorption rate (SAR) for human tissue is 1.6 W/kg for radiation in the 3 kHz to 300 GHz spectrum [28]. The standard limits of a 2°C temperature increase, of 40 mW/cm^2 heat flux are valid for most tissues in the body and is reasonable targeted thermal power dissipation value for BCI [29].

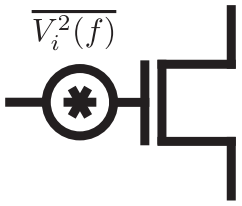


Fig. 9: Simplified noise model for low and moderate operation frequencies of the MOSFET.

As discussed previously, BCI are low-frequency acquisition systems ($< 10kHz$) that have strict constraints on power consumption and input referred noise. In order to understand why the TIGFETs could benefit such applications, it is worth mentioning how noise in a MOSFET is determined. For low and moderate frequencies, which is the case for a $10kHz$ low-noise amplifier for conditioning the neuron activity, the simplified noise model of the MOSFET shown in Fig. 9 can be used, assuming a large channel device [16] with:

$$\overline{V_i^2(f)} = 4kT(\frac{2}{3})\frac{1}{g_m} + \frac{K}{WLC_{ox}f}$$

The term $4kT(\frac{2}{3})\frac{1}{g_m}$ is the thermal noise of the device and $\frac{K}{WLC_{ox}f}$ is the flicker noise or 1/f noise. The thermal noise is purely dependant on the transconductance g_m of the device while the flicker noise is inversely proportional with the size of the device; this means that a larger device will have a smaller flicker noise, thus we can use the large channel approximation. K is a process dependent factor and widely varies for different devices in the same process. For low frequency applications, the flicker noise tends to be more of a concern and designers tend to increase the size of the input stage as much as is reasonable in order to keep the input referred noise low. However, some BCI [23] have shown that thermal and inband noise actually dominates the total input referred noise to almost 50%. To cover this issue, it is possible to increase the transconductance of the input device, at the expense of increased power consumption since $gm = \frac{I_d}{n \cdot V_t}$ (in subthreshold), which is not compatible with BCI applications because of the thermal dissipation requirements. Another solution is to use different semiconductors to overcome this device limitation. Section 3.3 shows that

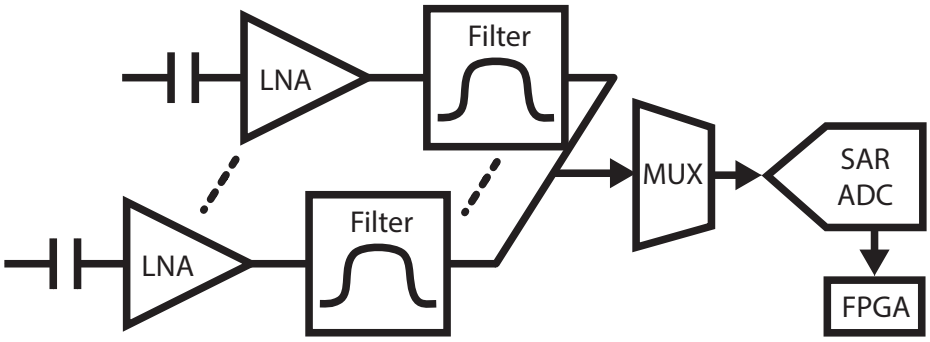


Fig. 10: Typical block diagram of a multi-channel, integrated brain-computer interface.

the TIGFET transconductance is equal to $2.64\mu S$ compared to the $0.45\mu S$ of the regular CMOS, for the same low biasing current. Thermal noise would be reduced by approximately $5\times$ and would greatly benefit any kind of low-power LNA in a brain-computer interface circuit. This increase in g_m is, generally, very interesting for any kind of low-power, low-noise application [32].

5.2 Typical Analog Front-end for Neuronal Recording

Fig. 10 presents an example of the high-level architecture for a typical brain computer interface. The electrodes connected to the neurons are interfaced by single channels in parallel through a line capacitor to filter DC signal and allow the spikes to pass through [23, 27, 31]. The low-noise amplifier is the first stage which interfaces the signals and great care must be taken in its design. This first stage must be designed to keep the input referred noise down to $2\mu V$. Signals are then filtered to detect either the spikes or the low-frequency LFP. Most BCI [23, 30] then use a multiplexer to digitize an array of channels. The output is processed by a controller and sent to an FPGA or μ-controller through low-power wireless communication. The LNA is the first stage of the acquisition front-end and its noise performance affects the overall acquisition system performance. Since the main trade-off in designing a BCI is between noise and power dissipation, we often use the noise efficiency factor (NEF) [24] or power efficiency factor to estimate the ability of a design to get a certain level of noise for a given power consumption.

NEF is defined as:

$$NEF = V_{ni,rms}\sqrt{\frac{2 \cdot I_{tot}}{\pi U_T 4kT \cdot BW}}$$

where I_{tot} is the current used by the low-noise amplifier, BW is the $-3dB$ bandwidth of the pass-band filter, and $V_{ni,rms}$ is the input referred noise of the amplifier.

Based on state-of-the-art literature, the current-reuse low-noise amplifier topology is the best-in-class for having the lowest NEF [25].

A typical first-stage current reuse topology [26] is shown in Fig. 11. As this topology is well-known for being very efficient in terms of NEF, we will discuss its noise performance, its power consumption, and its NEF equation. We will also provide some insights on how a TIGFET-based current reuse compares to a standard MOSFET in the next Section. [26] shows that the input referred noise of a single-ended current reuse topology is half the power of a regular single-ended differential pair (when $g_{mn} = g_{mp}$):

$$\overline{V_{in,n}^2} = \frac{8kT}{3(g_{mn} + g_{mp})}$$

The output current noise [26] of the circuit shown in Fig. 11 is defined by:

$$\overline{i_{o,noise}^2} = \frac{16kT}{3} \cdot (g_{mn} + g_{mp})$$

This value is valid for any type of device used in the design. The input referred thermal noise can then be determined by dividing the output current noise by the gain of the first-stage. This leads to:

$$\overline{V_{in,therm}^2} = \frac{\overline{V_{out,therm}^2}}{A_v^2} = \frac{\overline{i_{o,noise}^2} \cdot R_o^2}{(g_{mn} + g_{mp})^2 \cdot R_o^2}$$

$$\overline{V_{in,therm}^2} = \frac{16kT}{3(g_{mn} + g_{mp})}$$

5.3 Comparison Results

Using the previous equations for the NEF and the input referred thermal noise, and the performance of the TIGFET from Section 3.3 and Section 4, we can estimate the TIGFET noise level relatively to the MOSFET topology in Fig. 11. The input referred thermal noise of the current reuse stage is a function of the transconductance of the devices and we can derive the thermal noise improvement using the derived transconductance of the device from Section 3.3.

$$100 \cdot \frac{\overline{V_{in,therm-TIG}^2} - \overline{V_{in,therm-CMOS}^2}}{\overline{V_{in,therm-CMOS}^2}} = 100 \cdot \frac{g_{m-TIG} - g_{m-CMOS}}{g_{m-CMOS}} = -83\%$$

Considering the TIGFET g_m of $2.64\mu S$ and the CMOS g_m of $0.45\mu S$ leads to a calculated reduction of 83% in input referred thermal noise which is linearly linked to the improvement in transconductance of the device.

The NEF comparison is more complex because it is both a function of the current consumption and the input referred noise. We can either suppose: 1) two LNAs with the same power consumption but different input referred noise which

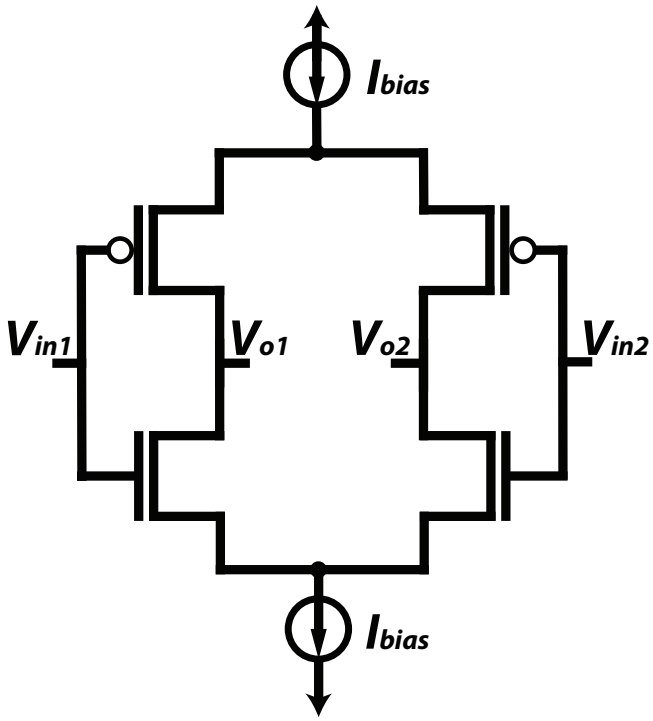


Fig. 11: Typical current-reuse input stage for the LNA.

also leads to a -83% improvement since the NEF linearly depends of noise, or: 2) having two LNAs with the same input noise and compare their power consumption. Since $g_m = \frac{I_d}{n \cdot V_t}$ is a function of I_d, the CMOS LNA's supply current must be $\frac{g_{m-TIG}}{g_{m-CMOS}} = 5.8\times$ bigger for having the same input referred noise. This leads to an increase in NEF of:

$$100 \cdot \frac{NEF_{TIG} - NEF_{CMOS}}{NEF_{CMOS}} = \frac{\sqrt{2 \cdot I_{tot-TIG}} - \sqrt{2 \cdot I_{tot-CMOS}}}{\sqrt{2 \cdot I_{tot-CMOS}}}$$

$$= 100 \cdot \sqrt{\frac{1}{5.8}} - 1 = -58\%$$

This comparison in NEF and input referred noise does not take the flicker noise into account but it is worth discussing flicker noise in more depth. Flicker noise in a MOSFET is defined as:

$$\overline{V_i^2(f)} = \frac{K}{WLC_{ox}f}$$

Flicker noise is inversely proportional to the device size and BCI interfaces use extremely large devices to mitigate the effect of flicker noise. Flicker noise is also

decreased by using low currents which is the case in BCI interfaces with thermal limitations. While it may be obvious that, for low-frequencies applications, flicker noise is the dominant source of noise, post-silicon experimental results have often shown that flicker noise is not significant in this application [23, 27]. [27] shows that in their design, flicker noise contributes to $0.1\mu V_{rms}$ of the total $2.2\mu V_{rms}$, a contribution of only 4.5%. For this purpose, this study did not include the effect of flicker noise on BCI.

It is also complex to compare the flicker noise of a CMOS device and a new emerging device because of different K constant terms that depend on how the devices are fabricated. An emerging device is most likely to suffer from a bad K because of the lack of maturity in the device. A TIGFET's *Super-Steep-Subthreshold-Slope* abilities rely on a positive feedback during impact ionization and this effect can influence the noise of the device. It is therefore important to mitigate the noise improvements that TIGFETs ideally show, as it is more likely to be higher that what we derived in this chapter.

6 Conclusion

In this book chapter, we have shown the benefits of S4 devices at a circuit level. While MOSFET devices are limited by their SS of 60 mV/dec, the TIGFET shows SS as low as 3.4 mV/dec. TIGFET-based amplifiers show great performance when biased in their subthreshold region, where they can benefit from their steep slope and high gain. In particular, we showed that a regular differential-pair using TIGFET devices improved the gain by 95.5× and increased the GBP by 13.8×. Besides, we showed that porting the same-performance MOSFET-based amplifier to TIGFET devices reduced the area and power by 22.8× and 7.2×, respectively. This demonstrates that TIGFETs are great devices for high-performance analog applications, where power consumption and cost are crucial. Additionally, this work paves new paths in the extremely low-power and low-noise analog domain for S4-devices in general, and TIGFETs in particular, with an 83% reduction in input referred noise and a 53% expected improvement in NEF.

Acknowledgments

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