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An Energy-Efficient Wideband Input-Buffer for High-Speed CMOS ADCs

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Abstract. Input buffers (IBs) for driving analog-to-digital converters (ADCs) in direct down-conversion radio frontends are normally operated with supply voltages higher than the nominal, mainly due to bandwidth (BW) and dynamic linearity constraints. Therefore, several voltage-regulators are required as well as the need of having I/O devices capable of handling such voltages. An energy-efficient input buffer architecture is presented in this paper and fairly compared to other existing IB realizations using a standard 1.2-V 130-nm CMOS technology as reference. The proposed new architecture presents better dynamic performance, and it can be readily used to drive moderate-resolution ADCs without requiring either a higher supply voltage or any non-standard I/O devices.

Keywords: ADC, Input Buffer, CMOS, High Linearity, High Bandwidth, Direct Conversion, Harmonic Distortion, Intermodulation Distortion.

1 Introduction

Moderate resolution ADCs (10-to-12 bits) with sampling-rates of several GHz (1-to-8 GHz) and dissipating low power are in high demand for the next generation of communication systems. In fact, the input bandwidths (BW) requirements of the ADCs have continuously increased allowing down-convert signals directly from radiofrequency (RF) multi-GHz bands. This is a common practice to either reduce or eliminate the need for analog mixers and complex filters. For 5G receivers, for instance, ADCs with resolutions of 10-bit and sampling speeds in the range of 1–2 GHz are often employed [1].

With faster ADCs, these operations can move forward, into the digital domain, and carried out in software. Therefore, in modern radio-receiver systems, the ADC is closer to the antenna. As a result, the required input signal BW of the sample-and-hold (S/H) circuit in the frontend of the ADC cannot be directly and efficiently driven by the low-noise amplifier (LNA) without rising significantly the power dissipation of the whole receiving chain. Therefore, as it is shown in Fig. **1**, a high-performance voltage input-buffer (IB) should be added between the wideband LNA and the ADC to properly interface these two main building-blocks. Due to the fast sampling-rate (*Fs*) of the ADC a relatively short time (a few hundreds of picoseconds) is available for input signal

tracking. During this window, the ADC driver must fully charge the large sampling capacitor with low noise and distortion.

In order to not degrade the overall dynamic performance of the entire receiving chain, the IB must reach excellent dynamic performance in terms of BW, linearity, and energy-efficiency. Consequently, the design of these (IBs) guarantee that the dynamic specifications of the ADC are not significantly degraded. Due to this reason, most of the existing solutions for these IBs require supply voltages higher than the nominal (core supply) values of the technology and, consequently, additional voltage regulators.

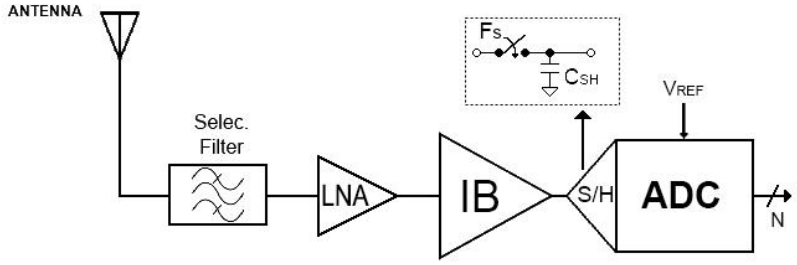

Fig. 1. Direct-conversion receiver system.

In this paper, a novel wideband IB architecture is proposed. When compared with other existing solutions and using the same comparison conditions, our architecture presents an extended BW, better dynamic performance and higher energy-efficiency, and it can be readily used to drive moderate-resolution ADCs without requiring either a higher supply voltage or any non-standard I/O devices

2 State of the Art of Input Buffer Architectures

2.1 The Source-Follower (SF) and Cascade SF

Due to its simplicity, the source-follower (SF), shown in Fig. 2(a), is the first design option for voltage buffers. The output voltage extracted on the source of a common-drain (CD) device (M1) is almost a perfect copy of its gate voltage if body-effect is eliminated [2]. Therefore, and despite the simplicity, the voltage buffer is an effective solution when nominal power-supply is not a major concern.

This design has, however, a few limitations that have been analyzed and optimized, over the years, in the literature. Limitations in the non-zero output resistance have been studied in [2-4]. Linearity issues with this design were studied in [5], as well as studies to overcome the level-shifting and offset at the output [3].

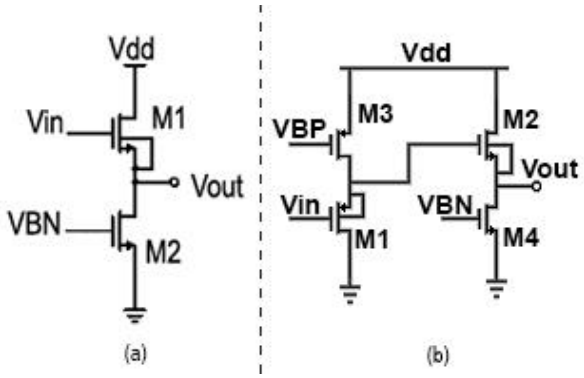

Fig. 2. (a) Source-follower, SF; (b) Cascade source-follower, CSF.

Fig. 2(b) shows the cascade source-follower (CSF) as early presented in [8]. This approach is used to keep the input common-mode voltage (V_{CMI}) close to the output common-mode voltage (V_{CMO}). In the design if $V_{GS2} \approx V_{SG1}$ then the $V_{CMO} \approx V_{CMI}$. However, small changes in the process, voltage and temperature (PVT) of the operating design may incur in changes of V_{GS} [8].

2.2 Super Source-Follower (SSF)

Since most of the deep-submicron technologies operate with low positive power supply voltages (≤ 1.2 V) the simple SF and CSF voltage buffers may have a larger output resistance than the one needed to drive large capacitive loads [3, 4]. Hence, in some cases, a super source-follower (SSF), as shown in Fig. 3, is used as an improved version of the traditional SF. In fact, this architecture can lower the output resistance of this buffer significantly, through the negative feedback implemented through common-source (CS) transistor M2 [3, 4]. However, due to the feedback in voltage-mode, it usually presents some bandwidth resonance in frequencies close to the cutoff frequency.

Nevertheless, this SSF buffer represents a significant improvement of the traditional SF, especially for heavy and switched capacitive loads, since it has a lower output resistance and the feedback loop on M2 corrects some of the non-linearity of the V_{GS} signal dependency of CD device M1.

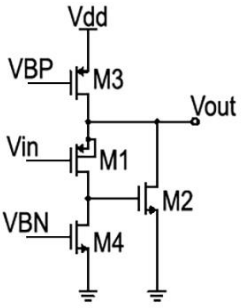

Fig. 3. Super source-follower (SSF).

2.3 Current-Feedback Input Buffer (CFIB)

The current-feedback input buffer (CFIB), as shown in Fig. 4, differs from the SSF since its feedback is in current-mode rather than in voltage-mode. Similar to the SSF, this current-mode negative feedback also maximizes the dynamic linearity of the SF and CSF architectures [6]. Moreover, it is better suited for operation with lower supply voltages.

The voltage at the drain of the main device M1 is used to regulate the V_{GS} of device M2. This will regulate the current flowing on the common-gate device M2 that is mirrored and fed-back by the wide-swing dynamic cascode-current-mirror composed by M3A and M4A. This feedback is controlled by the current mirroring factor (e.g., 1 : K where K represents the mirroring-ratio and usually made equal to 2, 3 or 4) between devices M3A and M3B, and devices M4A and M4B.

To reach a larger and an almost flat BW, the parasitic capacitances in the current-mode feedback-loop (particularly at the gate terminals of mirroring devices M3A and M3B) need to be minimized and properly compensation. With proper compensation, the AC current required to charge these parasitic capacitors is kept at its minimum value [6], while the feedback is still fast enough to improve (extend) the overall signal BW.

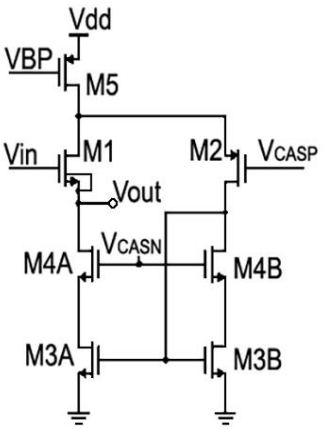

Fig. 4. Current Feedback Input Buffer (CFIB).

2.4 Cascade Source-Follower with V_{GS} Control (CSF-VC)

Fig. 5 shows the basic concept of the CSF circuit with V_{GS} control (CSF-VC) [8]. A global negative-feedback loop in the CSF further reduces the output resistance and keeps $V_{GS2} \approx V_{SG1}$, reducing both the constant and input-dependent components of the offset. Transistors M1 and M2 form the cascade source-follower. The gate and source of the PMOS transistor M3 are connected to the source and gate of NMOS device M2, allowing M3 to sense the V_{GS} of M2. Transistors M1 and M3 form a differential pair with current-mirror load M4 and M5. If $V_{GS2} \neq V_{SG1}$, the gate voltage of M9 is adjusted to change the current through M2 until V_{GS2} is approximately equal to V_{SG1}. A major aspect of this circuit is that it uses, simultaneously, local negative-feedback and local feedforward in the source followers to set the gain almost equal to unity and global feedback, thus reducing the gain and offset errors. Since global feedback is applied to a circuit with a small gain error, the BW of the circuit is significantly increased compared to circuits

relying on global feedback only to overcome gain errors. An additional compensation capacitor Cc needs to be added between the gate and the drain of transistor M9 for proper stabilization.

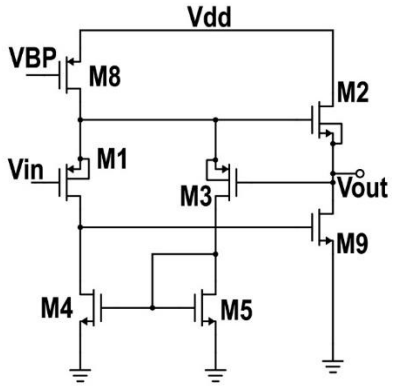

Fig. 5. Cascade Source Follower with VGS sensing (CSF-VC).

3 Proposed Input Buffer (IB) Circuit

The schematic of the proposed IB architecture is shown in Fig. 6. The main ideas behind our voltage buffer are: *i*) avoid the use of cascode structures at the output branch of the buffer circuit in order to maximize the output-swing and improve linearity; *ii*) implement all the necessary local feedback-loops, either positive or negative, in current-mode due to the reduced nominal power-supply. Common-drain (CD) devices M1 and M2 form a CSF and transistor M7 is in a common-gate (CG) configuration.

This IB uses two separated main current-mode feedback-loops. Similarly to the CFIB (removing the cascode device at the output branch), the first feedback-loop is implemented by the CG device M7 together with a wide-swing high-output impedance current-mirror comprising transistors M4 and M8-M11. When the voltage at the gate of M2 increases, the current increases. With this increase of the drain current, the voltage at the drain of M2 will decrease, decreasing the V_{GS} of M7 (V_{CASP} is a DC constant voltage biasing the CG device M7) and the current flowing through M7. The reduction in current in M7 will further decrease the gate voltage in M4. This first feedback-loop provides a local positive-feedback to guarantee additional bandwidth by quickly increase V_{out} when the input increases.

The second (negative) feedback-loop starts at the gate of M4, M9 and M14. When the voltage at this gate terminal decreases, then the current also decreases, since V_{GS} is reduced. This will increase the drain voltage of M14, decreasing the drain current of M12 and M5 (M12 and M5 form a basic current-mirror) feeding the main CD input device M1.

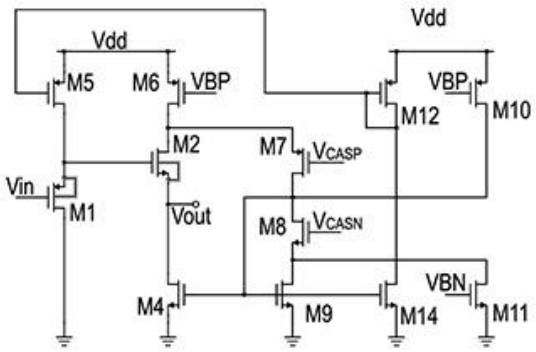

Fig. 5. Proposed Input Buffer.

Using MATLAB™ tool for Symbolic Analysis of Analog Circuits the transfer function (TF) at low-frequencies, and tolerating an error of the order of 10 %, is given by:

$$\text{DC Gain} = \frac{g_{m1} \cdot (g_{m4} + g_{m9})}{g_{m1} \cdot (g_{m4} + g_{m9}) + g_{m4} \cdot (g_{ds1} + g_{ds5})} \quad (1)$$

showing that the first stage feedback loop is the most important regarding low-frequency (DC) gain.

4 Simulation Results

The proposed IB has been designed and optimized employing a fully-differential structure and in a standard 1.2-V, 130-nm CMOS process node. Only standard devices have been employed. All IBs have been simulated in DC, AC, and using transient-noise simulations, in the same load conditions and with the same input signal (600 mVpp-differential). Hence, although the described IBs have different attenuations of the input signal at lower frequencies (DC gain), the output signal is kept similar for all topologies, in order to allow fair comparisons among all IBs. Moreover, all CD devices have been biased in the same operating bias condition in all the simulated IBs (i.e., in moderate inversion with V_{DSsat} ~ 100 mV) and the (switched) capacitive load has been normalized to 1 pF.

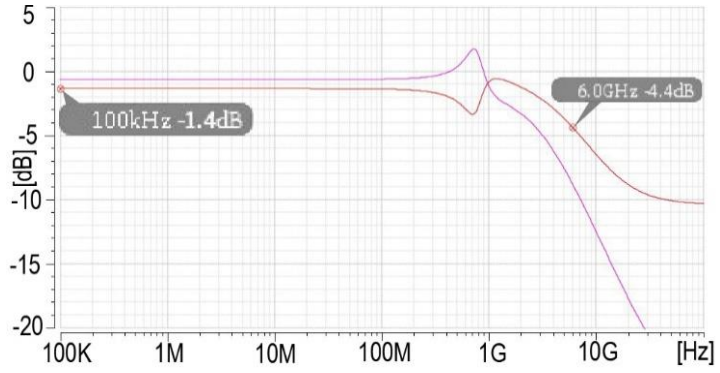

Fig. 6. Simulated frequency response of the two feedback-loops.

The frequency (AC) simulation results of the proposed IB demonstrate that the peaking at higher frequencies, which occurs in both circuits (SSF and the CFIB), is reduced in the proposed topology by employing the second current-mode negative feedback-loop. Fig. 6 shows the frequency response of each feedback-loop independently. Note that there are two resonances around the same frequency. Fig. 7 shows the overall (combined) simulated frequency response of the system where it is possible to see that the peaking is not that noticeable.

Transient-noise simulations have been performed in order to calculate the fast-Fourier-transform (FFT) of the output signal. The FFT results shown in Fig. 9 have been then used to calculate all key performance parameters regarding the dynamic linearity (THD and SFDR) and the signal-to-noise ratio (SNR).

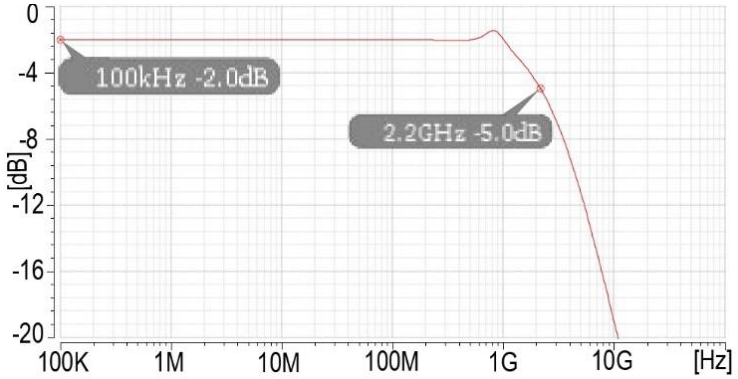

Fig. 7. Simulated frequency response of the proposed IB.

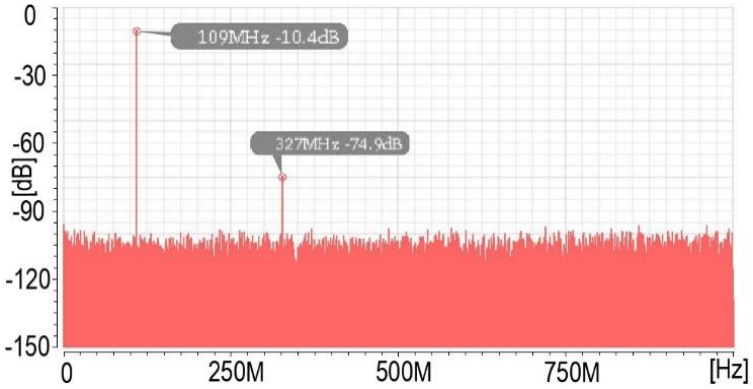

Fig. 8. Simulated FFT of the output signal (4096 bins and coherent sampling).

Similar simulations have been carried out of all the other IB architectures (also employing fully-differential designs), in order to compare them with the proposed IB. Table I shows the simulated key performance parameters for the different IBs.

In order to compare the energy-efficiency among the different IB solutions, and since the target application of the proposed IB is to drive high-speed ADCs, the well-known Walden figure-of-merit (FOM-W) has been used in the adapted form:

$$\text{FOM} - \text{W} = \frac{\text{Power}}{2^{\frac{\text{SNDR}-1.76}{6.02}} \cdot 2 \cdot \text{BW}} \qquad (2)$$

to account for the dissipated power, the signal bandwidth (BW) and both, the noise and the dynamic linearity (the signal-to-noise-plus-distortion-ratio, SNDR, taking into consideration both, the total-harmonic-distortion, THD, and the simulated transient noise). In case of the FOM-W, the lower the number the better the efficiency of the IB.

As stated in the Introduction section, since the IB will be interfacing between the LNA and the ADC, it must reach excellent dynamic performance in terms of BW, linearity (SNDR), and energy-efficiency (Power). Consequently, the design of these (IBs) guarantee that the dynamic specifications and the key performance parameters of the ADC are not significantly degraded.

To the best of the authors knowledge, the proposed IB is, in simulation, the most energy-efficient IB (reaching 1.83 fJ) among all from prior art, supplied with a single and nominal power supply of 1.2 V and comprising only standard (core) devices. Notice that, although the proposed IB has the highest current consumption among all, since it uses more active branches, it achieves the highest effective bandwidth (2.2 GHz) and the best linearity without the need of any type of additional compensation.

Table 1. Simulation Results in 1.2-V 130-nm Standard CMOS.

	SF [2]	CSF [8]	CFIB [6]	CSF-VC [8]	Proposed IB
Current consumption (mA) @ 1.2 V	2.0	2.6	3.0	2.8	**5.5**
Bandwidth (GHz) @ C_{LOAD} = 1pF	1.5	1.7	1.0	1.2	**2.2**
Input signal frequency (MHz)	109	109	109	109	**109**

Systematic offset (dB)	-121	-105	-106	-87	**-95**
$V_{CMI} = V_{CMO}$	No	Yes	No	Yes	**Yes**
HD2 (dB)	-80	-85	-84	-74	**-97**
HD3 (dB)	-55	-61	-54	-60	**-69**
IM3 (dB)	70	66	57	72	**65**
SFDR (dB)	55	61	54	57	**69**
SNDR (dB)	50	53	49	51	**60**
FOM-W (fJ)	3.10	2.51	7.82	4.83	**1.83**

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5 Conclusions

An energy-efficient input buffer architecture was presented in this paper and fairly compared to other existing IB realizations using a standard 1.2-V and 130-nm CMOS technology as reference. The proposed new architecture presents a better dynamic performance (fom, noise and distortion), it has a wider input signal BW and it can be readily used to drive moderate-resolution ADCs without requiring either a higher supply voltage or any non-standard I/O devices.

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