Experimental Evaluation of Neutron-Induced Errors on a RISC-V Processor

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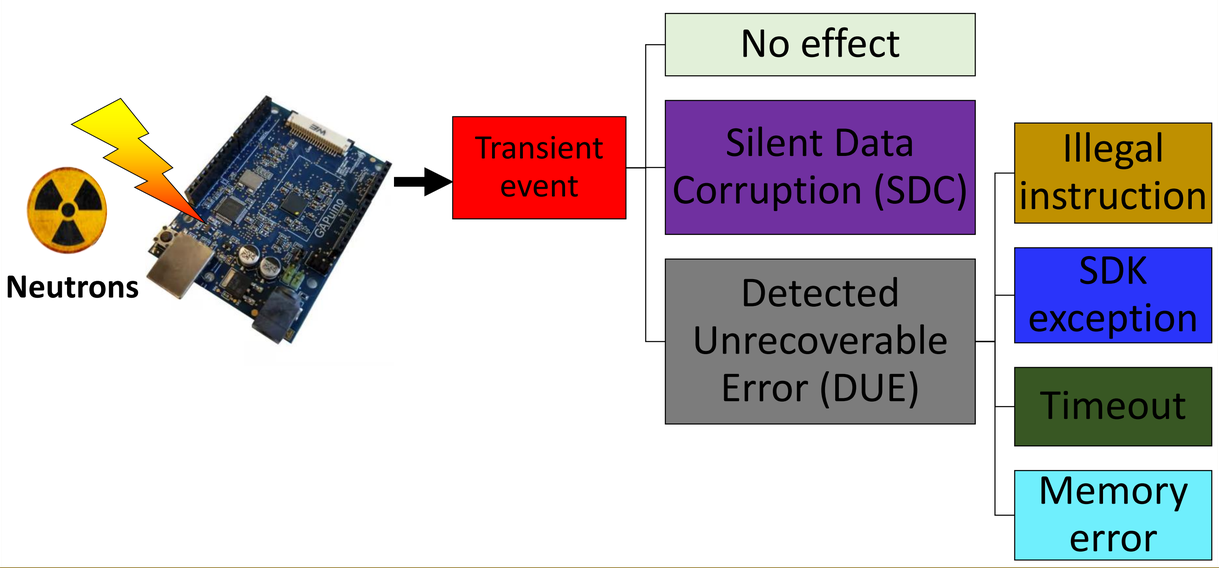
ERROR ANALYSIS

➢RISCV processors have been employed in smart houses, smart cities, space applications, etc. We investigated the error rate of a RISCV processor (GAP8) exposed to a neutron beam, and classified the execution outcomes.

➢A neutron strike may perturb a transistor's state, generating bit-flips in memory or current spikes in logic leading to errors.



EVALUATED PLATFORM

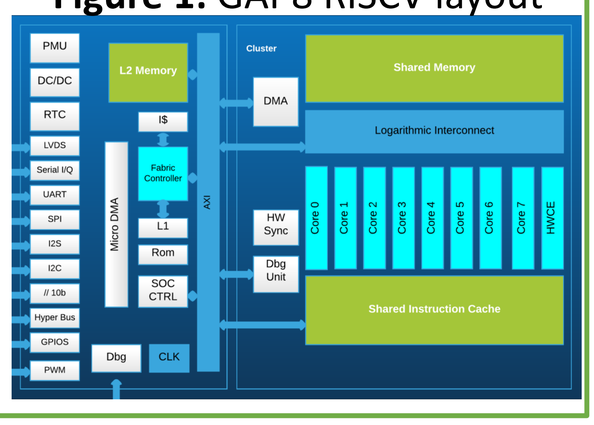
➢GAP8 from Greenwaves

➢Cluster of 8+1 RISC-V cores

➢Memory: L1 64KB, L2 512KB

➢Core max frequency: 175MHz

Figure 1: GAP8 RISCV layout

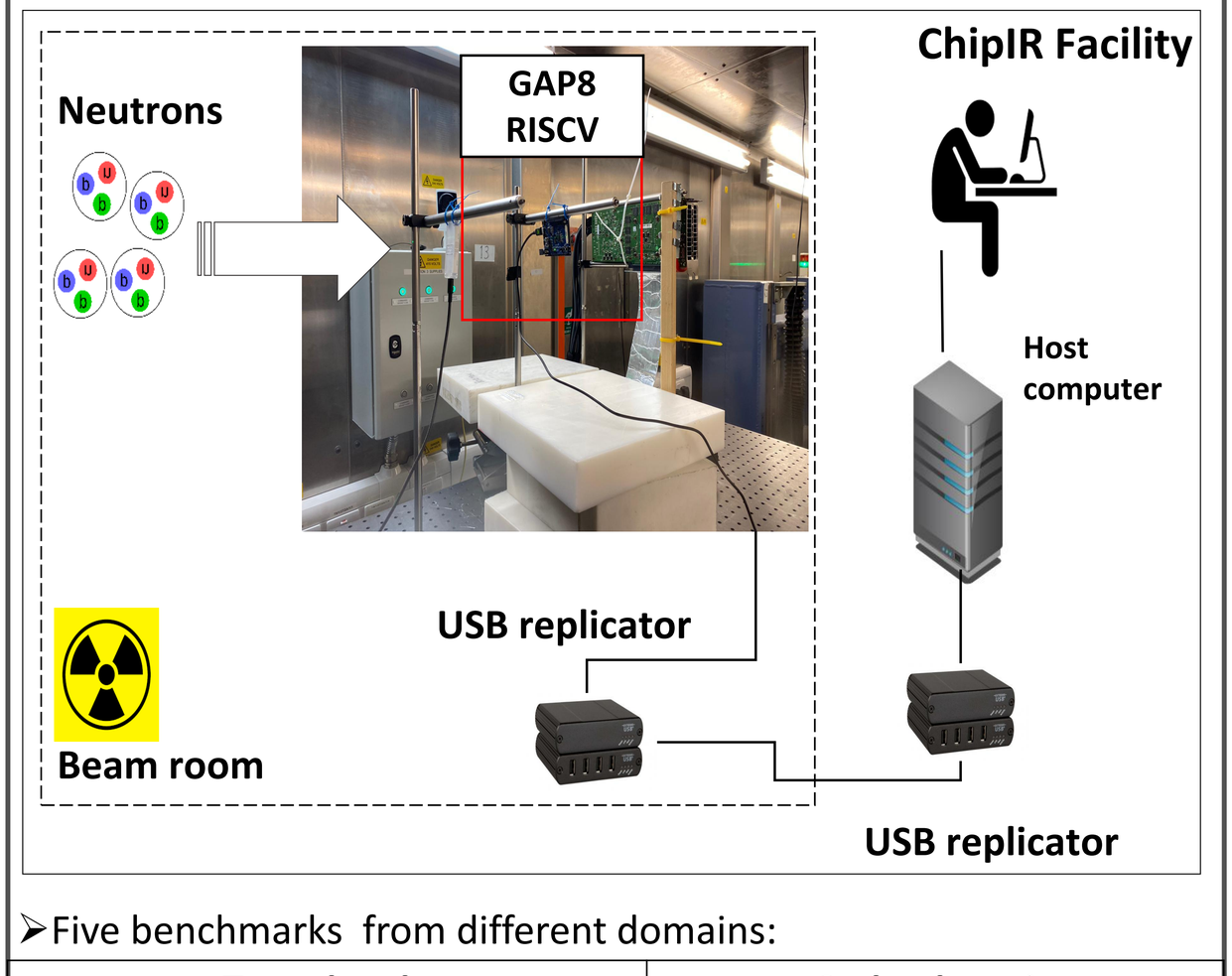


NEUTRON BEAM EXPERIMENTS

➢GAP8 exposed to a neutron beam (i.e., realistic error rate)

➢Experiments performed at ChipIR, RAL, UK

➢Neutron flux ≅ $3.5x10^6 n/cm^2/s$



➢Five benchmarks from different domains:

Tested code	Code domain
Finite Impulse Response (FIR)	Signal Processing
Matrix Addition	Linear algebra
Bilinear Resize	Image processing
Matrix multiplication	Linear Algebra
MNIST classification (CNN)	Machine learning

PRELIMINARY RESULTS

Figure 2: GAP8's error rate expressed as Cross Section, the number of errors observed divided by the fluence of neutrons. As cross-section depends on the number of resources used, MNIST has the highest error rate of all codes.

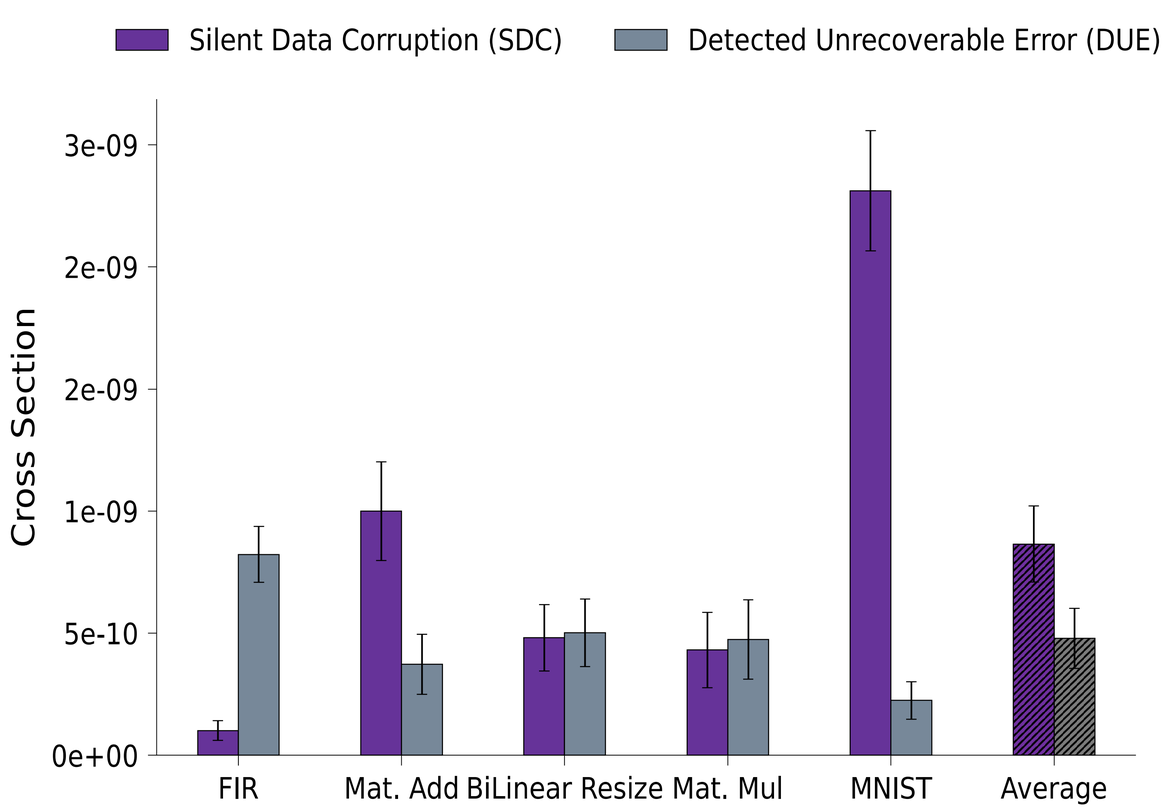
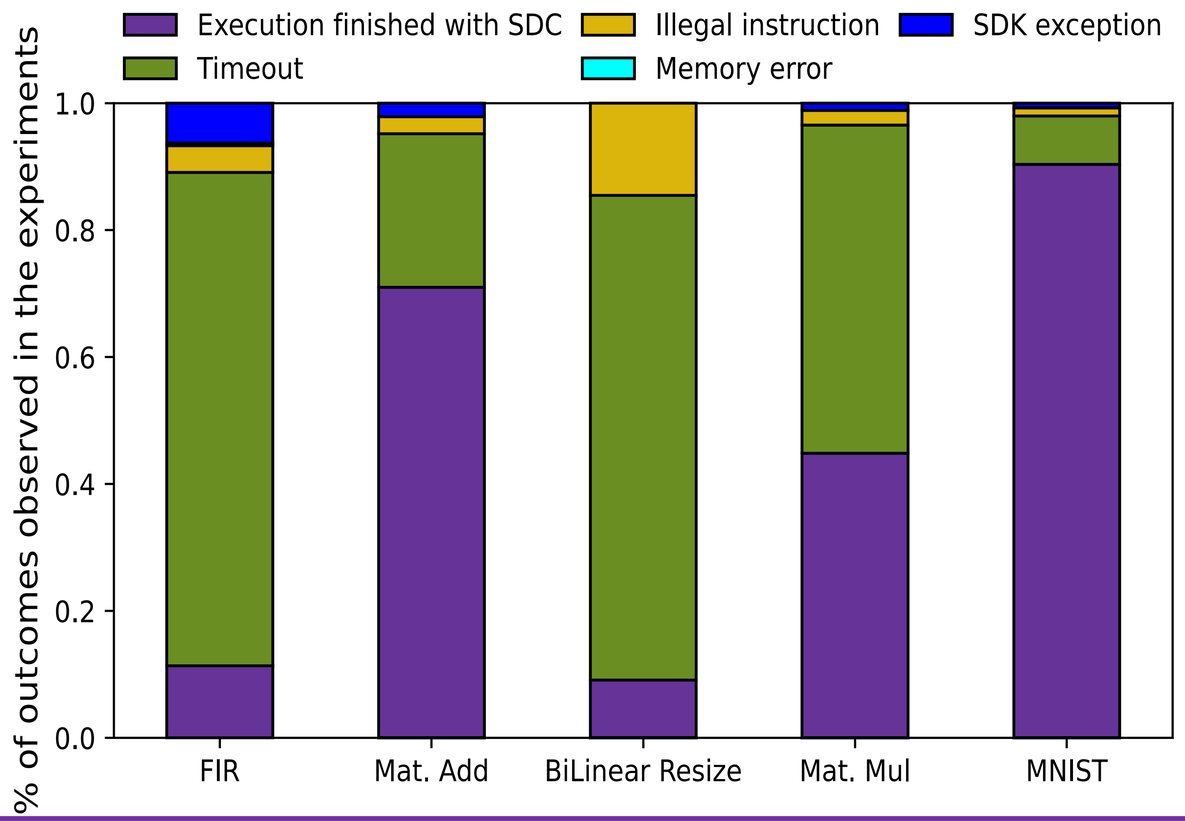


Figure 3: Most incorrect executions finished with an SDC or Timed out (e.g., due to an infinite loop). SDCs are not detectable without a fault-tolerance technique. An incorrect operation due to an SDC could lead to a catastrophic event.



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