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▶ **To cite this version:**

Fernando Fernandes dos Santos, Angeliki Kritikakou, Olivier Sentieys. Experimental evaluation of neutron-induced errors on a RISC-V processor. RISC-V Week 2022, May 2022, Paris, France. hal-03903370

HAL Id: hal-03903370

https://inria.hal.science/hal-03903370v1

Submitted on 16 Dec 2022

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Experimental evaluation of neutron-induced errors on a RISC-V processor

Fernando Fernandes dos Santos*, Angeliki Kritikakou*, and Olivier Sentieys*
*French Institute for Research in Computer Science and Automation (INRIA)

Introduction: Ultra low power processors based on RISC-V architecture have been employed in different applications, such as smart homes, space applications, smart cities, etc. [1], [2]. In some scenarios, the system must be reliable as a fault can compromise the system's ability to operate correctly. Fault sources can be environmental perturbations, ionizing radiation, software errors, and process, temperature, or voltage variations. It has been demonstrated that the faults caused by radiation have the highest error rates [3]. A terrestrial neutron strike may perturb a transistor's state, leading to an error. Neutron-induced events are typically soft because the device is not permanently damaged. A soft error can lead to: 1) **No effect on the program output**: The fault is masked, the program output is not affected. 2) **Silent Data Corruption (SDC)**: The program finishes, but the output is not correct, and no flag or indication is raised. 3) **Detected Unrecoverable Error (DUE)**: DUE is a class of error that makes the system stops working, forcing it to be rebooted or power cycled.

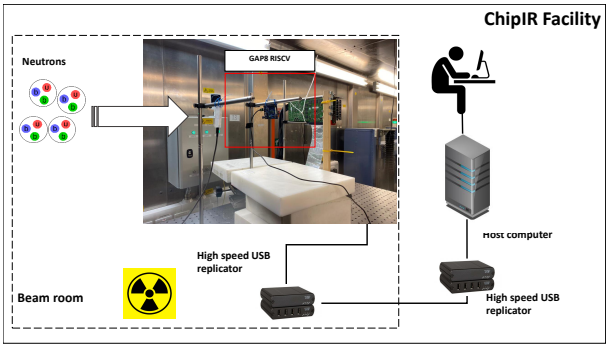

Fig. 1: GAP8 setup for the neutron beam experiments

Beam Experiment Setup: Beam experiments are the most effective way to evaluate the device reliability. We exposed a RISC-V processor (GAP8) on a neutron beam to evaluate its error rate. Our experiments were performed at the ChipIR facility of the Rutherford Appleton Laboratory, UK. Figure 1 shows the setup of our experiments. The facility delivers a beam of neutrons with a spectrum of energies that resembles the atmospheric neutron one [4]. Experimental data can then be scaled to the natural radioactive environment.

In the setup described in Figure 1, the *Host computer* runs a Python script that launches the kernels on the GAP8 device while the processor is on the neutron beam. A high-speed USB replicator connects the device inside the beam room to the host computer. The scripts can detect if the device does not produce the correct output (i.e., Execution finishes with SDC), hanged (Timeout error), or crashes due to runtime errors such as Illegal instructions, Memory allocation error, GAP 8 SDK exception, application Runtime error.

Preliminary results: We have evaluated five representative codes, Finite Impulse Response (FIR), Matrix Addition, Image Bilinear Resize, Matrix Multiplication (MxM), and a Convolutional Neural Network classifying digits from the MNIST dataset (referred to as MNIST code). All the evaluated codes are commonly used algorithms for Deep Neural Networks, the core of applications such as smart homes, autonomous cars, intelligent agricultural devices, etc.

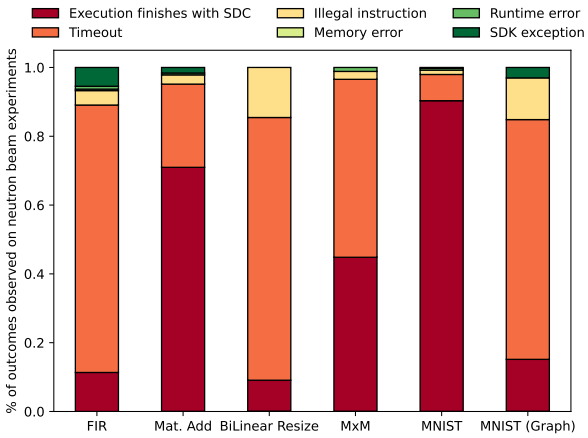

Fig. 2: Outcomes observed on the neutron beam experiments.

From Figure 2 it is worth noting that most of the incorrect executions are composed of executions that have an SDC and the ones that hanged (Timeout). Timeout errors are part of the DUE errors. Even if they pose a reliability issue, they are at least detectable. Contrarily, the SDCs are not detectable without a fault-tolerance technique applied to the system. SDCs are a critical issue even for smart home appliances. For instance, consider a system that controls an intelligent air conditioner that operates with high voltages. An incorrect operation due to an incorrect output (i.e., SDC) could lead to a catastrophic event.

In future works, we will perform fault injection and evaluate the source of the errors to understand the RISC-V errors observed in the radiation experiments deeply. Thus, we can propose fault tolerance to increase the reliability of RISC-V architectures.

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