

## VLSI-SoC: Design Trends

Andrea Calimera, Pierre-Emmanuel Gaillardon, Kunal Korgaonkar, Shahar Kvatinsky, Andre Reis

## ▶ To cite this version:

Andrea Calimera, Pierre-Emmanuel Gaillardon, Kunal Korgaonkar, Shahar Kvatinsky, Andre Reis. VLSI-SoC: Design Trends. Andrea Calimera; Pierre-Emmanuel Gaillardon; Kunal Korgaonkar; Shahar Kvatinsky; Ricardo Reis. Springer International Publishing, AICT-621, pp.i-xviii, 2021, VLSI-SoC: Design Trends, 978-3-030-81641-4. 10.1007/978-3-030-81641-4. hal-03759823

# HAL Id: hal-03759823 https://inria.hal.science/hal-03759823v1

Submitted on 24 Aug 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers. L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



### Editor-in-Chief

Kai Rannenberg, Goethe University Frankfurt, Germany

#### **Editorial Board Members**

TC 1 - Foundations of Computer Science

Luís Soares Barbosa, University of Minho, Braga, Portugal

TC 2 - Software: Theory and Practice

Michael Goedicke, University of Duisburg-Essen, Germany

TC 3 – Education

Arthur Tatnall, Victoria University, Melbourne, Australia

TC 5 - Information Technology Applications

Erich J. Neuhold, University of Vienna, Austria

TC 6 - Communication Systems

Burkhard Stiller, University of Zurich, Zürich, Switzerland

TC 7 - System Modeling and Optimization

Fredi Tröltzsch, TU Berlin, Germany

TC 8 - Information Systems

Jan Pries-Heje, Roskilde University, Denmark

TC 9 – ICT and Society

David Kreps, National University of Ireland, Galway, Ireland

TC 10 - Computer Systems Technology

Ricardo Reis, Federal University of Rio Grande do Sul, Porto Alegre, Brazil

TC 11 - Security and Privacy Protection in Information Processing Systems

Steven Furnello, Plymouth University, UK

TC 12 - Artificial Intelligence

Eunika Mercier-Laurent, University of Reims Champagne-Ardenne, Reims, France

TC 13 - Human-Computer Interaction

Marco Winckler, University of Nice Sophia Antipolis, France

TC 14 – Entertainment Computing

Rainer Malaka, University of Bremen, Germany

## IFIP - The International Federation for Information Processing

IFIP was founded in 1960 under the auspices of UNESCO, following the first World Computer Congress held in Paris the previous year. A federation for societies working in information processing, IFIP's aim is two-fold: to support information processing in the countries of its members and to encourage technology transfer to developing nations. As its mission statement clearly states:

IFIP is the global non-profit federation of societies of ICT professionals that aims at achieving a worldwide professional and socially responsible development and application of information and communication technologies.

IFIP is a non-profit-making organization, run almost solely by 2500 volunteers. It operates through a number of technical committees and working groups, which organize events and publications. IFIP's events range from large international open conferences to working conferences and local seminars.

The flagship event is the IFIP World Computer Congress, at which both invited and contributed papers are presented. Contributed papers are rigorously refereed and the rejection rate is high.

As with the Congress, participation in the open conferences is open to all and papers may be invited or submitted. Again, submitted papers are stringently refereed.

The working conferences are structured differently. They are usually run by a working group and attendance is generally smaller and occasionally by invitation only. Their purpose is to create an atmosphere conducive to innovation and development. Refereeing is also rigorous and papers are subjected to extensive group discussion.

Publications arising from IFIP events vary. The papers presented at the IFIP World Computer Congress and at open conferences are published as conference proceedings, while the results of the working conferences are often published as collections of selected and edited papers.

IFIP distinguishes three types of institutional membership: Country Representative Members, Members at Large, and Associate Members. The type of organization that can apply for membership is a wide variety and includes national or international societies of individual computer scientists/ICT professionals, associations or federations of such societies, government institutions/government related organizations, national or international research institutes or consortia, universities, academies of sciences, companies, national or international associations or federations of companies.

More information about this series at http://www.springer.com/series/6102

Andrea Calimera · Pierre-Emmanuel Gaillardon · Kunal Korgaonkar · Shahar Kvatinsky · Ricardo Reis (Eds.)

# VLSI-SoC: Design Trends

28th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2020 Salt Lake City, UT, USA, October 6–9, 2020 Revised and Extended Selected Papers



Editors
Andrea Calimera
Politecnico di Torino
Turin, Italy

Kunal Korgaonkar D
Technion – Israel Institute of Technology
Haifa, Israel

Ricardo Reis D
Universidade Federal do Rio Grande do Sul
Porto Alegre, Brazil

Pierre-Emmanuel Gaillardon D University of Utah Salt Lake City, UT, USA

Shahar Kvatinsky (5)
Technion – Israel Institute of Technology
Haifa, Israel

ISSN 1868-4238 ISSN 1868-422X (electronic)
IFIP Advances in Information and Communication Technology
ISBN 978-3-030-81640-7 ISBN 978-3-030-81641-4 (eBook)
https://doi.org/10.1007/978-3-030-81641-4

#### © IFIP International Federation for Information Processing 2021

This work is subject to copyright. All rights are reserved by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed.

The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

The publisher, the authors and the editors are safe to assume that the advice and information in this book are believed to be true and accurate at the date of publication. Neither the publisher nor the authors or the editors give a warranty, expressed or implied, with respect to the material contained herein or for any errors or omissions that may have been made. The publisher remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

This Springer imprint is published by the registered company Springer Nature Switzerland AG The registered company address is: Gewerbestrasse 11, 6330 Cham, Switzerland

## **Preface**

This book contains extended and revised versions of the highest quality papers presented during the 28th edition of the IFIP/IEEE WG 10.5 International Conference on Very Large Scale Integration (VLSI-SoC 2020), a global system-on-chip design and CAD conference. The 28th edition of the conference was held during October 6–9, 2020, virtually from Salt Lake City, USA. Previous conferences have taken place in Edinburgh, Scotland (1981); Trondheim, Norway (1983); Tokyo, Japan (1985); Vancouver, Canada (1987); Munich, Germany (1989); Edinburgh, Scotland (1991); Grenoble, France (1993); Chiba, Japan (1995); Gramado, Brazil (1997); Lisbon, Portugal (1999); Montpellier, France (2001); Darmstadt, Germany (2003); Perth, Australia (2005); Nice, France (2006); Atlanta, USA (2007); Rhodes Island, Greece (2008); Florianopolis, Brazil (2009); Madrid, Spain (2010); Kowloon, Hong Kong (2011), Santa Cruz, USA (2012), Istanbul, Turkey (2013), Playa del Carmen, Mexico (2014), Daejeon, South Korea (2015), Tallin, Estonia (2016), Abu Dhabi, United Arab Emirates (2017), Verona, Italy (2018), and Cuzco, Peru (2019).

The purpose of this conference, sponsored by the IFIP TC 10 Working Group 10.5, the IEEE Council on Electronic Design Automation (CEDA), and the IEEE Circuits and Systems Society, with the in-cooperation of ACM SIGDA, is to provide a forum for the presentation and discussion of the latest academic and industrial results and developments as well as the future trends in the field of system-on-chip (SoC) design, considering the challenges of nano-scale along with state-of-the-art and emerging manufacturing technologies. In particular, VLSI-SoC 2020 addressed cutting-edge research fields like low-power design of RF, analog and mixed-signal circuits, EDA tools for the synthesis and verification of heterogenous SoCs, accelerators for cryptography and deep learning and on-chip interconnection systems, reliability and testing, and integration of 3D-ICs. The chapters of this new book in the VLSI-SoC series continue its tradition of providing an internationally acknowledged platform for scientific contributions and industrial progress in this field.

For VLSI-SoC 2020, 38 papers out of 74 submissions were selected for oral presentation, and out of those 38 full papers presented at the conference, 16 papers were chosen by a special selection committee to have an extended and revised version included in this book. The selection process for these papers considered the evaluation scores during the review process as well as the review forms provided by members of the Technical Program Committee and the session chairs as a result of the presentations.

The chapters of this book have authors from Belgium, Brazil, England, France, Germany, Israel, Italy, Japan, and USA. The Technical Program Committee for the regular tracks comprised 93 members from 23 countries.

VLSI-SoC 2020 was the culmination of the work of many dedicated volunteers: paper authors, reviewers, session chairs, invited speakers, and various committee chairs. We thank them all for their contributions.

#### vi Preface

This book is intended for the VLSI community at large, and in particular the many colleagues who did not have the chance to attend the conference. We hope that you enjoy reading this book and find it useful in your professional life and for the development of the VLSI community as a whole.

May 2021

Andrea Calimera Pierre-Emmanuel Gaillardon Kunal Korgaonkar Shahar Kvatinsky Ricardo Reis

## **Organization**

The IFIP/IEEE International Conference on Very Large Scale Integration System-on-Chip (VLSI-SoC) 2020 took place during October 6–9, 2020, virtually from Salt Lake City, USA. VLSI-SoC 2020 was the 28th in a series of international conferences, sponsored by IFIP TC 10 Working Group 10.5 (VLSI), IEEE CEDA, and ACM SIGDA. The Organization Committee of the conference consisted of the following colleagues:

#### **General Chair**

Pierre-Emmanuel
Gaillardon

University of Utah, USA

## **Technical Program Chairs**

Shahar Kvatinsky Technion, Israel

Andrea Calimera Politecnico di Torino, Italy

## **Special Sessions Chairs**

Mike Niemier University of Notre Dame, USA

David Atienza EPFL, Switzerland

PhD Forum Chair

Cunxi Yu University of Utah, USA

**Local Chairs** 

Ross Walker University of Utah, USA

Mike Wirthlin Brigham Young University, USA

**Industrial Chair** 

Luca Amaru Synopsys, USA

**Publicity Chairs** 

Anupam Chattopadhyay
Andre Reis
UFRGS, Brazil
Ian O'Connor
Joseph Friedman
UT Dallas, USA

## **Publication Chair**

Kunal Korgaonkar Technion, Israel

#### Web Chairs

viii

Ganesh Gore University of Utah, USA Edouard Giacomin University of Utah, USA

### **VLSI-SoC Steering Committee**

Graziano Pravadelli
Ibrahim Elfadel
Manfred Glesner
Matthew Guthaus
Luis Miguel Silveira
University of Verona, Italy
Khalifa University, UAE
TU Darmstadt, Germany
UC Santa Cruz, USA
INESC ID, Portugal

Fatih Ugurdag Ozyegin University, Turkey

Salvador Mir TIMA, France Ricardo Reis UFRGS, Brazil

Chi-Ying Tsui HKUST, Hong Kong, China

Ian O'Connor INL, France

Masahiro Fujita The University of Tokyo, Japan

As for the Technical Program Committee, it was composed as follows:

## **Technical Program Committee Track Chairs**

## AMS, Sensors, and RF Track

Salvador Mir TIMA, France

Ross Walker University of Utah, USA

#### VLSI Circuits and SoC Design Track

H. Fatih Ugurdag Ozyegin University, Istanbul Adam Teman Bar-Ilan University, Israel

#### **Embedded Systems Design and Software Track**

Ibrahim Elfadel Khalifa University, UAE Michele Magno ETH Zurich, Switzerland

## CAD Tools and Methodologies for Digital IC Design and Optimization Track

Victor Grimblatt Synopsys, Chile

Aida Todri-Sanial University of Montpellier and CNRS, France

#### Verification, Modeling, and Prototyping Track

Graziano Pravadelli Università di Verona, Italy

Yakir Vizel Technion, Israel

#### Design for Testability, Reliability, and Fault Tolerance Track

Matteo Sonza Reorda Politecnico di Torino, Italy

Leticia Bolzani Poehls PUCRS and RWTH Aachen, Germany

#### **Hardware Security Track**

Odysseas Koufopavlou University of Patras, Greece

Anupam Chattopadhyay Nanyang Technological University of Singapore,

Singapore

#### **Emerging Technologies and New Computing Paradigms Track**

Ian O'Connor Lyon Institute of Nanotechnology, France

Yang (Cindy) Yi Virginia Tech, USA

## **Technical Program Committee**

Alain Pegatoguet University of Nice, France
Alberto Bosio Ecole Centrale de Lyon, France
Alessandro Cimatti Fondazione Bruno Kessler, Italy

Alexander Ivrii IBM, Israel Alexander Nadel Intel, Israel

Alexandre Levisse EPFL, Switzerland

Ali Akoglu University of Arizona, USA Armin Tajalli University of Utah, USA

Arnaud Virazel University of Montpellier, France

Avi Mendelson Technion, Israel

Ayesha Khalid Queen's University Belfast, Northern Ireland

Azemard Nadine University of Montpellier, France

Bah Hwee Gwee Nanyang Technological University of Singapore,

Singapore

C. Andras Moritz University of Massachusetts, USA

Carlos Silva-Cardenas Pontificia Universidad Catolica del Peru, Peru

Chester Rebeiro IIT Madras, India

Christos Papachristou Case Western Reserve University, USA Chun-Jen Tsai National Chiao Tung University, Taiwan

Daniele Pagliari Politecnico di Torino, Italy

David Atienza EPFL, Switzerland
Debdeep Mukhopadhyay IIT Kharagpur, India

Dimitrios Soudris National Technical University of Athens, Greece

Donatella Sciuto Politecnico di Milano, Italy

Elena Ioana Vatajelu TIMA, France

#### Organization

Francesco Regazzoni

George Gielen

Х

ALaRI, Switzerland

Catholic University of Leuven, Belgium

University of Texas at Dallas, USA Université Grenoble Alpes, France

National Chiao Tung University, Taiwan

George Yuan Hong-Kong University of Science and Technology,

Hong Kong

Brown University, USA

Gianvito Urgese

Gurgen Harutvunvan

Jacob Rosenstein Joseph Friedman

Katell Morin-Allory Ke-Horng Chen L. Miguel Silveira

Lars Bauer Luc Claesen

Maciej Ogorzalek Marco Donato

Matthew Guthaus Matthew Johnston Michail Maniatakos

Michele Lora Michele Portolan

Mottagiallah Taouil Nicola Nicolici

Ozgur Tasdizen Paolo Rech

Peng Liu Per Larsson-Edefors

Piero Malcovati Pramod Subramanyan

Piero Malcovati

Ricardo Reis

Robert Wille Rongmei Chen

Salvatore Pennisi Sébastien Le Beux Seiji Kajihara

Sezer Gören Shigeru Yamashita

Shiyam Bhasin

Smail Niar

Politecnico di Torino, Italy Gilles Sicard CEA LETI. France Synopsys, Armenia

Karlsruhe Institute of Technology, Germany Hasselt University, Belgium Jagiellonian University, Poland

Harvard University, USA University of California, Santa Cruz, USA

Oregon State University, USA NYU Abu Dhabi, UAE

University of Lisbon, Portugal

Singapore University of Technology, Singapore Grenoble INP. France

Delft University of Technology, the Netherlands

McMaster University, Canada

ARM, England

Federal University of Rio Grande do Sul, Brazil

Zhejiang University, China

Chalmers University of Technology, Sweden

University of Pavia, Italy University of Pavia, Italy

Indian Institute of Technology, Italy Universidade Federal do Rio Grande do Sul, Brazil

Linz University, Austria

IMEC, Belgium

University of Catania, Italy Concordia University, Canada

Kyushu Institute of Technology, Japan Yeditepe University, Turkey

Ritsumeikan University, Japan

Nanyang Technological University of Singapore,

Singapore

Université Polytechnique Hauts-de-France, France

University of South Florida, USA Srinivas Katkoori Sujoy Sinha Roy University of Birmingham, England Pennsylvania State University, USA Swaroop Chosh Svlvain Bourdel Université Grenoble Alpes, France The University of Tokyo, Japan Tetsuya Iizuka

Tiago Balen Federal University of Rio Grande do Sul, Brazil

Tiziana Margaria Lero, Ireland

Tolga Yalcin Northern Arizona University, USA Vasilis Pavlidis University of Manchester, England

Walter Weber TU Wien, Austria

Wenjing Rao University of Illinois at Chicago, USA Xing Huang Technical University of Munich, Germany

Yuanqing Cheng Beihang University, China Zhaohao Wang Beihang University, China

# Contents

Low-Power High-Speed ADCs for ADC-Based Wireline Receivers in 22 nm FDSOI	1
Mixed-Mode Signal Processing for Implementing MCMC  MIMO Detector	21
Low Power Current-Mode Relaxation Oscillators for Temperature and Supply Voltage Monitoring	39
Fully-Autonomous SoC Synthesis Using Customizable Cell-Based Analog and Mixed-Signal Circuits Generation	65
Assessing the Configuration Space of the Open Source NVDLA Deep Learning Accelerator on a Mainstream MPSoC Platform	87
SAT-Based Mapping of Data-Flow Graphs onto Coarse-Grained Reconfigurable Arrays	113
Learning Based Timing Closure on Relative Timed Design	133
Multilevel Signaling for High-Speed Chiplet-to-Chiplet Communication Rakshith Saligram, Ankit Kaul, Muhannad S. Bakir, and Arijit Raychowdhury	149
From Informal Specifications to an ABV Framework for Industrial Firmware Verification	179
Samuele Germiniani, Moreno Bragaglio, and Graziano Pravadelli	11)

## xiv Contents

Modular Functional Testing: Targeting the Small Embedded Memories in GPUs	205
Josie Esteban Rodriguez Condia and Matteo Sonza Reorda	203
RAT: A Lightweight Architecture Independent System-Level Soft Error Mitigation Technique.	235
Jonas Gava, Ricardo Reis, and Luciano Ost	
SANSCrypt: Sporadic-Authentication-Based Sequential Logic Encryption Yinghua Hu, Kaixin Yang, Shahin Nazarian, and Pierluigi Nuzzo	255
3D Nanofabric: Layout Challenges and Solutions for Ultra-scaled Logic Designs	279
Edouard Giacomin, Juergen Boemmels, Julien Ryckaert, Francky Catthoor, and Pierre-Emmanuel Gaillardon	
3D Logic Cells Design and Results Based on Vertical NWFET Technology Including Tied Compact Model	301
Arnaud Poittevin, Chhandak Mukherjee, Ian O'Connor, Cristell Maneux, Guilhem Larrieu, Marina Deng, Sebastien Le Beux, François Marc, Aurélie Lecestre, Cedric Marchand, and Abhishek Kumar	
Statistical Array Allocation and Partitioning for Compute	
In-Memory Fabrics	323
abstractPIM: A Technology Backward-Compatible Compilation Flow for Processing-In-Memory	343
Author Index	363

## **List of Contributors**

**Amin Aghighi** Electrical and Computer Engineering Department, University of Utah, Salt Lake City, USA

Tutu Ajayi University of Michigan, Ann Arbor, MI, USA

Muhannad S. Bakir Georgia Institute of Technology, Atlanta, GA, USA

Rotem Ben-Hur Technion - Israel Institute of Technology, Haifa, Israel

**Davide Bertozzi** Department of Engineering, Universitá degli Studi di Ferrara, Ferrara, Italy

David Blaauw University of Michigan, Ann Arbor, MI, USA

Juergen Boemmels IMEC, Leuven, Belgium

**Moreno Bragaglio** Department of Computer Science, University of Verona, Verona, Italy

Benton Calhoun University of Virginia, Charlottesville, VA, USA

Francky Catthoor IMEC, Leuven, Belgium; KU Leuven, Leuven, Belgium

Chien-Hen Chen University of Virginia, Charlottesville, VA, USA

Yaswanth K. Cherivirala University of Michigan, Ann Arbor, MI, USA

**Josie Esteban Rodriguez Condia** Dip. di Automatica e Informatica (DAUIN), Politecnico di Torino, Torino, Italy

Wim Cops MACOM Technology Solutions, Sophia Antipolis, France

David Cordova MACOM Technology Solutions, Sophia Antipolis, France

Brian Crafton Georgia Institute of Technology, Atlanta, GA, USA

Shanshan Dai Brown University, Providence, RI, USA

Marina Deng University of Bordeaux, CNRS UMR 5218, Bordeaux INP Talence, Bordeaux, France

**Yann Deval** Laboratorie IMS, Université de of Bordeaux, Bordeaux INP, CNRS UMR 5218, Talence, France

Ronald Dreslinski Jr. University of Michigan, Ann Arbor, MI, USA

Wenbo Duan University of Michigan, Ann Arbor, MI, USA

Adi Eliahu Technion - Israel Institute of Technology, Haifa, Israel

**Behrouz Farhang-Boroujeny** Electrical and Computer Engineering Department, University of Utah, Salt Lake City, USA

Morteza Fayazi University of Michigan, Ann Arbor, MI, USA

Masahiro Fujita The University of Tokyo, Tokyo, Japan

Pierre-Emmanuel Gaillardon University of Utah, Salt Lake City, UT, USA

**Jonas Gava** Instituto de Informática, PGMicro, Universidade Federal do Rio Grande do Sul - UFRGS, 9500, Porto Alegre, Brazil

**Samuele Germiniani** Department of Computer Science, University of Verona, Verona, Italy

Edouard Giacomin University of Utah, Salt Lake City, UT, USA

Shourya Gupta University of Virginia, Charlottesville, VA, USA

Kangping Hu Brown University, Providence, RI, USA

Yinghua Hu University of Southern California, Los Angeles, CA, USA

Sumanth Kamineni University of Virginia, Charlottesville, VA, USA

Ankit Kaul Georgia Institute of Technology, Atlanta, GA, USA

Sumanth Kolluru University of Utah, Salt Lake City, USA

Tushar Krishna Georgia Institute of Technology, Atlanta, GA, USA

**Milos Krstic** IHP - Leibniz-Institut für innovative Mikroelektronik, Frankfurt Oder, Germany

**Abhishek Kumar** Université de Toulouse, LAAS, CNRS, INP Toulouse, Toulouse, France

Shahar Kvatinsky Technion - Israel Institute of Technology, Haifa, Israel

**Kyumin Kwon** University of Michigan, Ann Arbor, MI, USA

**Herve Lapuyade** Laboratorie IMS, Université de of Bordeaux, Bordeaux INP, CNRS UMR 5218, Talence, France

**Guilhem Larrieu** Université de Toulouse, LAAS, CNRS, INP Toulouse, Toulouse, France; Institute of Industrial Science, LIMMS-CNRS/IIS, The University of Tokyo, Tokyo, Japan

**Sebastien Le Beux** Lyon Institute of Nanotechnology, University of Lyon, CNRS UMR 5270, Lyon, France; Ecole Centrale de Lyon, Ecully, France

**Aurélie Lecestre** Université de Toulouse, LAAS, CNRS, INP Toulouse, Toulouse, France

Jeongsup Lee University of Michigan, Ann Arbor, MI, USA

Xiaoyu Lian Brown University, Providence, RI, USA

Sung-Kyu Lim Georgia Institute of Technology, Atlanta, GA, USA

**Cristell Maneux** University of Bordeaux, CNRS UMR 5218, Bordeaux INP Talence, Bordeaux, France

**François Marc** University of Bordeaux, CNRS UMR 5218, Bordeaux INP Talence, Bordeaux, France

**Cedric Marchand** Lyon Institute of Nanotechnology, University of Lyon, CNRS UMR 5270, Ecole Centrale de Lyon, Ecully, France

Alan Mishchenko UC Berkeley, Berkeley, CA, USA

Yukio Miyasaka UC Berkeley, Berkeley, CA, USA

**Chhandak Mukherjee** University of Bordeaux, CNRS UMR 5218, Bordeaux INP Talence, Bordeaux, France

Gauthaman Murali Georgia Institute of Technology, Atlanta, GA, USA

Shahin Nazarian University of Southern California, Los Angeles, CA, USA

Nicolas Nodenot MACOM Technology Solutions, Sophia Antipolis, France

Pierluigi Nuzzo University of Southern California, Los Angeles, CA, USA

**Ian O'Connor** Lyon Institute of Nanotechnology, University of Lyon, CNRS UMR 5270, Ecole Centrale de Lyon, Ecully, France

Luciano Ost Wolfson School, Loughborough University, Loughborough, England

Yohan Piccin MACOM Technology Solutions, Sophia Antipolis, France

**Arnaud Poittevin** Lyon Institute of Nanotechnology, University of Lyon, CNRS UMR 5270, Ecole Centrale de Lyon, Ecully, France

**Graziano Pravadelli** Department of Computer Science, University of Verona, Verona, Italy

Arijit Raychowdhury Georgia Institute of Technology, Atlanta, GA, USA

Sherief Reda Brown University, Providence, RI, USA

**Ricardo Reis** Instituto de Informática, PGMicro, Universidade Federal do Rio Grande do Sul - UFRGS, 9500, Porto Alegre, Brazil

**François Rivet** Laboratorie IMS, Université de of Bordeaux, Bordeaux INP, CNRS UMR 5218, Talence, France

Ronny Ronen Technion - Israel Institute of Technology, Haifa, Israel

Jacob K. Rosenstein Brown University, Providence, RI, USA

Julien Ryckaert IMEC, Leuven, Belgium

Mehdi Saligane University of Michigan, Ann Arbor, MI, USA

Rakshith Saligram Georgia Institute of Technology, Atlanta, GA, USA

Tannu Sharma University of Utah, Salt Lake City, USA

**Matteo Sonza Reorda** Dip. di Automatica e Informatica (DAUIN), Politecnico di Torino, Torino, Italy

Samuel Spetalnick Georgia Institute of Technology, Atlanta, GA, USA

Kenneth S. Stevens University of Utah, Salt Lake City, USA

Dennis Sylvester University of Michigan, Ann Arbor, MI, USA

**Armin Tajalli** Electrical and Computer Engineering Department, University of Utah, Salt Lake City, USA

Caleb R. Tulloss Columbia University, New York, NY, USA

**Alessandro Veronesi** IHP - Leibniz-Institut für innovative Mikroelektronik, Frankfurt Oder, Germany

John Wawrzynek UC Berkeley, Berkeley, CA, USA

David D. Wentzloff University of Michigan, Ann Arbor, MI, USA

Kaixin Yang University of Southern California, Los Angeles, CA, USA