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► **To cite this version:**

David Cordova, Wim Cops, Yann Deval, François Rivet, Herve Lapuyade, et al.. Low-Power High-Speed ADCs for ADC-Based Wireline Receivers in 22 nm FDSOI. 28th IFIP/IEEE International Conference on Very Large Scale Integration - System on a Chip (VLSI-SoC), Oct 2020, Salt Lake City, UT, United States. pp.1-19, 10.1007/978-3-030-81641-4\_1 . hal-03759737

**HAL Id: hal-03759737**

**<https://inria.hal.science/hal-03759737>**

Submitted on 24 Aug 2022

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# Low-Power High-Speed ADCs for ADC-Based Wireline Receivers in 22nm FDSOI

David Cordova<sup>2</sup>, Wim Cops<sup>2</sup>, Yann Deval<sup>1</sup>, François Rivet<sup>1</sup>, Herve Lapuyade<sup>1</sup>,  
Nicolas Nodenot<sup>2</sup>, and Yohan Piccin<sup>2</sup>

<sup>1</sup> Laboratoire IMS, Université de Bordeaux, Bordeaux  
INP, CNRS UMR 5218, Talence, France

<sup>2</sup> MACOM Technology Solutions, Sophia Antipolis, France

**Abstract.** A very low-power 875MS/s 7b single-channel high-speed successive approximation register (SAR) analog-to-digital converter (ADC) that achieves a SNDR/SFDR at Nyquist rate of 41.46/55.01dB is presented. The use of an integer-based split CDAC combined with an improvement for the LSB capacitor allows a substantial improvement in the SNDR. A simple and accurate calibration procedure for the ADC is presented thanks to back gate biasing. The ADC is designed in 22nm FDSOI while consuming 1.65mW from a 0.8V supply with a core chip area of 0.00074mm<sup>2</sup>. The Walden figure-of-merit of 19.5fJ/conversion-step at Nyquist rate making it one of the lowest among recently published medium resolution SAR ADCs.

**Keywords:** Analog-to-digital converter (ADC), low power, single channel, successive approximation register (SAR)

## 1 Introduction

The increasing demand of higher data rates in datacenters has led to new emerging standards (200-400G Ethernet and others) in wireline communications. These standards will favor more sophisticated encoding schemes that require less bandwidth such as the case of PAM4. Its encoding uses 4 levels and reduces the bandwidth by a factor of 2. But at the price to be harder to be supported by purely analog solutions. So, a natural shift towards multi-level signaling and mixed-signal architectures is expected.

ADC-based solutions give more opportunities for speed increase. They present more robust solutions over channels with high losses (>20dB) because they can take advantage of technology scaling and most of the equalization can be implemented in the digital domain [1, 2].

Such ADCs are implemented using time-interleaving: identical sub-ADCs multiplexed in time, operating in parallel to achieve a higher sampling rate [3]. A suitable sub-ADC should optimize the achievable speed, resolution, power performance and complexity [4–7]. Thus, research in this area is crucial for the next-generation of wireline communication systems.

This paper continues the works presented in [8, 9] on ADCs for high-speed wireline receivers. It explains the ADC-based receiver architecture using the speed requirements for future wireline communications standards. The ADC architecture selection is based on energy efficiency and the back gate biasing calibration.

As a result of the above, a very low-power 7-bit SAR ADC is been presented. It features: an improvement for the CDAC LSB capacitor is implemented to improve the SNDR, a simple and accurate calibration procedure for the comparator and ADC using back gate biasing. The circuit was designed using the 22FDX<sup>TM</sup> platform enabling a power efficient and flexible design.

Section II introduces the context of high-speed wireline receivers, the speed and modulation requirements for 100Gb/s operation. Section III presents the sub-ADC resolution estimation based on link budget analysis. Section IV highlights the ADC architecture selection from the energy efficiency comparison of two high-speed converters. In Section V, the circuit description is presented. Simulation results are shown in Section VI and Section VII draws the main conclusions from this work.

## 2 High-Speed Wireline Receivers

Today, all datacenter managers (e.g. Google, Facebook, Amazon, ...) have implemented 100 Gigabit Ethernet connectivity which consists of 4 parallel signals at 25Gb/s. The encoding of the signals is NRZ (binary modulation Non Return to Zero). The circuits in receivers and transmitters (optical or electrical) are well known and generally of an analog nature. The main disadvantage using this protocol is the high frequency bandwidth usage, especially up to (and even beyond) 12.5GHz.

For this reason, future standards for higher bitrate transmissions will abandon NRZ in favor of more sophisticated encodings that use less frequency bandwidth. The IEEE 802.3 Ethernet Workgroup is in charge to complete the standard by fall of 2021 under the denomination IEEE 802.3ck which consists of 100, 200, and 400GbE using 100Gb/s lanes [10].

The Optical Internetworking Forum (OIF), a non-profit consortium, is also working on the Common Electrical I/O (CEI) 112G standard, which targets 112Gb/s electrical interfaces. As data rate continues to increase, 112Gb/s over single lane is on the horizon. The feasibility certainly depends on the choice of signal modulation and channel characteristics.

4-level Pulse Amplitude Modulation (PAM4) is gaining more attention in recent years as an alternative coding scheme to NRZ. In NRZ signaling, one bit is a symbol and has two distinct amplitude levels of '0' or '1'. Symbols are expressed in terms of baud. NRZ bitrate is equal to its symbol rate where 1Gb/s is equal to 1Gbaud.

PAM4 signaling uses four different levels, where each level corresponds to one symbol representing two bits. With two bits per symbol, the baud rate is half the bitrate. For example, 56Gbaud PAM4 is equal to 112Gbaud NRZ (112Gb/s). As such, PAM4 achieves twice as much throughput using half the bandwidth compared to NRZ.

In standard linear PAM4 signaling, it is possible for two transitions to happen at the same time. These transitions can cause two-bit errors per symbol. If standard PAM4 signaling is converted to gray code, the Bit Error Rate (BER) is reduced to one-bit per symbol and the overall bit error rate is cut in half. BER can be expressed as a function of the signal-to-noise ratio (SNR) at the decision point. The use of PAM4 signaling brings many advantages to overcome the bandwidth limitations of NRZ, but also bring new challenges in link-path analysis.

As the link's speed requirements become more stringent, pure analog architectures cannot meet them. So, a natural shift towards mixed-signal architectures is expected. ADC-based receivers give more opportunities for speed augmentation because they constitute more robust solutions due to their digital nature and they scale well with process. The high density of lower processes will allow receivers relying heavily on digital signal processing (DSP) [11]. These receivers incorporate an ADC to digitize the received signal and perform equalization in the digital domain [8, 9]. A typical ADC-based receiver is shown in Figure 1.

### 3 sub-ADC Resolution Estimation

The resolution of the sub-ADC will be calculated using the BER at the output of the receiver (pre-FEC or raw BER). Figure 1 corresponds to the link budget of a realistic implementation for an ADC-based receiver.

The proposed sub-ADC is designed to meet the SNR requirements for 56 GBaud PAM4 signaling. Considering the same amplitude swing for NRZ and PAM4 encodings, the SNR in PAM4 is lower than NRZ. Forward error correction (FEC) is used to improve link integrity and counteract physical layer level errors introduced by reduced SNR in PAM4 signals [8, 9].

At 56 GBaud, the pre-FEC raw BER of  $< 10^{-4}$  is a typical target. In our design the receiver is designed to achieve BER=  $10^{-6}$  over a 30dB loss channel at 28GHz. We start from the output SNR (post-FEC BER=  $10^{-15}$ ) and work backwards from there.

$$\text{BER}_{\text{post,FEC}} = \left( \frac{M-1}{2M} \right) \times \text{erfc} \left( \sqrt{\frac{3 \cdot \text{SNR}}{2(M^2-1)}} \right) \quad (1)$$

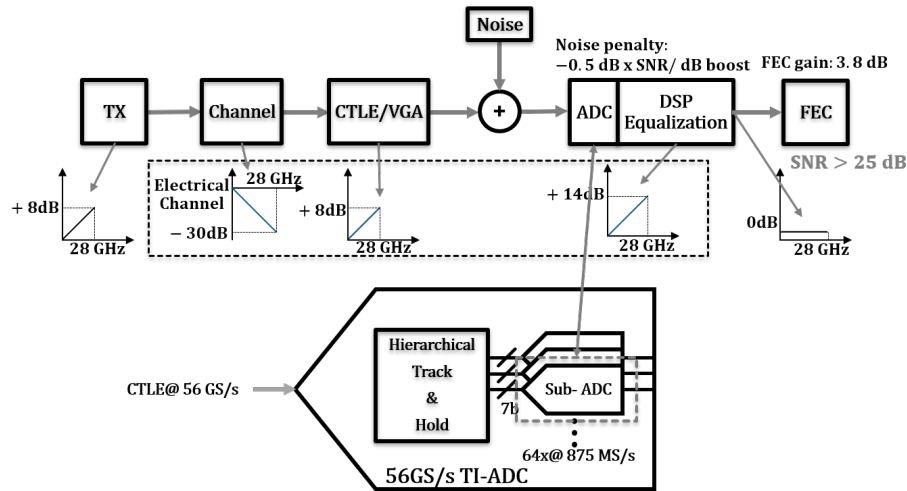


Fig. 1. sub-ADC in a Time Interleaved System

where is  $M=4$ , for PAM4 modulation and  $erfc$  is the complementary error function, which yields a  $\text{SNR} \approx 25\text{dB}$ .

For a FEC gain of  $3.8\text{dB}$ , the pre-FEC BER is

$$\underbrace{25\text{dB}}_{\text{BER}_{\text{post,FEC}}} - \underbrace{3.8\text{dB}}_{\text{Gain}_{\text{FEC}}} = \underbrace{21.2\text{dB}}_{\text{BER}_{\text{pre,FEC}} < 10^{-6}} \quad (2)$$

The DSP equalization boost is calculated as

$$\underbrace{30\text{dB}}_{\text{channel loss}} - \underbrace{8\text{dB}}_{\text{Tx}_{\text{gain}}} - \underbrace{8\text{dB}}_{\text{Rx}_{\text{gain}}} = 14\text{dB} \quad (3)$$

Considering a SNR noise penalty of  $-0.5\text{dB}$  per dB of DSP boost and a margin of  $6\text{dB}$ , the SNR requirement at the input of the ADC yields:

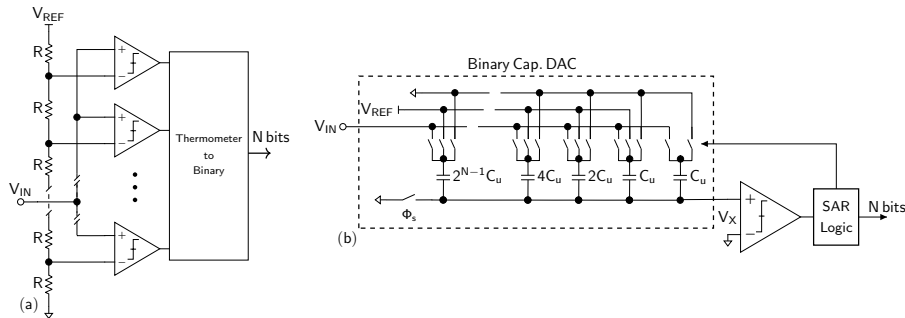
$$\text{SNR}_{\text{ADC}} = \underbrace{21.2\text{dB}}_{\text{BER}_{\text{pre,FEC}} < 10^{-6}} + \underbrace{14 \times 0.5\text{dB}}_{N_{\text{o,DSP}}} + \underbrace{6\text{dB}}_{\text{Margin}} = 34.2\text{dB} \quad (4)$$

which roughly corresponds to a resolution of  $\approx 5.4\text{b}$ . Our design targets a resolution of  $7\text{b}$  as a trade-off of speed and power for a single-channel ADC.

#### 4 sub-ADC architecture selection

A suitable sub-ADC architecture should not magnify the complexity and the achievable speed and resolution. The architecture selection was chosen from the energy efficiency comparison of two high-speed, medium-resolution converters: the flash ADC and SAR ADC.

An  $N$ -bit flash ADC is composed of  $2^N - 1$  comparators, a reference resistor ladder and a thermometer-to-binary encoder as shown in Figure 2(a). The reference resistor ladder and thermometer-to-binary encoder energies scale roughly as  $2^N$  but are usually less than the total comparator energy. For simplicity, the speed and structure of the



**Fig. 2.** (a) Flash ADC; (b) SAR ADC with binary-weighted capacitive DAC.

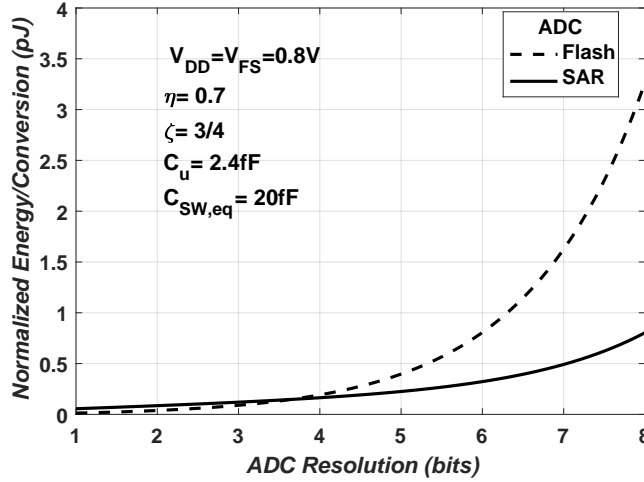


Fig. 3. Energy comparison between SAR and Flash ADCs as a function of resolution

comparators used in Flash and SAR ADC are assumed to be the same. Therefore, the energy per conversion for a flash ADC is

$$\begin{aligned} E_{\text{comp}} &= C_{\text{latch}} V_{\text{DD}}^2 \\ E_{\text{flash}} &= (2^N - 1) \cdot E_{\text{comp}}, \end{aligned} \quad (5)$$

where  $E_{\text{comp}}$  is the energy of a single comparator.  $C_{\text{latch}}$  and  $V_{\text{DD}}$  represent the total switched capacitance in the comparator's latch and supply voltage, respectively. A basic SAR ADC structure is shown in Figure 2(b). It consists of a comparator, a capacitive DAC and a SAR control logic. There are several switching schemes aiming to improve the energy efficiency in SAR ADCs [12]. For simplicity, the conventional switching scheme is used in this comparison. The energy per conversion of the comparator can be calculated similar to a flash ADC.

The capacitive DAC using the conventional switching scheme presents a total array energy for one conversion is

$$E_{\text{DAC}} = 2\eta^2 (1+1/2\zeta)^N \frac{C'_u}{2^{N'/2\zeta}} (V_{\text{DD}} V_{\text{FS}}), \quad (6)$$

where  $C'_u$  is the process-dependent unit capacitance required for matching to the  $N'$ -bit level and is assumed to be 2.4fF in 22FDX.  $V_{\text{FS}}$  is the ADC full scale, respectively. The  $\eta^3$  and  $\gamma^4$  coefficients represent the DAC energy dependence on the input-signal and capacitance mismatch, respectively. The total energy consumed by the switching of the

<sup>3</sup> $\eta=0.7$  is a reasonable approximation [13]

<sup>4</sup> $\gamma$  equals 3/4 or 1/2 if the mismatch is dominated by edge effects or oxide variation, respectively.

SAR logic over one conversion is

$$E_{\text{logic}} \approx N C_{\text{SW,eq}} V_{\text{DD}}^2. \quad (7)$$

where  $C_{\text{SW,eq}}$  is the total switched capacitance in the SAR logic normalized to 1-bit level. Summing the energy of the SAR blocks, the total energy per sample conversion yields

$$E_{\text{SAR}} = E_{\text{DAC}} + (N + 1) \cdot E_{\text{comp}} + E_{\text{logic}} \quad (8)$$

The total energy consumption of flash and SAR ADCs are compared versus a resolution range of 1 to 8 bits, as seen in Figure 3. At resolutions below 4 bits, a flash ADC presents lower energy compared to a SAR ADC. However, as the resolution increases the number of comparators in a flash ADC increases exponentially, while it increases linearly for a SAR ADC. Above a resolution of 6 bits, the energy efficiency of the SAR structure becomes more apparent. Based on this energy comparison, a SAR ADC is the better choice for 7-bit resolution, which is the target range for the proposed ADC-based receiver.

## 5 Circuit Description

This sub-ADC is designed as a building block inside a Time-Interleaved (TI) ADC. This TI-ADC is a 7-bit 56GSample/s with a Interleaved Sampler Ratio (ISR) of 64 [8], [9]. Thus, making the sub-ADC operates at 875MHz.

A very low-power 875 MS/s 7-bit SAR ADC that is suitable for integration into a TI-ADC is presented. The use of an integer-based split CDAC combined with an improvement for the LSB capacitor allows a substantial improvement in the SNDR. A simple and accurate calibration procedure for the ADC is presented thanks to back gate biasing.

The proposed SAR ADC uses asynchronous design to improve the speed conversion, an integer-based split capacitive DAC (CDAC) and the monotonic switching principle. Fig. 4a illustrates the top-level ADC architecture. The front-end T&H circuit consists of a sampling bootstrapped switch with feed-through and charge-injection compensation. The sampling clock ( $\Phi_{\text{s,ADC}}$ ), with a 25% duty cycle, drives the T&H and triggers the asynchronous internal conversion logic, which is responsible for generating the bit-cycle phases, controlling the comparator, storing its decisions and switching the CDAC.

The ADC comprises two identical 6b CDACs to accommodate differential operation. Since the MSB decision is the sign bit, it can be decided without changing the state of the CDAC. Thus, 6b CDAC, instead of 7b CDAC, is sufficient for this 7b SAR ADC design [14].

### 5.1 Capacitive DAC

The 6b CDAC, depicted in Fig. 4a, is based on an integer-based split capacitive DAC. The CDAC is divided in two sides: the lower side and the higher side of 2b and 4b,



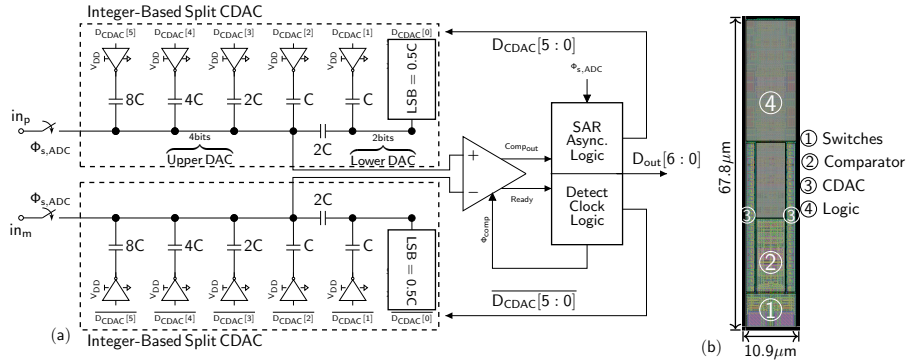


Fig. 4. (a) Architecture of the proposed single-channel 7b SAR ADC; (b) Layout

respectively. The split capacitor with a value  $2C$  ( $C$ =unit capacitor) is placed just after the smallest unit capacitor of the 4b array, thus avoiding the non-linearity issues found in the common split capacitor array [15]. In the lower side two variations for the LSB capacitor were evaluated, Fig. 5. Instead of switching a fraction of the unit capacitor ( $0.5C$ ) during the LSB conversion by the full difference of the reference voltage,  $V_{REF}=V_{DD}$ , a  $C$  unit capacitor is switched by a fraction of the reference voltage,  $V_{REF}=V_{DD}/2$ , which will be referred as  $LSB_1$ , [5]. And the other  $LSB_2$  is implemented switching two unit capacitors ( $1C$ ) in series by  $V_{REF}=V_{DD}$ .

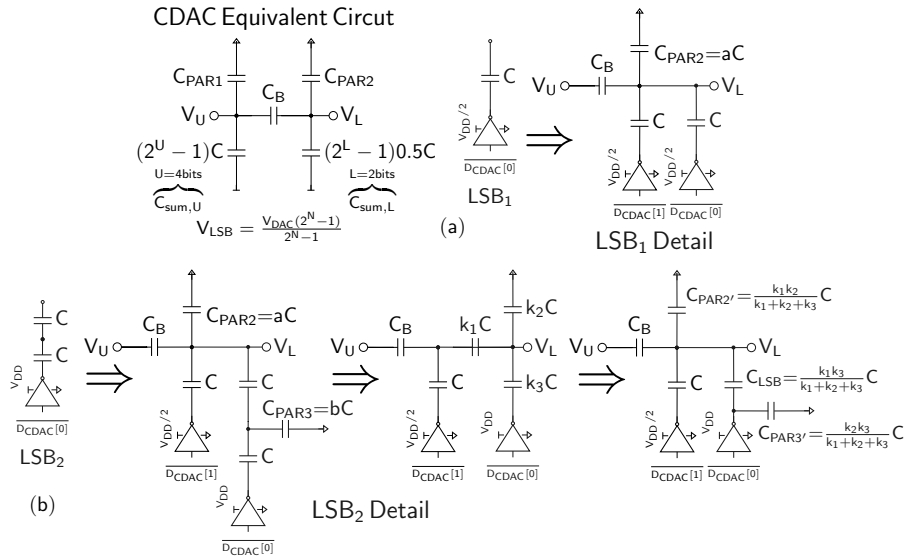


Fig. 5. LSB Capacitor Variation with parasitics: (a)  $LSB_1$ ; (b)  $LSB_2$

The unit capacitors of the CDAC are designed to achieve best area efficiency using alternate-polarity metal-finger capacitors (APMOM) which offer high density, good matching characteristics and low parasitics.

For this 7b SAR ADC, the total capacitance of this capacitor array is  $(2^{7-3}+3)C=19$ , [15]. A 70% area reduction compared to a conventional CDAC with monotonic switching is obtained, thus reducing settling time between conversion cycles and minimizing area and power consumption.

The designed one-side total capacitance is 45.6fF, which produces an equivalent  $kT/C$  thermal noise of  $301.4\mu\text{V}$ . The least significant bit (LSB) value for a 7b ADC at a reference voltage of 0.8V is 6.25mV so the thermal noise introduced by this capacitor array is not a limiting factor. Following the equivalent circuit shown in Fig. 5, the CDAC voltage ( $V_{\text{DAC}}$ ) and LSB voltage ( $V_{\text{LSB}}$ ) are

$$V_{\text{DAC}} = \frac{C_B(C_{\text{VREF}}^U + C_{\text{VREF}}^L) + C_{\text{VREF}}^U C_{\text{sum,L}}}{\text{den}} \cdot V_{\text{REF}} + \frac{C_{\text{VREF}}^U C_{\text{PAR2}}}{\text{den}} \cdot V_{\text{REF}} \quad (9)$$

$$V_{\text{LSB}} = \frac{V_{\text{DAC}}(2^N - 1)}{2^N - 1} = \frac{C_B(C_{\text{sum,U}} + C_{\text{sum,L}}) + C_{\text{sum,U}}C_{\text{sum,L}} + C_{\text{sum,U}}C_{\text{PAR2}}}{(2^N - 1)\text{den}} \cdot V_{\text{REF}} \quad (10)$$

where  $N=U+L$ ,  $\text{den}=(C_{\text{sum,U}}+C_{\text{PAR1}})(C_{\text{sum,L}}+C_{\text{PAR2}})+C_B(C_{\text{sum,U}}+C_{\text{sum,L}}+C_{\text{PAR1}}+C_{\text{PAR2}})$ ,  $C_B=2C$ .  $C_{\text{sum,U-L}}$  and  $C_{\text{VREF}}^{U-L}$  denotes the total capacitance and total capacitors connected to  $V_{\text{REF}}$  in the Upper and lower DACs, respectively.

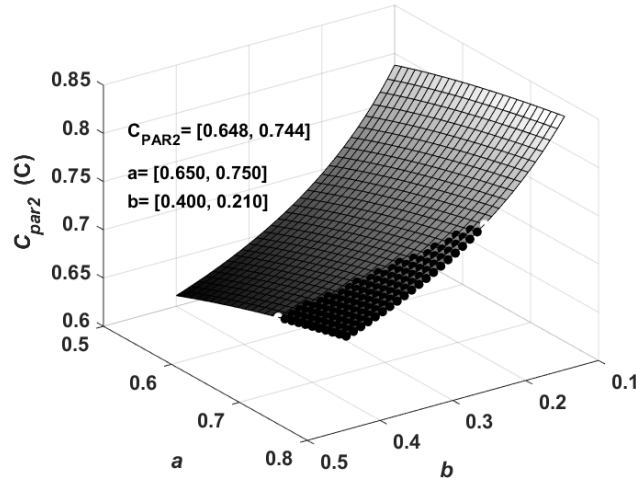


Fig. 6.  $C_{\text{PAR2}}$  grid for a,b values

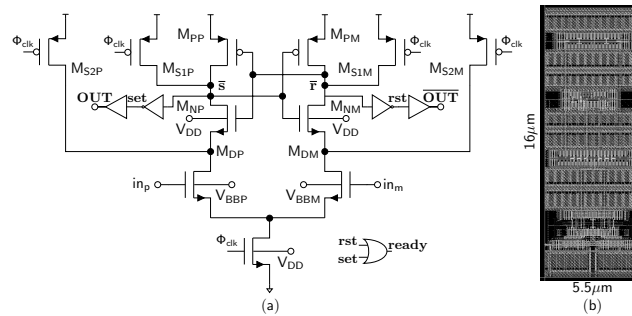
The parasitic capacitance  $C_{PAR2}$  in the numerator of Eq. 10 contributes to a code dependent error, degrading the DAC linearity [16].  $C_{PAR2}$  is defined by the total parasitic capacitance of the top plates in the Lower CDAC and the metal interconnection. Fig. 5a shows the Lower DAC section for the  $LSB_1$  capacitor.  $C_{PAR2}$  is denoted as a fraction of the unit capacitor (aC), for this condition the  $V_{LSB}$  error can be reduced by minimizing  $C_{PAR2}$  contribution.

In Fig. 5b it is shown a variation of LSB capacitor ( $LSB_2$ ) to reduce the  $V_{LSB}$  error.  $C_{PAR2}$  is the same as in  $LSB_1$ , but with the addition of  $C_{PAR3}$  as the parasitic capacitance of the bottom plates of the two unit capacitors in series.  $C_{PAR3}$  is represented as a fraction of of the unit capacitor (bC). Through a delta-star transformation  $LSB_2$  is shaped with the same arrangement as for  $LSB_1$ . Fig. 6 shows the new values of  $C_{PAR2}$  and  $C_{LSB}$ . A range for  $C_{PAR3}$  between  $[0.21 \ 0.4]C$  yields the reduction of  $C_{LSB}$  and  $C_{PAR2}$  simultaneously. In 22nm FDSOI, the APMOM capacitors present a parasitic  $\approx 0.13C$  per capacitor yielding a value of b around 0.26.

## 5.2 Comparator and Back gate biasing calibration

Since the comparator determines the accuracy and speed of the ADC, special care has to be taken for its design [17]. A strong-ARM comparator is chosen for its superior decision speed enabled by the single-stage design. It is optimized for low noise and low power. Fig. 7a shows the schematic, the latch regeneration forces one of the signals, *rst* and *set*, to high and the other to low, depending on the comparison result. As a result, the output of the OR gate (*ready*) is pulled high to enable the asynchronous control clock and to facilitate the progression to the next step in the SAR conversion.

The offset voltage  $V_{OS}$  introduced by the input differential pair is calibrated using a simple and accurate procedure. The calibration operates in two phases:  $V_{OS}$  extraction and  $V_{OS}$  calibration. The offset extraction is a fast loop operating at the comparator's clock frequency  $\Phi_{CLK}$  and follows the smart resettable SAR (SR-SAR) technique presented in [18]. The SR-SAR technique is proposed as a fast and accurate alternative to the conventional linear search technique, which is simple and accurate but suffers from long simulation time. The SR-SAR uses a modified SAR algorithm to determine the comparator offset voltage in a much shorter time. The input of the comparator is



**Fig. 7.** Strong ARM Comparator: (a) Schematic; (b) Layout

modified to provide a quasi-monotonic stimulus. It allows a well defined crossing from low-to-high and high-to-low transitions. It yields to an accurate extraction of the rising offset ( $V_{OSR}$ ) and falling offset ( $V_{OSF}$ ) voltages.

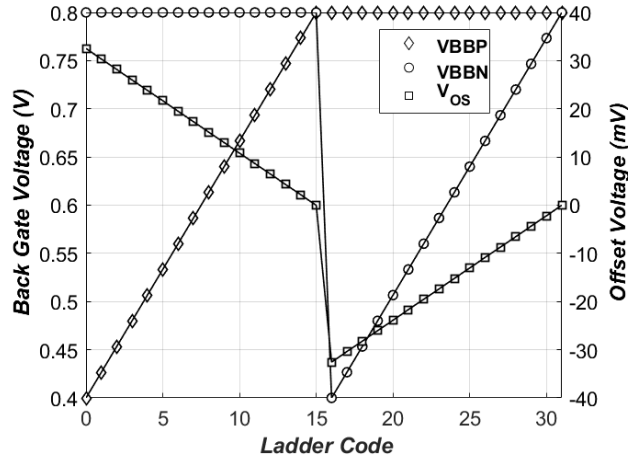
The second phase is a slow loop (below 1 MHz), due to the low frequency nature of the transistor's back gate. After extracting the  $V_{OS}$ , the control block begins to adjust the threshold voltages ( $V_{TH}$ ) of the differential pair through a back gate biasing DAC until  $V_{OS} \approx 0$  or a margin is reached.

The back gate biasing DAC consists of a resistor ladder controlled by a 5-bit digital word. In order to choose the variation range of the ladder, we need to extract the  $V_{OS}$  range of the comparator. Using Monte-Carlo (MC) simulations from the schematic, a  $V_{OS}$  range ( $\pm 3\sigma$ ) of  $\approx 45\text{mV}$  was obtained for the nominal clock frequency of 875MHz.

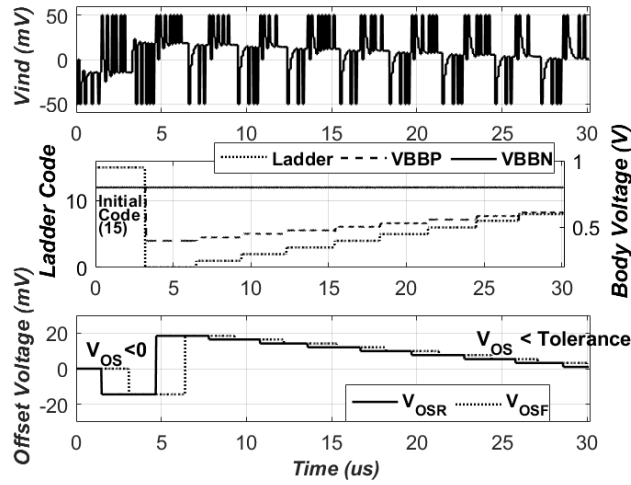
The nominal voltage supply for the comparator is 0.8V, the same for the back gate bias at nominal operation. In Fig. 8 is shown the back gate bias control. The ladder was designed using a resolution of 5bits, with the back gate voltage varying between 0.4 to 0.8V. An artificial offset voltage range of  $\pm 32\text{mV}$  ( $\approx 2.1\text{mV}$  steps) was created. For example if a negative  $V_{OS}$  is extracted, the calibration controller will only choose from the positive range to counterbalanced the negative  $V_{OS}$  generated by the differential pair.

The  $V_{OS}$  calibration for the comparator consists of two phases:

1.  $V_{OS}$  extraction:
  - It begins with initialization of the back gate biasing DAC, ladder code= 15  $\rightarrow$   $V_{BBP} = V_{BBN} = 0.8\text{V}$ ,
  - After initialization  $V_{OSR}$  and  $V_{OSF}$  are extracted.
2.  $V_{OS}$  calibration:
  - $V_{OSR}$  and  $V_{OSF}$  determine the iteration sequence for the ladder with  $V_{OS,init} = V_{OSR} = V_{OSF}$ ,



**Fig. 8.** Back gate biasing DAC: back gate bias and offset voltage



**Fig. 9.** Back gate biasing calibration procedure showing: input differential voltage ( $V_{ind}$ ), DAC ladder code, DAC back gate voltage and offset voltage ( $V_{OS}$ )

**Table 1.** Post-Layout  $V_{OS}$  Calibration.

Search range	-50 to 50mV	
Resolution	0.1mV (10 bits)	
$\Phi_{CLK}$	10MHz	
	Uncalibrated	Calibrated
Mean ( $V_{OS}$ )	-1.61mV	0.02mV
$\sigma$ ( $V_{OS}$ )	8.86mV	0.73mV

- For  $V_{OS,init} < 0$ , the ladder will add a positive  $V_{OS,iter}[code] > 0$ , with the code starting at 0. For  $V_{OS,init} > 0$ , the code starts at 16 ( $V_{OS,iter}[code] < 0$ ).
- The body-bias are switched to the current code value:  $V_{BBP}[code]$ ,  $V_{BBN}[code]$  and  $V_{OS,iter}[code]$  is extracted,
- The iteration sequence continues until  $V_{OS,iter}[code] < tolerance$ , i.e. 1mV or the code reaches its final value.

Fig. 9 shows the time diagram of the comparator's  $V_{OS}$  calibration sequence for  $V_{OS,init} < 0$ . The code transitions had a time step of  $2.5\mu s$  and the comparator is clocked at 10MHz ( $T=100ns$ ). By clocking the comparator at low frequency, the time step of the transient simulation is coarse enough to allow a much faster convergence solution.

To evaluate the proposed calibration methodology, MC Post-Layout Simulations (PLS) were performed on the comparator using the same search range and resolution for  $V_{OS}$  extraction. Fig. 10 shows the histogram of  $V_{OS}$  for 100 MC runs for an un-

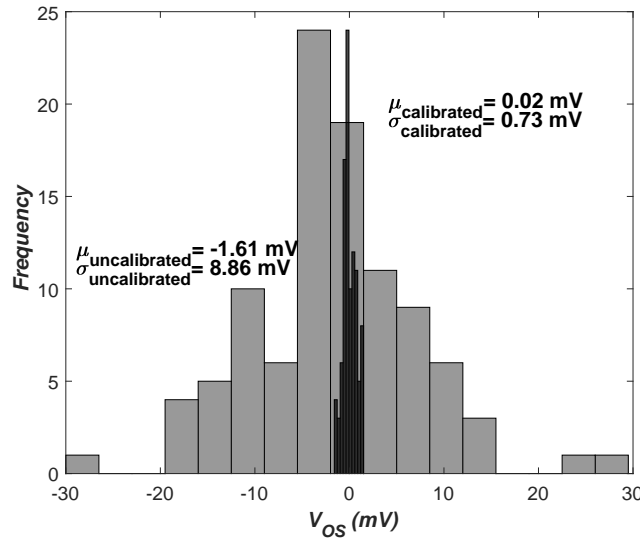


Fig. 10. Histogram Strong ARM  $V_{OS}$ : Uncalibrated, Calibrated for 100 MC runs

calibrated and calibrated comparator. It clearly stands out the  $V_{OS}$  mean and standard deviation reduction for the calibrated comparator. Another aspect to point out is the larger  $V_{OS}$  of the uncalibrated version, but this did not present any issues since the resistor ladder was designed with some margin. Table 1 summarizes the MC results. The  $V_{OS}$  mean was almost zeroed and the standard deviation was reduced by a factor of 12.

### 5.3 SAR Logic

Besides the advantage of faster bit-cycle conversion, an additional benefit of asynchronous SAR logic is that it does not require an external high-frequency clock, and thus saves the power needed to generate and distribute it. This is extremely important, since this ADC will be part of a time-interleaved system.

The logic of the SAR ADC can be divided into two parts: 1) the clock generation, which provides the clock for the comparator and the bit-cycle phases and 2) the state memory, in charge of controlling the CDAC based on the comparator decision in each of the bit-cycle phases, Fig. 11. The Track duration is set at 25% of the 875MHz clock period.

The clock generation combines the clock  $\Phi_{ADC}$ , ready and  $\text{stop}_{\text{cycle}}$  signals to generate the comparator clock ( $\Phi_{\text{Comp}}$ ) and bit-cycle clocks ( $\text{CLK}_{p,n}$ ) with simple combinational logic. At the same time, a sampling *pulse* is generated from  $\overline{\Phi_{ADC}}$  and its delay. This *pulse* propagates sequentially, as controlled by the  $\text{CLK}_{p,n}$  signals, generating each of the bit-cycle phases, Fig. 11. The Track duration is set at 25% of the 875 MHz clock period. Additionally, the  $\text{stop}_{\text{cycle}}$  signal is used to indicate the end of the conversion cycle.

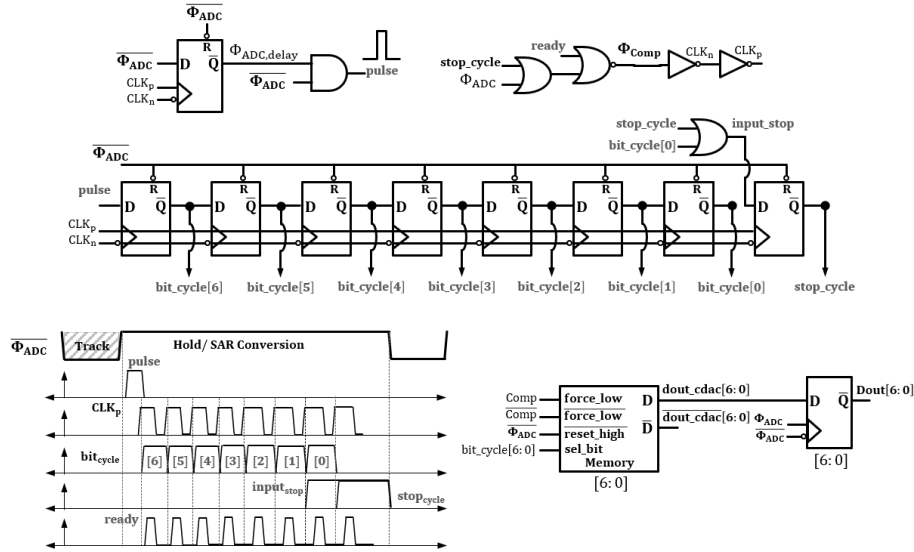


Fig. 11. SAR Logic and timing

The state memory part connects directly to the differential output of the comparator. A dynamic register is used as memory to optimize loop delay and enable fast settling upon comparator decision. One cell is activated during every comparison by its corresponding  $bit\_cycle[i]$  and provides  $Dout_{CDAC}$  and  $\overline{Dout}_{CDAC}$  as control signals for the CDAC. Finally,  $Dout_{CDAC}$  is retimed by  $\Phi_{ADC}$  to create the output data.

## 6 Simulation Results

This circuit has been designed using the 22FDX<sup>TM</sup> platform in 22nm FDSOI CMOS of GLOBALFOUNDRIES, [19]. One of the most differentiated features of the 22FDX platform is the capability of effective back gate biasing. Back gate biasing applies a positive or a negative voltage to the back gate of the transistor, which allows the transistor  $V_{TH}$  to be tuned, and can be done statistically or dynamically.

The nominal full-scale ADC input is  $800mV_{pp,diff}$  with a common mode of 400mV. It operates from a core 0.8 V supply and simulated, under typical conditions. Power consumption is 1.65mW based on PLS results at 875MS/s. This overall power consists of  $80\mu W$  for the bootstrapped input switch,  $40\mu W$  for the CDAC, 0.68 mW for the comparator and 0.85mW for the phase and SAR logic, as seen in Figure 12.

Although, the calibration for the comparator was implemented to extract the  $V_{OS}$ , it can also be used to calibrate the ADC. Fig. 13 shows the MC simulation results, the ADC was calibrated at the middle of the range (64LSB) and a 4x reduction of the output code  $\sigma$  was achieved. It is worth to mention that the limiting factor for the ADC calibration is the resolution,  $LSB=6.25mV$  (7 bits).

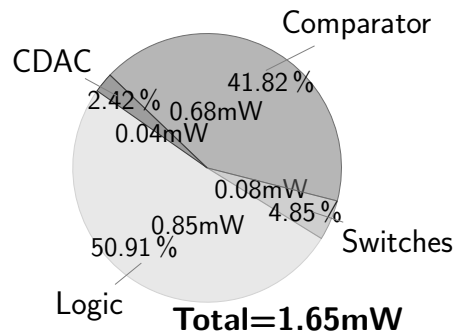


Fig. 12. sub-ADC power consumption breakdown

It is worth to mention, that the calibration procedure for the comparator and ADC was performed at low frequency, due to the time step of the transient simulation is coarse enough to allow a much faster convergence solution. For that reason, the results for static and dynamic characteristics shown are just for nominal conditions without calibration.

The simulated DNL and INL results at 875MS/s for a ramp up input for the two LSB capacitor versions are depicted in Fig. 14. It can be seen that the second version (LSB<sub>2</sub>) is more robust to implement the LSB capacitor of the lower side of the differential DAC. LSB<sub>2</sub> presents a DNL within 1.08/-0.51LSB, and the INL within -0.78/+0.6LSB.

The output spectrum at 428.96MHz input frequency is shown in Fig. 15. The ADC achieves a SNDR/SFDR of 41.46/55.01dB at Nyquist frequency for the LSB<sub>2</sub> ver-

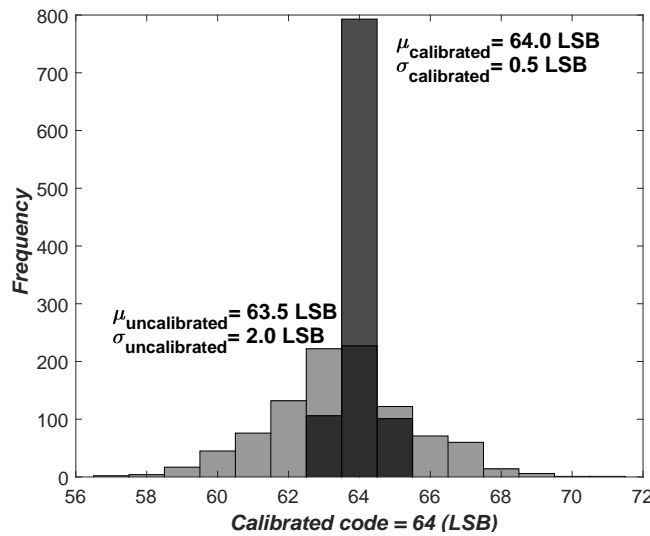


Fig. 13. Histogram of ADC Output Code: Uncalibrated, Calibrated for 1000 MC runs



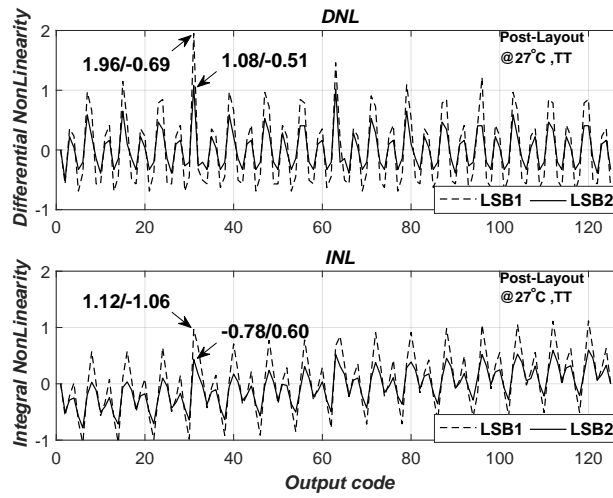


Fig. 14. DNL and INL. LSB<sub>1</sub> (dashed); LSB<sub>2</sub> (solid)

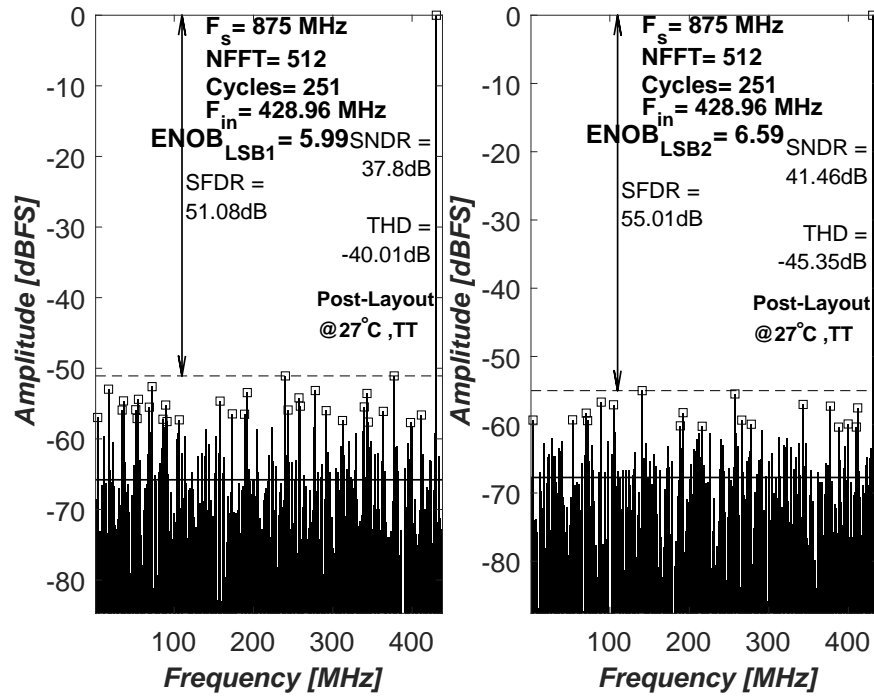


Fig. 15. Output Spectrum with 0 dBFS signal applied at 428.96 MHz, sampling frequency is 875 MHz. LSB<sub>1</sub> (left); LSB<sub>2</sub> (right)

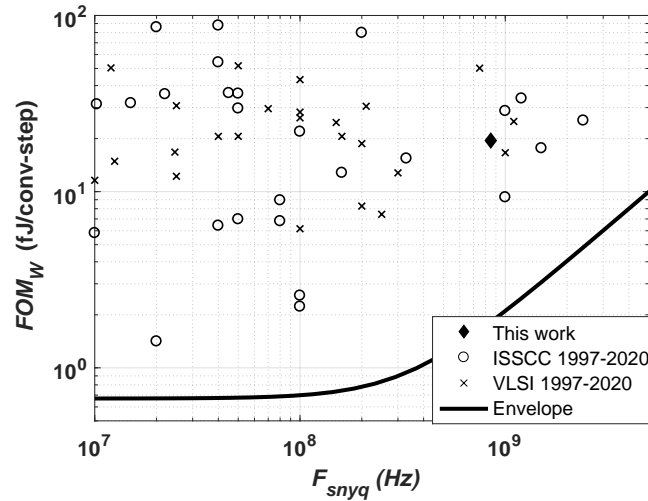
**Table 2.** Performance Summary and Comparison with Single-Channel State-of-the-Art SAR ADCs

	This Work*	[7] <sup>+</sup>	[4] <sup>+</sup>	[5] <sup>+</sup>	[6] <sup>+</sup>
Technology [nm]	22nm FDSOI	28nm CMOS	65nm CMOS	32nm SOI	40nm CMOS
Architecture	SAR	SAR	2b/c SAR	2 comp. SAR	ci-SAR
Calibration	YES	NO	YES	YES	YES
Resolution [bits]	7	7	8	8	6
Supply [Volts]	0.8	1.0	1.2	1.0	1.0
Samplig Rate [GS/s]	0.875	1.25	0.4	1.2	1
Power Consumption [mW]	1.65	3.56	4.0	3.1	1.26
Active Area [mm <sup>2</sup> ]	0.00074	0.0071	0.024	0.0031	0.00058
SFDR@ Nyq. [dB]	55.01	52	53	49.8	49.7
SNDR@ Nyq. [dB]	41.46	40.1	40.4	39.3	34.6
FoM@Nyq. [fJ/conv-step]	19.5	34.4	116.9	34	28.7

<sup>+</sup> Measured; \* Post Layout

sion, presenting an overall improvement of 0.6ENOB with respect to the LSB<sub>1</sub> version, showing the advantage of the proposed modification for the LSB capacitor.

Table 2 shows a performance summary and comparison with recent state-of-the-art SAR ADCs of similar performance, Fig. 16. The presented ADC achieves a comparable SNDR and lower FoM for a similar sampling rate (between 400MS/s  $\leftrightarrow$  1.25GS/s) and resolution (6-8b) while having a lower complexity and a smaller area.

**Fig. 16.** Comparison with state-of-the-art single-channel SAR based on [20]

## 7 Conclusion

A 7b 875MS/s single-channel SAR ADC has been presented. The integer-based split CDAC combined with an improvement for the LSB capacitor allows a substantial improvement in the SNDR. A simple and accurate calibration procedure for the ADC is presented thanks to back gate biasing. The use of a dynamic register in the SAR logic yields a shorter and more uniform settling time per cycle and therefore a faster ADC. The circuit in 22nm FDSOI achieves a Nyquist Walden FoM of 19.5fJ/conversion-step, which is the lowest FoM among previously medium resolution ( $5.5 \Leftrightarrow 7.5\text{ENOB}$ ) SAR ADCs with sampling rates greater than 0.8GS/s/channel.

## Acknowledgment

The authors thank the MACOM High-Performance-Analog design team for contributing to the circuit design and GLOBALFOUNDRIES for technology access.

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