# Reliability Enhanced Digital Low-Dropout Regulator with Improved Transient Performance

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**Abstract.** Digital low-dropout voltage regulators (DLDOs) have drawn increasing attention for the easy implementation within nanoscale devices. Despite their various benefits over analog LDOs, disadvantages may arise in the form of bias temperature instability (BTI) induced performance degradation. In this Chapter, conventional DLDO operation and BTI effects are explained. Reliability enhanced DLDO topologies with performance improvement for both steady-state and transient operations are discussed. DLDOs with adaptive gain scaling (AGS) technique, where the number of power transistors that are turned on/off per clock cycle changes dynamically according to load current conditions, have not been explored in view of reliability concerns. As the benefits of AGS technique can be promising regarding DLDO transient performance improvement, a simple and effective reliability aware AGS technique with a steady-state capture feature is proposed in this work. AGS senses the steady-state output of a DLDO and reduces the gain to the minimum value to obtain a stable output voltage. Moreover, a novel unidirectional barrel shifter is proposed to reduce the aging effect of the DLDO. This unidirectional barrel shifter evenly distributes the load among DLDO output stages to obtain a longer lifetime. The benefits of the proposed techniques are explored and highlighted through extensive simulations. The proposed techniques also have negligible power and area overhead. NBTI-aware design with AGS can reduce the transient response time by 59.5% as compared to aging unaware conventional DLDO and mitigate the aging effect by up to 33%.

**Keywords:** NBTI, reliability, aging, steady state performance, transient performance, shift register, unidirectional control

## 1 Introduction

Semiconductor technology that enables rapid advancements in the design and fabrication of nanoscale integrated circuits continuously improves while demanding a higher amount of power per unit area [1]. Integrating voltage regulators fully on-chip to provide robust power to the integrated circuits have been a challenging design issue. Several techniques have been proposed in the literature to improve the power conversion efficiency, stability, and reliability of on-chip voltage regulators or power delivery networks as a whole [2–14]. There is

also an emerging trend to leverage voltage regulators to address security concerns [15–23]. In addition to the existing challenges, bias temperature instability (BTI) induced reliability concerns have recently drawn attention especially for digital low-dropout regulators (DLDOs) [24–27]. Modern computing systems and internet of things (IoT) devices require reliable operation and long lifetime of on-chip voltage regulators [25,29,30]. Generating and delivering a robust output voltage under highly dynamic workload conditions have become even more difficult with the variations in the environmental conditions. These environmental conditions deteriorate the performance and lifetime of the transistors. Voltage regulators suffer from the abrupt variations in the workload and may experience serious aging phenomenon, necessitating reliability aware designs [25].

Transistor aging mechanisms such as BTI, hot carrier injection, and time-dependent dielectric breakdown have become more important with the scaling of transistor size. BTI is the major aging mechanism [31–37] where negative BTI (NBTI) induces performance degradation of PMOS transistors. Various studies have been performed to address the reliability issues of semiconductor devices [28,38,39]. BTI-aware sleep transistor sizing algorithms for reliable power gating design [38], integral impact of BTI and PVT variation [40], and impact of BTI variations [41] have been investigated. A conventional DLDO has a bi-directional controller which activates certain transistors frequently and leaves the others unused. This reliability unaware control scheme makes the performance degradation even worse because the activation pattern of PMOS is concentrated on certain transistors, thus causing heavy electrical stress on these transistors. The over usage of certain transistors degrades the performance significantly. Distributing the electrical stress among all of the transistors can therefore be effective. The primary literature that address the aging effects of on-chip DLDOs include a reliable digitally synthesizable linear drop-out regulator design, a digitally controlled linear regulator for per-core wide-range DVFS of Atom$^{TM}$ cores, and mitigation of NBTI induced performance degradation in on-chip DLDOs [25, 42, 43]. To evenly distribute the workload, a decoding algorithm for DLDO is proposed in [42]. A code roaming algorithm with per-core dynamic voltage and frequency scaling method is proposed in [43]. These techniques need dedicated control algorithms to enhance the reliability of a DLDO. A unidirectional shifter is proposed for conventional DLDOs in [25] to decrease the electrical stress on transistors. A DLDO without AGS, however, suffers from slow response time when there are large transitions in the load current. The supply voltage should be robust as the operation of all of the on-chip devices are sensitive to the variations at the output of the voltage regulators. Transient performance enhancements and loop stability can be increased by utilizing a barrel shifter as discussed in [44]. A barrel shifter which can perform the switching of two or three transistors within a single clock cycle improves the transient response time significantly. A barrel shifter based DLDO design with a steady load current estimator and dynamic gain scaling control is discussed in [45]. Although there are benefits of the aforementioned techniques, a DLDO with AGS still suffers from performance degradation due to NBTI. Additionally, a conven-

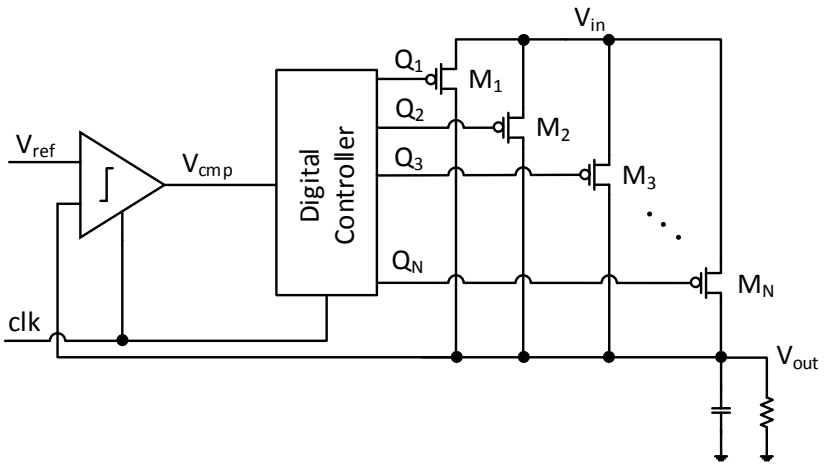



**Fig. 1.** Schematic of conventional DLDO.

tional DLDO with AGS also does not consider aging effect. Gain scaling using a bi-directional barrel shifter in [46, 47] may not be directly applicable to add gain scaling capability for a reliability enhanced DLDO. Therefore, further research should be performed on AGS DLDO to mitigate performance degradation due to NBTI. A novel aging aware DLDO with AGS and a steady-state detection circuit to obtain fast transient response under abrupt changes in the load current is proposed in this work.

The main contributions of this work are threefold. First, an NBTI-aware DLDO with AGS is proposed. Second, a simple and effective steady state, overshoot, and undershoot detection circuit is proposed and verified. Third, extensive simulations verify that the proposed circuit works effectively.

As an extension of [48], the rest of this Chapter is organized as follows. Background information regarding conventional DLDOs, steady state and transient performance of DLDO, and BTI is discussed in Section 2. Existing NBTI-aware DLDO topologies are explained in Section 3. The proposed NBTI-aware DLDO with AGS is discussed in Section 4. Evaluation of the proposed technique and simulation results are discussed in Section 5. Concluding remarks are given in Section 6.

## 2 Background

In this section, background information on the design of conventional DLDO, steady state performance and transient performance thereof, and BTI effects are explained.

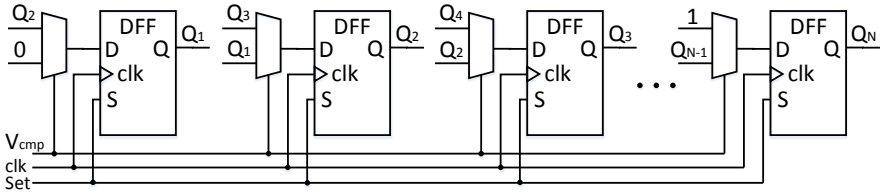



**Fig. 2.** Schematic of bidirectional shift register [25, 29].

| $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ | ... | ... | $Q_{N-1}$ | $Q_N$ |
|---|---|---|---|---|---|---|---|---|---|---|
| (1) Initialize: all $M_i$s turned off | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | ... | ... | 1 | 1 |
| (2) Step k | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | ... | ... | 1 | 1 |
| (3-a) Step k+1, if Vcmp is High: Shift right ➡ | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | ... | ... | 1 | 1 |
| (3-b) Step k+1, if Vcmp is Low: Shift left ⬅ | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | ... | ... | 1 | 1 |

**Fig. 3.** Operation of bi-directional shift register.

### 2.1 Conventional DLDO

The schematic of a conventional DLDO [29] is illustrated in Fig. 1. The $V_{ref}$ and $clk$ are the inputs and $V_{out}$ is the output of the conventional DLDO. The schematic and the operation principle of a bi-directional shift register used in the conventional DLDO are described in Figs. 2 and 3, respectively. The bi-directional shift register consists of a multiplexer and a DFF in each stage. The digital controller modulates the value $Q_i$ based on Fig. 3. The DLDO is composed of $N$ parallel PMOS transistors and a feedback control to adjust the output voltage. A bi-directional shift register is implemented in conventional DLDOs. $M_i$ is the $i^{th}$ PMOS and $Q_i$ is the logic output of the digital controller. $i$ denotes the activation stage of the digital controller. The bi-directional shift register switches the state of one of the power transistors according to $V_{cmp}$ at rising edge of each clock cycle. $Q_N$ is the $N^{th}$ output signal of the digital controller, as shown in Fig. 1. At step $k+1$, $Q_{n+1}$ ($Q_n$) is turned on (off) when $V_{cmp}$ is high (low) and the bi-directional shift register shifts right (left), as shown in Fig. 3 where $k$ is the activation step of the digital controller [25]. Each $M_n$ is connected to $Q_n$. Since the activation scheme is bi-directional, this scheme leads to heavy usage of $M_1$ to $M_n$. DLDO performance degradation can occur due to this power transistor activation and deactivation scheme as discussed in Sections 2.3 and 2.4.

### 2.2 Bias Temperature Instability

BTI includes NBTI for PMOS transistors and positive BTI (PBTI) for NMOS transistors. BTI leads to the increase of transistor threshold voltage $|V_{th}|$. NBTI increases the $|V_{th}|$ of PMOS transistors utilized in the DLDO power transistor array, leading to slower response time and the decrease of load supply capacity of the DLDO. The increase in $|V_{th}|$ is related to the traps generated in $Si/SiO_2$ interface at the gate when there is a negative gate voltage [49]. $\Delta V_{th}$ formula is given in (1) where $C_{ox}$, $k$, $T$, $\alpha$, and $t$ are the oxide capacitance, Boltzmann Constant, temperature, fraction of time when the transistor is under stress, and time, respectively. $K_{lt}$ and $E_a$ are the fitting parameters to comply with the experimental data [50].

$$\Delta V_{th} = K_{lt}\sqrt{C_{ox}(|V_{gs}| - |V_{th}|)}e^{-E_a/kT}(\alpha t)^{1/6} \tag{1}$$

Considering the case of DLDOs, most practical applications need less than average power, which leads to heavy utilization of certain transistors within conventional DLDOs. The undamped voltage output of DLDO causes large swings at the voltage waveform which leads to heavy use of certain transistors. The operation of the regulator causes the heavy use of $M_1$ to $M_m$ and less or even no use of $M_{m+1}$ to $M_N$. Alternatively, certain transistors (*i.e.*, the ones with a lower index number) are almost always active whereas some other transistors (*i.e.*, the ones with a greater index number) are almost never active. This activation scheme therefore induces serious non-symmetric degradation of PMOS due to NBTI.

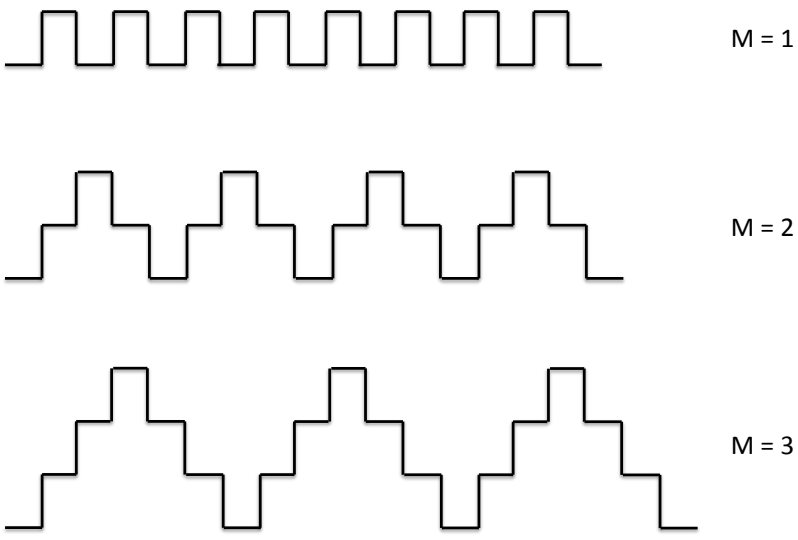



**Fig. 4.** Illustration of DLDO limit cycle oscillation mode.

### 2.3 Steady State Performance of DLDO

Under a constant load current, DLDO reaches steady state operation as $V_{out}$ approaches $V_{ref}$. Due to the discrete nature of digital control loop and the corresponding quantization error, limit cycle oscillation occurs during DLDO steady state operation, which negatively affects output voltage ripple. The mode of limit cycle oscillation $M$ can be indentified through the output of bidirectional shift register $Q(t)$ as shown in Fig. 4. The period of limit cycle oscillation (LCO) is $2MT_{clk}$, where $T_{clk}$ is the clock period. Under a certain $f_{clk}$, a larger LCO mode typically leads to a larger amplitude of output voltage ripple. LCO mode and output voltage ripple amplitude are largely affected by the unit current provided by each power transistor, load capacitance, clock frequency, and load current [51–54]. As NBTI can introduce PMOS $|V_{th}|$ degradation, it can be also detrimental to the existing LCO mitigation technique detailed in Section 3.

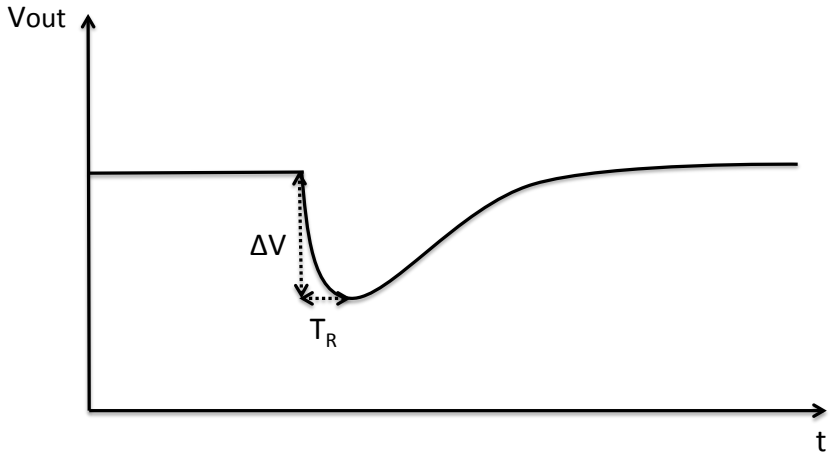



**Fig. 5.** Illustration of DLDO transient response.

### 2.4 Transient Performance of DLDO

Transient performance of a DLDO largely affects important application domains such as dynamic voltage and frequency scaling (DVFS) and near-threshold computing (NTC). A typical DLDO transient response is illustrated in Fig. 5. When the load current of the DLDO increases, the DLDO output voltage $V_{out}$ decreases to $V_{out} - \Delta V$ before recovering, where $\Delta V$ is the magnitude of the transient voltage droop and $T_R$ is the load response time. Smaller values of $\Delta V$ and $T_R$ are desirable for better DLDO transient performance. $\Delta V$ and $T_R$ can be, respectively, expressed as [25, 55–58]

$$\Delta V = R\Delta i_{load} - I_{pMOS} f_{clk} R^2 C ln(1 + \frac{\Delta i_{load}}{I_{pMOS} f_{clk} RC}). \quad (2)$$

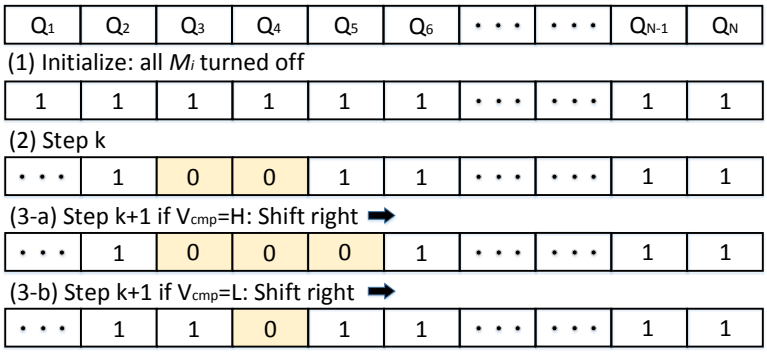



**Fig. 6.** Operation of the uni-directional shift register [25].

and

$$T_R = RCln(1 + \frac{\Delta i_{load}}{I_{pMOS} f_{clk} RC}) \tag{3}$$

where $I_{pMOS}$, $\Delta i_{load}$, $C$, and $R$ are, respectively, the current provided by a single active power transistor, load current change, load capacitance, and average DLDO output resistance before and after load current change. Due to the NBTI induced $|V_{th}|$ degradation, it is demonstrated in [25] that $\Delta V$ and $T_R$ also degrade. Such DLDO performance degradation needs to be considered when designing voltage regulators with a stringent lifetime requirement [59–61].

## 3 NBTI-Aware Digital Low-Dropout Regulators

Multiple NBTI-aware DLDO topologies have been proposed to mitigate steady state and transient performance degradation [24–26, 39]. The working principles of these techniques are explained in this section.

### 3.1 NBTI-Aware DLDO with Unidirectional Shift Register

As illustrated in Fig. 3, the operation of a bi-directional shift register leads to the heavy usage of the first few power transistors, which essentially increases activity factor of these transistors and the corresponding $|V_{th}|$ degradation. To mitigate this side effect, NBTI-aware DLDO with a unidirectional shift register control is proposed in [25, 62]. With minor changes of the control logic in each stage, the power transistor activation and deactivation can be realized in the same direction. In such a way, activity factor of each power transistor can be effectively reduced and the resulting DLDO performance degradation can be mitigated. Furthermore, the power and area overhead of the implementation are negligible.

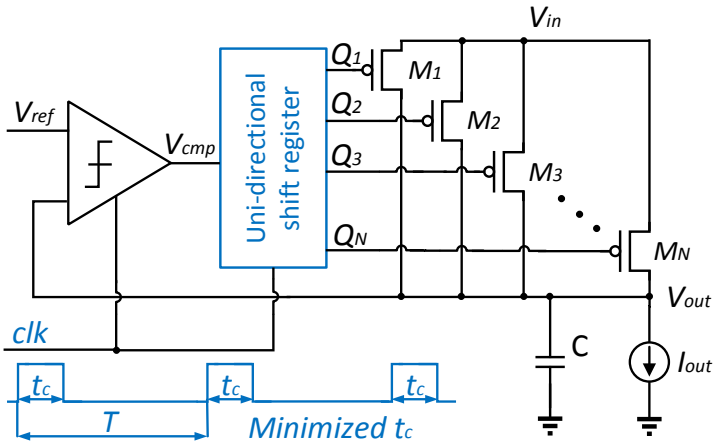



**Fig. 7.** Schematic of reduced clock pulse width DLDO [24].

### 3.2 Reduced Clock Pulse Width DLDO

During steady state operation, the LCO can be an issue for DLDO as it affects the amplitude of the output voltage ripple. It is demonstrated in [24] that BTI induced threshold voltage degradation can lead to the propagation delay degradation of the clocked comparator and shift register. Such delay degradation has a negative effect on the possible mode of LCO. Reduced clock pulse width DLDO as shown in Fig. 7 is proposed in [24] to mitigate the side effects of LCO. Minimum clock pulse width $t_c$ considering BTI induced propagation delay degradation is adopted and a uni-directional shift register is utilized to simultaneously improve steady state and transient performance of DLDO.

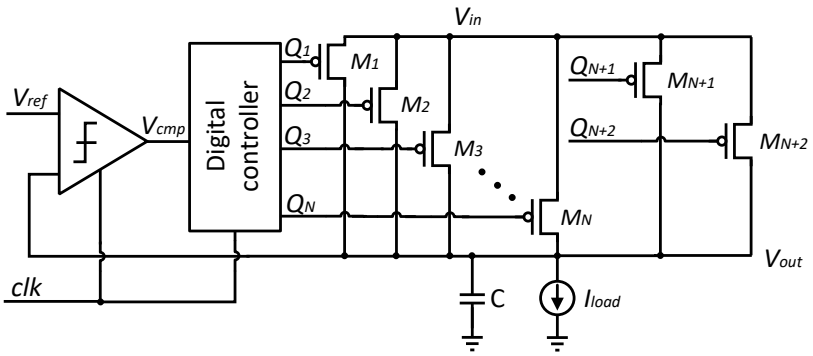



**Fig. 8.** Schematic of NBTI-aware DLDO with LCO mitigation [39].

### 3.3 NBTI-Aware DLDO with Limit Cycle Oscillation Mitigation

Due to the side effects of LCO on the DLDO steady state performance, it is desirable to achieve the minimum LCO mode or even remove LCO to reduce the steady state output voltage ripple. It is discovered in [63] that by adding two additional parallel power transistors as shown in Fig. 8, minimum LCO mode of one can be realized. However, due to NBTI induced $|V_{th}|$ increase, the current provided by a single additional power transistor deviates from that provided by the original power transistor. Such deviation gradually nullifies the effectiveness of the proposed technique. To more evenly distribute the electrical stress among all of the $N + 2$ power transistors, NBTI-aware DLDO with LCO mitigation is proposed in [39]. A dedicated digital controller is proposed to realize unidirectional control among the $N + 2$ power transistors.

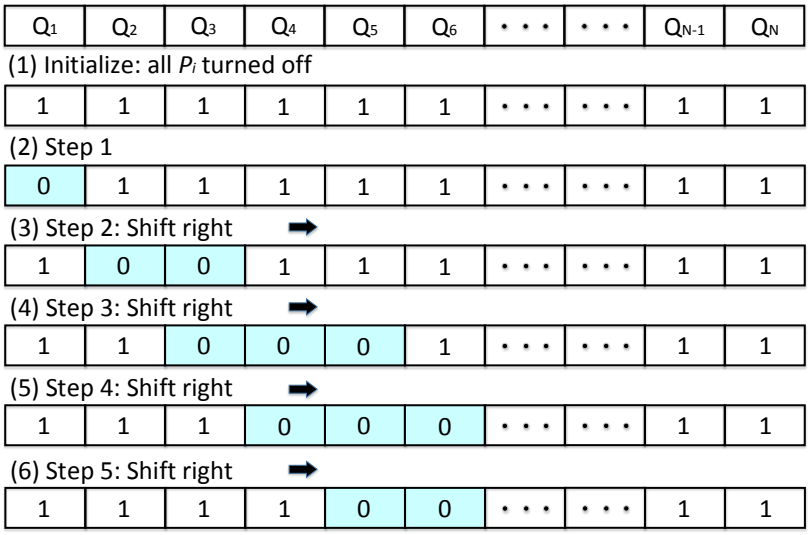



**Fig. 9.** Operation of the startup aware reliability enhancement controller [26].

### 3.4 NBTI-Aware DLDO with Improved Startup Performance

NBTI-Aware DLDO with unidirectional shift register is effective to more evenly distribute electrical stress among all of the power transistors as compared to bidirectional shift register control. However, for a special case when DLDO has to be turned off before or shortly after reaching steady state operation, the first few power transistors still undergo too much electrical stress as compared to the rest. When utilized in cyclic power gating [64], DLDOs can be periodically turned off when reaching around steady state. In this case, an unidirectional shift register functions similar to a bidirectional shift register. To mitigate this drawback

and enhance the reliability of DLDO during cyclic power gating operations, NBTI-Aware DLDO with improved startup performance is proposed in [26]. The operation of the startup aware reliability enhancement controller is demonstrated in Fig. 9. When more number of power transistor needs to be turned on during startup, two more power transistors are turned and one is turned off at the same time. In such a way, electrical stress can be more evenly distributed among more number of power transistors.

## 4 Proposed NBTI-Aware DLDO with AGS

Although there are respective advantages of the aforementioned DLDOs, the techniques proposed in previous works cannot be directly applied to DLDOs with AGS capability [65,66]. With AGS, DLDOs can adaptively change the number of power transistor (de)activated per clock cycle to speed up the transient process. NBTI-aware DLDO with AGS capability is proposed and investigated in this work. This is the first work which designs a novel uni-directional barrel shifter with AGS control.

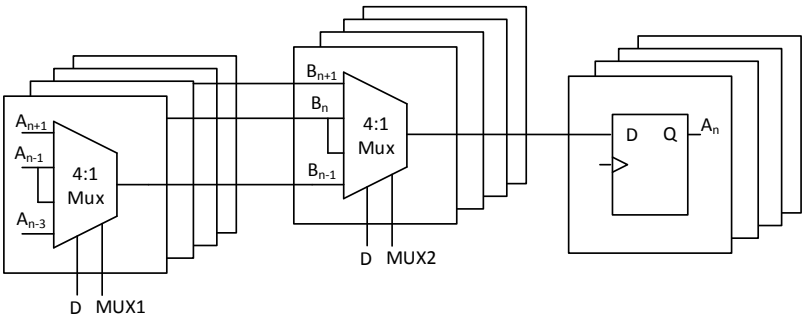



**Fig. 10.** Schematic of bi-directional barrel shifter.

### 4.1 Barrel shifter

Barrel shifter is the main component of the control loop. A simple schematic for a barrel shifter is shown in Fig. 10. A barrel shifter can activate multiple power transistors at the same clock cycle. For example, it can shift -3, -2, -1, 0, 1, 2, 3 stages at the same clock cycle. The magnitude of the shift in a barrel shifter serves as a gain control knob in the forward activation pattern of a DLDO. The barrel shifter in Fig. 10, is implemented using two levels of signal multiplexing followed by a flip-flop. A is the output of D flip flop and B is the output of the first level of MUX. The first level of MUX gives 0, 2, -2 and second level of MUX gives 0, 1, -1 shifts to obtain -3, -2, -1, 0, 1, 2, 3 shifts at the output

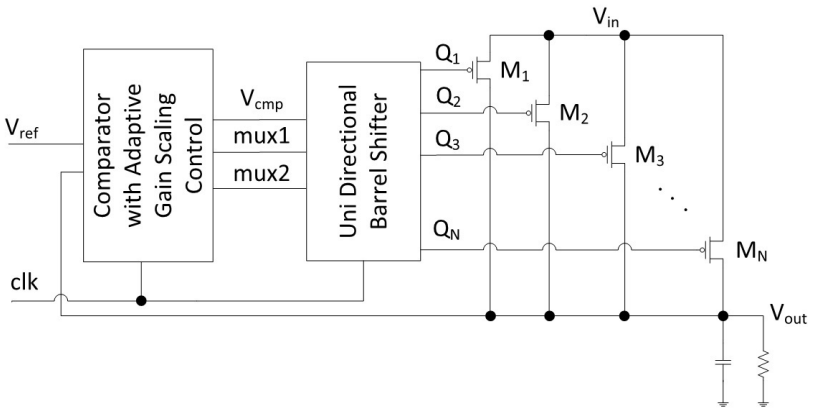



**Fig. 11.** Proposed NBTI-aware DLDO with AGS capability.

of the barrel shifter. The positive values mean a shift to the right and negative values to the left. $MUX1$ and $MUX2$ are used to control the barrel shifter as an output of up to three shifts. The first stage leads the input signals to the output of the 4:1 mux. $D$ is the comparator output which determines the direction of the activation scheme. $n$ is the stages of the barrel shifter. $n-1$ determines previous stage and $n+1$ determines forward stage similarly. The combination of $D$, $MUX1$, and $MUX2$ determines the gain of the barrel shifter and direction of the barrel shifter output activation scheme.

A bi-directional barrel shifter is proposed in [44] where the details can be seen in Fig. 10. This barrel shifter operates by switching a maximum of three transistors at the same clock cycle. 2N number of muxes and N number of D flip-flops are housed in the barrel shifter. The operation is maintained by adjusting the gain which can be adapted by selecting the logic inputs of the muxes. The work in [45] improves the operation of conventional DLDOs by introducing a bi-directional barrel shifter with steady-state load current estimator and a dynamic bi-directional shift register gain scaling control which adjusts the barrel shifter to obtain fast transient time. Steady-state load current estimator senses the load current and adjusts the frequency of the digital controller to get damped behavior of the voltage waveform. Dynamic bi-directional shift register gain scaling control automates the eight different gain according to the predetermined conditions which are studied in [45].

In this work, a new NBTI-aware DLDO with uni-directional barrel shifter with AGS is implemented. Therefore, the performance mitigation due to NBTI is maintained low and a good improvement in the transient response time has been achieved.

DLDO has a slow transient response under large load current changes. A trade-off exists between steady-state stability, transient response, and perfor-

| $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ | $Q_8$ | . . . | $Q_{N-1}$ | $Q_N$ |
|---|---|---|---|---|---|---|---|---|---|---|
| (1) Initialize: all $M_i$ turned off | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | . . . | 1 | 1 |
| (2) Step k | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | . . . | 1 | 1 |
| (3-a) Step k+1, if Vout < Vref & mux1=L, gain=1 shift ➡ | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | . . . | 1 | 1 |
| (3-b) Step k+1, if Vout > Vref & mux1=L, gain=1 shift ➡ | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | . . . | 1 | 1 |
| (3-c) Step k+1, if Vout < Vref and Vout > Vref - Δ, gain=2 shift ➡ | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | . . . | 1 | 1 |
| (3-d) Step k+1, if Vout > Vref and Vout < Vref + Δ, gain=2 shift ➡ | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | . . . | 1 | 1 |
| (3-e) Step k+1, if Vout < Vref - Δ, gain=3 shift ➡ | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | . . . | 1 | 1 |
| (3-f) Step k+1, if Vout > Vref + Δ, gain=3 shift ➡ | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | . . . | 1 | 1 |

**Fig. 12.** Operation of uni-directional barrel shifter with AGS.

mance degradation due to NBTI. A new architecture is designed to reduce the NBTI induced stress and to speed up the transient response.

Rotating the load stress among the power transistors enables the distribution of the loading evenly and reduces the NBTI induced performance degradation [67]. Furthermore, due to the steady-state gain control, settling time after the overshoots and undershoots are reduced. The transient loading effects are also minimized. As compared to a conventional DLDO, the transient loading response is improved.

A uni-directional DLDO with a barrel shifter is implemented within the proposed AGS. An enhanced AGS control manages all of the power transistors in a way that shortens settling time under severe transient loading and reduced aging for longer operation times have been achieved as compared to a conventional DLDO. The $V_{cmp}$, $mux1$, and $mux2$ are the control signals generated by the AGS. The details are depicted in Fig. 11.

### 4.2 Uni-directional shift register

The activation pattern of pass transistors in a conventional DLDO is typically designed to serve bidirectional. This deactivation and activation of the PMOS scheme can be observed in Fig. 12. The one-directional activation pattern can be observed in Fig. 12 (3-a) and (3-b). The $M_i$ represents the PMOS transistors. In the first stage, all PMOS is deactivated. In the second stage, when the digital controller reaches the $k$ stage, the controller determines the output pattern ac-

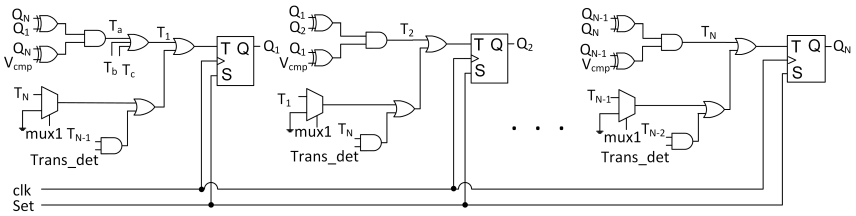



**Fig. 13.** Proposed uni-directional NBTI-aware DLDO with barrel shifter.

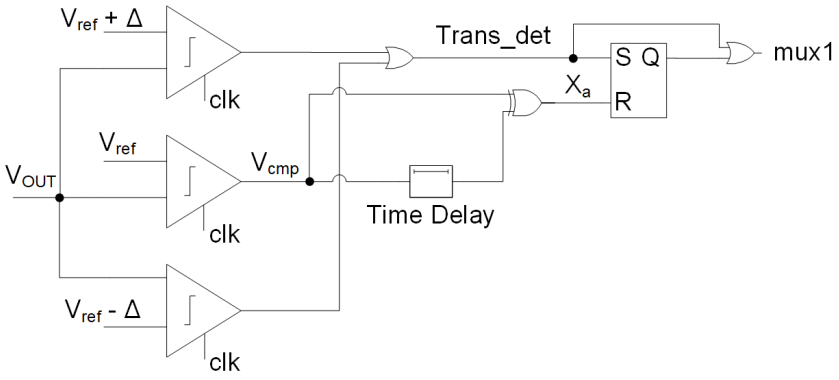



**Fig. 14.** Three stage adaptive gain scaling with steady state capture.

cording to $Vout$ value. In Fig. 12 (3-a), the gain is one which leads to activation of one transistor at the right boundary of the activation schema. In Fig. 12 (3-b), the activation of PMOS is at the left boundary of activation schema. Similarly, in Fig. 12 (3-c) and (3-d), the gain is two which activates two PMOS transistors at the same clock cycle. In Fig. 12 (3-e) and (3-f), the gain is three and causes the activation of three PMOS at the same clock cycle within the defined boundaries. This activation pattern should be modified to mitigate the NBTI induced performance degradation. Evenly distributing the electrical stress to all of the transistors can decrease the degradation in the current supply capacity of PMOS. Under transient loading, a uni-directional DLDO can activate and deactivate the PMOS due to the increased load current.

### 4.3 Uni-Directional NBTI-Aware DLDO with Barrel Shifter

The uni-directional barrel shifter is shown in Fig. 13. The schematic and operation of the proposed architecture are shown in Fig. 11 and Fig. 12. The Comparator in adaptive gain scaling control produces the signal of $V_{cmp}$, $mux1$, and $mux2$ which controls the uni-directional barrel shifter as the steady-state, gain 2 and gain 3 regions are operated. The elementary D flip-flop (DFF) and multiplexer within bi-directional shift register are replaced with T flip-flop and simple logic gates within the proposed uni-directional shift register. A multiplexer and simple logic gates are designed for uni-directional barrel shifter. A multiplexer and logic gates are added to get barrel shifter behavior in the uni-directional controller. This controller is designed to toggle a maximum of three gates at a single clock cycle, and it is the first time implementation of the uni-directional barrel shifter controller. The parallel gates remain unchanged, and uni-directional barrel shifter and AGS are added. The idea is to balance the loading of each power transistors under all load current conditions. The $Q_i$ and $Q_{i-1}$ are gated using XOR gate to equate the output signal switched consequently. $V_{cmp}$ is gated with $Q_{i-1}$ together with other $Q_i$ to determine the logic $T_i$. Therefore, when $V_{cmp}$ is high (low), inactive (active) power transistors at the right (left) boundary is turned ON (OFF). A uni-directional barrel shift register is realized through this activation/deactivation scheme, as demonstrated in Fig. 12. $T_b$ and $T_c$ are added at the logic to prevent the conflicting situations. $T_b = Q_1 \times Q_2 \times ... \times Q_N \times V_{cmp}$ and $T_c = \overline{Q_1 + Q_2 + ... + Q_N + V_{cmp}}$ [25]. During transient state, three signals $V_{cmp}$, $mux1$, and $Trans\_det$ are generated to adjust the gain of the barrel shifter where $mux1$ is a steady-state indicator signal that is generated by a novel steady-state detection circuit. After the system enters the steady-state, the system adjusts the gain to one. For barrel shifter, one mux and three additional gates are used in Fig. 14. Area overhead can be determined by counting the additional transistors and compared to the conventional DLDO per control stage. According to the previous definition, there is only a 4.5% area overhead. As the bi-directional shift register consumes a few $\mu W$ power, the uni-directional shift register power overhear is also negligible [25], [50]. Additional controllers consume low current, thus the power overhead is negligible for the proposed design.

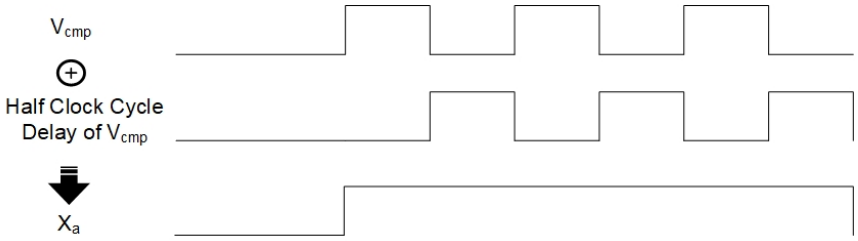



**Fig. 15.** $V_{cmp}$ and half clock cycle delay of $V_{cmp}$ XORed.

### 4.4 Three Stage AGS with Steady-State Detection Circuit

The schematic of a three-stage AGS with steady-state capture is shown in Fig. 14. There are three voltage comparators, two OR gates, one XOR gate, one-time delay, and one SR latch. There are two inputs and two outputs which are $V_{ref}$, $V_{out}$, $mux1$, and $Trans\_det$, respectively, for this circuit. Two comparators provide overshoot and undershoot detection. One comparator senses the changes in the $V_{out}$. Half cycle time delayed $V_{cmp}$ is XORed with $V_{cmp}$ to determine the steady-state operation. AGS senses the changes in $V_{cmp}$ during steady-state operation. The operation of uni-directional barrel shifter starts to control the oscillation at the output of DLDO due to limit cycle oscillation [68]. When $V_{cmp}$ starts to oscillate during the steady-state operation, $X_a$, the output of XOR gate $X_a$ is high, leading to the reset of SR latch. The $X_a$ signal can be observed in Fig. 15. Thus, the output $mux1$ is low to enter a steady-state region. The variation at the output of DLDO is minimum when the gain is one because the voltage change of one PMOS activation is lower than two or more PMOS activation. If the number of parallel PMOS increases, according to Kirchhoff's voltage law, the drop-out voltage decreased. When the DLDO enters out of the steady-state region, $V_{cmp}$ and time-delayed $V_{cmp}$ are XORed giving logic low at $X_a$. Following the output of the XOR gate, SR latch's output is high which makes $mux1$ high and the gain scaling circuit operates out of steady-state mode.

The circuit operates in three different modes in three different regions. The first region is the highest gain area in which the circuit operates to provide high in $mux1$ and $Trans\_det$ and the gain is three, which means that barrel shifter switches three consecutive power transistors at the rising edge of a single clock cycle. Within the second region, the gain is two such that two power transistors will be turned on/off at the same time. This region is for fast settling of the output voltage. The third region is the gain one region where the steady state voltage variation is achieved at the output by changing the minimum amount of power transistor. For steady state operation $mux1$ and $Trans\_det$ are logic low.

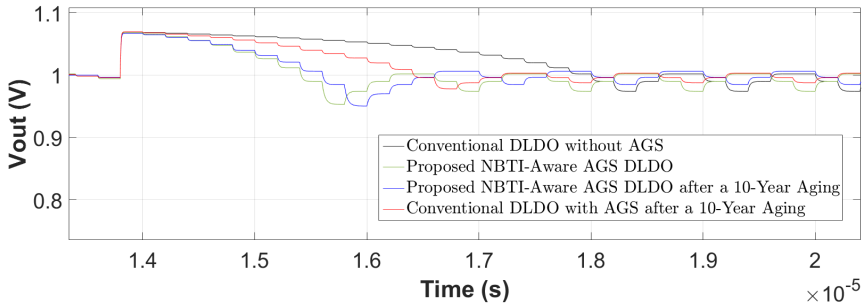
### 4.5 Operation of the Proposed NBTI-Aware DLDO with AGS Capability

The NBTI-aware uni-directional controller with AGS capability is shown in Fig. 12. When $V_{out}$ is lower than $V_{ref}$, the barrel shifter activates the power transistors at the right boundary. Similarly, when $V_{out}$ is higher than $V_{ref}$, the barrel shifter deactivates the power transistors at the left boundary of the inactive/active power transistor region. Depending on the value of gain, a maximum of three active (inactive) power transistors switch inactive (active) power transistors at the boundary. The uni-directional barrel shifter always toggles the power transistors at the right of the boundary. The switching of the power transistors is always in one direction (right shift). Therefore, the stress on the power transistors evenly distributed because the operation load of each PMOS is distributed equally among each transistor. Furthermore, as compared to conventional DLDO, the steady-state performance does not change and the transient response time is decreased. During the design of the DLDO, being aware of NBTI induced performance degradation is important. The reliability of DLDO can be enhanced by implementing the method in this article. This work improves the performance of AGS with respect to other works in Table 1 since the AGS has three modes. The first mode is aggressive gain scaling. The second mode is slow settling and the third mode is steady-state mode.

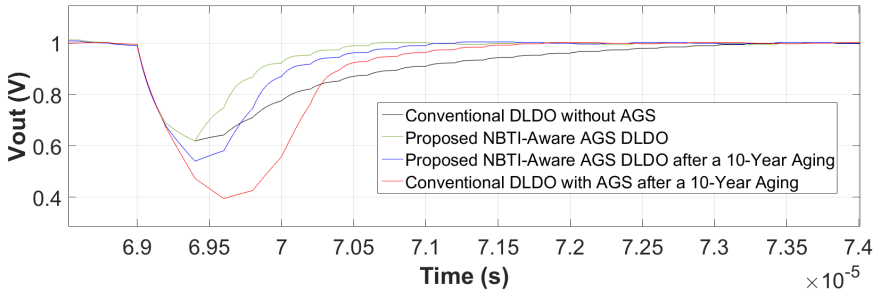
**Steady-State Operation** In the steady-state mode, the number of active and passive PMOS is changing dynamically. Limit cycle oscillation leads to output voltage ripple at steady-state. The number of active/inactive transistors are the same for both NBTI-aware DLDO with AGS and conventional DLDO but the gain is different while transient state resulting in faster settling time. In Fig. 12 (3-a) and (3-b), the operation of steady-state operation can be observed. The PMOS at the right boundary changes its activity one transistor at each clock cycle.

**Slow Settling Operation** In the slow settling mode, the barrel shifter gain is two, meaning that PMOS transistors change their activity two transistors at each clock cycle. The operation is quite different from conventional DLDO since the gain of conventional DLDO is one in every loading case. The advantage of this mode is that it reduces the overshooting and undershooting under transient loading. In Fig. 12 (3-c) and (3-d), the slow settling operation can be observed. The PMOS at the boundary changes its activity two transistors at each clock cycle. Depending on $V_{out}$, the transistors at the left boundary or at the right boundary change their operation from inactive to active.

**Aggressive Gain Scaling** In the aggressive gain scaling mode, the barrel shifter gain is three. The advantage of this operation is that it reduces the settling time significantly [45, 69]. Under transient loading, the load current changes significantly. In Fig. 12 (3-e) and (3-f), the operation of aggressive gain scaling




(a) Comparison of overshoot.




(b) Comparison of undershoot.

**Fig. 16.** Comparison of transient loading among aging-aware and aging-unaware DLDOs.

can be observed. The active PMOSs (shaded region) change their operation to inactive depending on the $V_{out}$. The consecutive three transistors change their operation in the same clock cycle.

## 5 Evaluation of the Proposed Circuit

In order to validate the effectiveness of the 1.1 V to 1.0 V DLDO, this on-chip circuit is designed in a 32 nm standard CMOS process. The proposed DLDO can supply a maximum of 124 mA current. The transient output voltage waveform from 20 mA to 60 mA step load change and comparison of the results of the conventional DLDO without AGS, the proposed NBTI-aware DLDO with AGS, the proposed NBTI-aware DLDO with AGS after 10-year aging and the conventional DLDO with AGS after 10-year aging are shown in Fig. 16. 1 MHz clock frequency is applied and aging induced degradation is evaluated under $100°C$. The settling time after load decrease is 4.5 $\mu s$ and the settling time after load increase is 4.2 $\mu s$ for the conventional DLDO without AGS. The proposed NBTI-aware AGS DLDO has 2.4 $\mu s$ settling time after an overshoot and 1.7 $\mu s$ settling time after an undershoot. The proposed NBTI-aware DLDO with AGS after 10-

**Table 1.** Comparison with Previous Aging-Aware On-Chip DLDOs

| | [42] | [43] | [25] | This work |
|---|---|---|---|---|
| Year | 2015 | 2017 | 2018 | 2019 |
| Broad load range | Yes | Yes | Yes | Yes |
| Additional controller | Yes | Yes | No | No |
| Added overhead | Multiple decoders | Decoder | Modification of original controller | Modification of conventional DLDO |
| Topology | Row rotation scheme | Code roaming algorithm | Uni-directional shift controller | Uni-directional shift controller with barrel shifter |
| Adaptive gain scaling capability | Yes | Yes | No | Yes |

year aging has 2.8 $\mu s$ settling time after an overshoot and 2.1 $\mu s$ settling time after an undershoot. The conventional DLDO with AGS after a 10-year aging has 3.4 $\mu s$ settling time after overshoot and 2.8 $\mu s$ settling time after undershoot. The results for conventional DLDO with AGS without aging is the same as the results of proposed NBTI-aware DLDO with AGS. There is 46.7% decrease in the settling time of overshoot of the proposed DLDO with AGS as compared to the conventional DLDO. There is also a 59.5% decrease in the settling time of undershooting of the proposed DLDO with AGS as compared to the conventional DLDO. Furthermore, the settling time for the proposed DLDO with AGS after 10-year aging is decreased by 59.5% as compared to the conventional DLDO with AGS after 10-year aging.

Previous works are compared with this work in Table 1. The power overhead in [42] is negligible since added decoders have little power consumption with respect to power PMOS. Similarly, the power overhead in [43] and [25] is negligible because the modifications add negligible power consumption. The works in [42] and [43] have AGS capability.

## 6 Conclusion

In this work, an NBTI-aware DLDO with the AGS control is proposed to diminish the aging effect and to reduce the settling time. The settling time is reduced by 46.7% and 59.5% for overshoot and undershoot without aging aware design, respectively. The proposed circuit is NBTI-aware, thus, performance degradations due to NBTI are reduced. A novel uni-directional shift register with barrel shifter is proposed to distribute the electrical stress among the power transistors evenly. The proposed NBTI-aware DLDO with AGS control is efficient because the settling time is reduced by 33% after 10-year aging.

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