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Design of a Real-Time DSP Engine on RF-SoC FPGA for 5G Networks

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Abstract. 5G advances the wireless communications by providing a significant improvement to the data rate, capability of connected devices and data volumes compared to the previous generations. While these advantages combine along with a wider range of applications to merit the end-user, the technologies to be used are not specified. Considering this problem and in order to efficiently support the 5G deployment researchers and engineers turned their attention on FPGA base band architectures that keep the implementation cost relatively low and at the same time they are reprogrammable to provide solutions to the emerging requirements and their consequent modifications. Aiming at the contribution to the 5G technologies the current paper introduces the design of a base band DSP architecture that targets the required real time performance. Moreover, the proposed architecture is scalable by efficiently parallelizing and/or pipelining the corresponding data paths. The paper presents the pilot FPGA designs of the IFFT/FFT and Sampling Frequency Offset (SFO) functions that achieve a 500 Msps performance on a RF-SoC Xilinx ZCU111 board.

Keywords: 5G Networks · 5G-PHOS · DSP Engine · FPGA.

1 Introduction

Even though the number of 5G technology demonstrations that are presented by the system vendors and telecom operators is increasing [1], the transition from 4G-Long Term Evolution (LTE) will be a long process, while the final 5G specifications are not defined yet. This transition is enforced by the network demands of increasingly popular emerging technologies such as virtual/augmented

reality and 4K video, low latency, reliability and device/network energy efficiency, will be addressed by 5G networks by exploiting existing technologies that include millimeter waves (mmWave), massive multiple input – multiple output (MIMO), beamforming [2], [3] and multi-carrier modulation formats [4]. The prevailing network architectures are the centralized and ultra-dense network topologies at the mobile fronthaul (MFH), providing higher data rates in a new radio-band (30-300GHz) [5] through the use of mmWave (radiofrequency) RF carriers. However, the high attenuation of mmWave transmission, due to atmospheric absorption, will anchor optical fiber as the main transmission link between the Base Band Unit (BBU) and the Remote Radio Head (RRH) side, bringing Radio-over-Fiber (RoF) technology to the core of future 5G implementations [5].

The MFH with digital fiber-optic interfaces, such as the Common Public Radio Interface (CPRI), with high data rates cannot be supported by the CPRI-formatted frame specifications [6]. Moreover, the latency of RRH processing [7] makes Analog RoF (A-RoF) a strong 5G candidate, without digitization penalty but with high throughput eliminating the optical hardware demands.

In this context, the EU funded H2020 5G-PHOS project, will exploit results in the area of photonics in order to architect centralized A-RoF 5G networks for dense, ultra-dense and Hot-Spot areas incorporating Photonic Integrated Circuits (PICs) in optical mmWave signal generation, DSP-assisted optical transmission, reconfigurable optical add/drop multiplexing (ROADM) and optical beamforming functionalities. 5G-PHOS expects to release a seamless, interoperable, RAT-agnostic and SDN-programmable FiWi 5G network that supports 64x64 MIMO antennas in the V-band.

BBUs involve computationally demanding DSP functions and have to be reprogrammable because the standards are still open. Moreover, the transition from Distributed-RAN (D-RAN) topologies towards Cloud-RAN (C-RAN) architectures, where a pool of BBUs accommodate the needs of several RRHs, will use reconfigurable processors and FPGAs [11]. Besides the cloudification of the mobile fronthaul, fully elastic optical transceivers will operate in dual mode supporting both D-RoF and A-RoF transport, and allow for distance-adaptive modulation [12]. These elastic FPGA-based BBUs facilitate also the transition towards Ethernet-based fronthaul [13]. Through this Radio-over-Ethernet (RoE) approach, FPGAs can offer solutions that cope with the inherent jitters of the CPRI traffic over standard Ethernet [14].

In the current work within the context of 5GPHOS [23], we design a proof-of-concept datapath to transmit and receive data according to the aforementioned ideas of C-RAN and A-RoF, with potential use even in future MEC scenarios. More specifically, we consider here data streams e.g., via Ethernet, as input to our system consisting of: a) CPU/smartNIC handling MAC layer tasks, b) FPGA handling the digital baseband processing, c) DAC/ADC for signal conversion to an IF, d) fiber optics for ARoF transmission/reception to the RRH, and e) mmWave RRH for establishing new radio-band links. Aiming at providing an effective solution to the BBU, this paper focuses on the design of a

System-on-Chip (SoC) FPGA-based architecture realizing parts (b) and (c). To this end, we capitalize on state-of-the-art chips integrating processors, FPGA resources, DAC/ADC with digital-up/down-conversion and hard-IPs for the FEC functions, to provide a scalable embedded solution with low cost/power but real-time performance. We research for developing the BBU DSP functions and their fine tuning by the use of simulations and implement these on Xilinx RF-SoC FPGA of the ZCU111 board [21]. The proposed custom VHDL circuits are based on pipelining and parallelization techniques to achieve the required real-time performance. The following sections present an overview of our envisaged final system, details regarding our functions at algorithmic level, as well as the FPGA architectures of the IFFT/FFT and Sampling Frequency Offset (SFO) designed during the ongoing development stage of our DSP chain.

The paper is organized with the following section presenting related FPGA architectures. Section 3 describes the DSP algorithmic design and details. Section 4 presents the DSP architecture. Section 5 gives the details of the design on the FPGA and the corresponding performance results and finally, Section 6 concludes the paper.

2 State of the Art and Related Results

The main challenge in A-RoF transmission is the transport of mmWave signals over the optical link achieving high performance. In order to overcome signal impairments, the proposed methods include the impact of chromatic dispersion through RF power fading and distortion due to nonlinearity within the link [8]. A-IFoF is gaining momentum on the verge of 5G release, while DSP-enabled A-IFoF/mmWave transmission is shown in laboratory scale [11]. Using IF frequencies can mitigate the distortion caused by optical links without fully compensating for the Fi-Wi channel impairments. Consequently, DSP technics on FPGAs improve the signal quality based on pre-emphasis and post-equalization technics [9]. DSP-enabled channel aggregation methods used in MFH systems achieve high bit-rates and multiple-user connectivity [10].

There is a plethora of works for OFDM transceivers on FPGA devices for specific communication standards. The work in [15] shows FPGAs with a full processing chain for an OFDM transceiver for the IEEE 802.11, IEEE 802.16 and IEEE 802.22 standards. In [17] a non-continuous OFDM FPGA-based baseband architecture utilizes dynamic partial-reconfiguration to adapt its processing datapath and [18] gives the adaptable FFT core. Finally, [16] presents a pilot-based channel estimation technique for a system consisting of a 16-QAM mapper/demapper, 1024-point IFFT/FFT with 798 data samples, 56 pilots and 170 zeros.

3 DSP Algorithm

3.1 Centralized DSP engine

Figure 1 shows the single band Tx and Rx DSP block chain designed to support the centralized, analog RoF based network architecture targeted in 5GPhos.

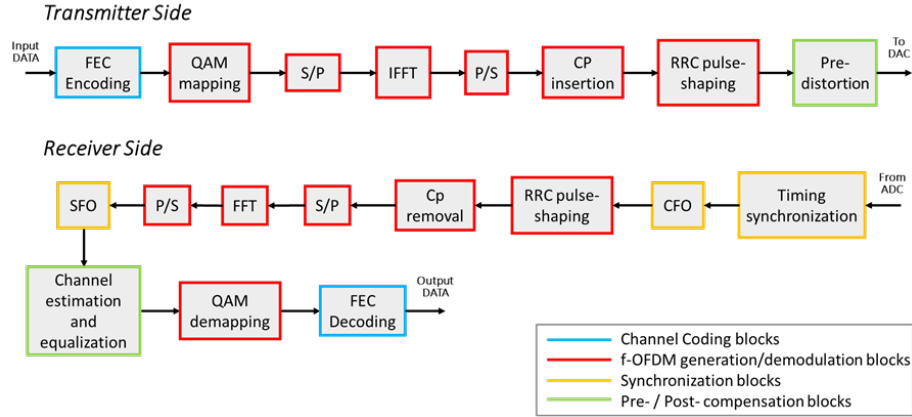


Fig. 1. Block diagrams of typical f-OFDM optical transmitter and receiver DSP chain

Multiplexing of multiple bands will be performed in the DACs driving the centralized transceiver’s unit optical interface. The DSP blocks represented with red color, are used for the generation and demodulation of f-OFDM signals. Specifically, the operations of these blocks are the modulation of the QAM symbols, their mapping to orthogonal sub-carriers, the CP insertion and the filtering at the transmitter side and the corresponding operations at the receiver side. Considering 5G specifications [22], the 5GPHOS waveform parameters are: 400MHz band-size, 256-point FFT and 32-samples cyclic prefix (cp). In the literature the candidate filters are: the soft-truncated sinc filters, including hann and rrc window, and the equiripple filters based on the Remez exchange algorithm. Given that equiripple filtered signals are prone to ISI and the extended use of rrc filters, the latter was the filter of choice in 5GPhos.

3.2 Algorithmic Treatment of Timing and Frequency Synchronization

Both FFT window alignment and carrier frequency offsets (CFO) correction are dealt with in time domain, as depicted in Fig. 1. The operating principle of the two block relies on identifying in the received signal an expected time domain sequence or some form of repetition. For this purpose, a preamble is used and correlation algorithms executed at the receiver side track the f-OFDM symbols and the local oscillator induced frequency offsets.

Possible inaccuracies in the receiver and transmitter sampling clocks could lead to ICI. Sampling frequency offsets (SFO) causes slow drift of the FFT window, hence loss of the sub-carriers orthogonality. In contrast to the CFO, the effect of SFO depends on the individual sub-carriers’ characteristics, therefore most DSP techniques for SFO compensation are applied in frequency domain, thus after the FFT block. Both pilot-aided and blind methods can be adopted

for the algorithmic treatment of the effect. In 5G-PHOS, we will use a blind algorithm based on the fourth power of the phase of the received sub-carriers for extracting a mean value of the constellation rotation. Then, we apply the estimated phase to the signal.

3.3 A-IFoF Tx pre-Compensation and Rx Equalization

To achieve correct demodulation of the received signal, an estimation of the inverted channel response must be calculated and applied to the signal, minimizing the impact of the channel noise and frequency selectivity. The term “channel” refers to the whole transmission link that includes the length of the sSMF fiber, the wireless link, any electro/optical amplification and up/down-conversion required. The above processes are implemented either at the receiver, by an equalization filter, or at the transmitter by a pre-distortion filter. For a C-RAN compatible DSP engine, an FPGA board will perform both the pre-distortion and equalization DSP functions, alleviating end-user hardware processing.

Multi-carrier waveforms consist of a large number of modulated sub-carriers, which can result in much higher instantaneous amplitudes than the signal average power. The insertion of a pulse shaping filter in the f-OFDM waveform results in a lower PAPR, compared to a CP-OFDM approach [19], but still high enough to render the signal prone to distortion caused by the non-linear components of the A-IFoF transmission. Those include all electro-optic components, i.e. the EMLs and the PDs, but also power amplifiers and passive mixers. To improve the f-OFDM transmission linearity, a pre-distortion technique is required. For the respective algorithm generation, the memory effects of high PAPR caused non-linearity are taken into account. A widely discussed method for modeling the nonlinearity in literature is the Volterra series memory polynomial. However, since extracting the inverse of the Volterra system is complicated, an adaptive pre-distorter scheme seems to be preferable than a post-compensation scenario. This algorithm can be implemented by an adaptive filter fed by a one-tap RLS or LMS algorithm [20].

An advantage of multi-carrier waveforms is their robustness to chromatic dispersion and wireless link multipath effects. Thanks to the cyclic prefix insertion to the transmitted f-OFDM symbols, the time-domain signal presents periodicity which allows for a simpler channel estimation in frequency domain. Thus, the receiver equalization can be performed by a single-tap filter, as in the pre-distortion case. The equalization schemes are selected by taking into account the wireless channel transmission effects, since the optical link is static and adds insignificant distortion to the signal.

4 Base Band Digital Architecture

The 5G-PHOS project will use a ZCU111 board hosting a Xilinx’s Zynq Ultra-scale+ RF-SoC device [21], which integrates a quad-core Cortex-A53 APU, a

dual-core Cortex-R5 RPU, an FPGA fabric and dedicated ADCs/DACs. Moreover, each ADC/DAC component has its own digital datapath that offers real or complex signal processing, digital-up/down conversion units and mixing to digital IF frequencies in the order of GHz. Furthermore, specialized soft-decision FEC (SD-FEC) hard-blocks support the processing requirements.

Currently, similar deployed systems use an FPGA device along with external DACs/ADCs to implement the required functionality. These systems adopt the JESD204B standard as the link between converters and the receiver/transmitter. The downside of this approach is the development time needed to optimize the communication, as well as the power consumed. On the other hand, the RF-SoC device offers an embedded hardware platform for the deployment of the proposed DSP engine, alleviating extra development or performance costs. In the presented setup, the RF-SoC device includes the DSP blocks for the transmitter and the receiver. The board communicates with an ethernet switch utilizing the 25GBASE-SR standard through an SFP28 connector and by SMA cables it interfaces the ADCs/DACs with the analogue front-end.

The transmitter gets data from the ethernet switch and forwards these into four independent processing paths that handle a 500MHz band each. The bands are processed independently (Fig.1 transmitter) and their data are forwarded to four distinct DAC units configured in pairs to merge their respective bands and to produce two dual-band signals digitally up-converted to 1.5GHz digital IF and converted to analog. These analog signals are transmitted through SMA cables in an analog synthesizer, capable to up-convert the received signals to their analog IF of 5GHz and from there drive the next stage, which consists of the optoelectronics components. In the receiver, optical signals are converted to electrical on the optoelectronics components. These analog signals have an analog IF of 5GHz and are down-converted to 1.5GHz analog IF by the analog synthesizer, that feeds the ADCs of the RF-SoC device. A single ADC digitizes the received signal and it further digitally down-converts a dual-band signal to baseband, separates it to two single bands and sets apart the I/Q parts of the signals. The output of an ADC is then processed by the FPGA DSP blocks of the receiver subsystem (Fig.1 receiver) and the results are transmitted through the ethernet IP core to the external ethernet switch. Fig. 2 illustrates the high-level architecture of the DSP engine on RF-SoC device. Note that the dual-band creation on the DACs is simplified for illustrative purposes.

We illustrate the design of the DSP algorithms of the RF-SoC device by the description of the receiver processing chain for a single band signal. An ADC provides to the FPGA a 2Gsps single band signal separated to its I/Q parts. First, a timing synchronization algorithm on two streams of samples locates the frame start. The output rate will be 500Msps. Next, the CFO correction block corrects any frequency offset on the received signal and then each I/Q stream drives through an RRC pulse-shaping filter to minimize ICI and ISI effects and it removes the samples of the CP. The fourth step is the FFT decimation in frequency radix-2 FFT algorithm; it processes 256 complex points since every OFDM symbol consists of 256 I/Q samples (191 carriers, 17 pilots and 48 ze-

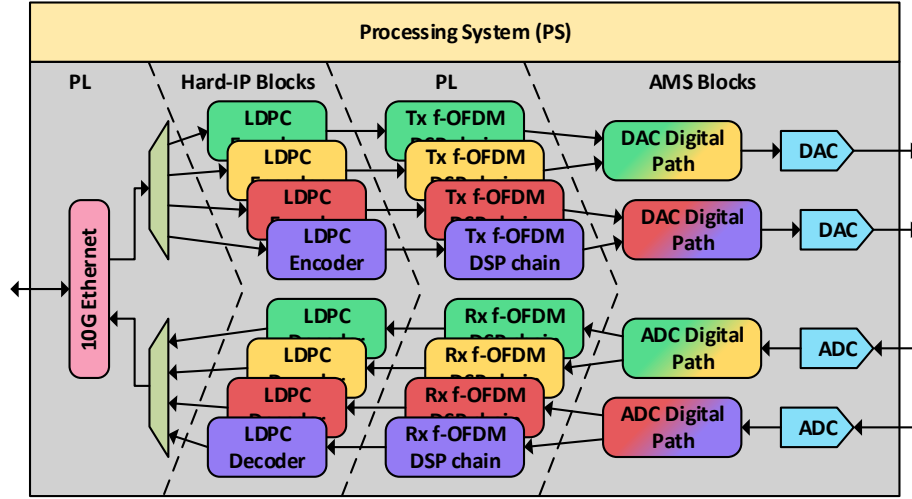


Fig. 2. High-level architecture of DSP processing on Zynq Ultrascale+ RF-SoC device.

ros) and produces results with ~ 470 Mps. The fifth step implements the SFO correction block based on the Viterbi Fourth Power Estimator algorithm. The block receives the complex output points from the FFT block and corrects the frequency offsets.

At this stage, after completing the correction of the possible errors introduced during the transmission of the signals through the channel, the DSP chain performs the channel estimation and equalization. This procedure takes as input the results calculated by the SFO correction block and uses the 17-pilots samples present in each OFDM symbol to perform its operation. The results of this block are forwarded to a soft-decision QAM demodulation block. The QAM demodulator can demodulate 4/16/64-QAM constellations and implements the approximate log-likelihood ratio (ALLR) algorithm to give an estimate on the value of the data bits received. Finally, the ALLR values are given as input to the soft-decision FEC block at ~ 350 Mps. The FEC processing block performs LDPC decoding, and based on the ALLR values gives the final stream of data. This stream of data is the input to the ethernet IP block.

5 FPGA Design & Results

The proposed FPGA architectures are scalable with respect to the throughput by parallelizing and/or pipelining the data paths. For efficiently supporting the data stream we opted to include all the modules as a pipelined chain architecture. Currently, we have complete the FPGA design and the testing of its two major modules: the *FFT* and the *phase shift estimation and compensation (SFO)*.

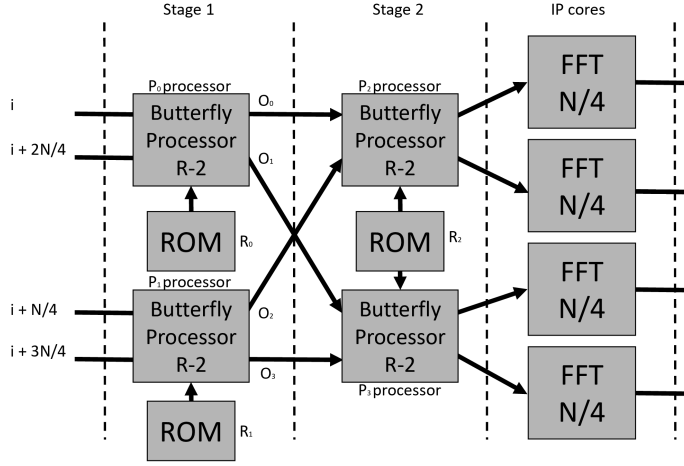


Fig. 3. The FFT module

5.1 FFT Module

Off-the-self IPs can be used for the radix-2 decimation in frequency (DIF)FFT. To achieve though the required throughput we have to include more than one cores into a parallel design: it has a throughput proportional to the number of cores, that is the parallel architecture of k parallel smaller FFT blocks, the parallel design achieves k times greater throughput than a single block design. For a relatively small k the parallel design will achieve the same clock frequency with the single core. The proposed design is based on a scalable k block N -point FFT. The initial study showed that the four blocks should suffice with respect to the required throughput (Fig. 3). The four blocks N -FFT design accomplishes four times the throughput and operates with four $N/4$ -point FFT blocks. Two additional stages must be implemented before the $N/4$ -FFT blocks, to complete the two first stages of the DIF-FFT algorithm. The first stage consists of two radix-2 processors (P_0 and P_1) and two ROM memories (one memory per processor, R_0 and R_1). The first processor P_0 receives as inputs the FFT points with indexes i and $i + 2N/4$ (where $i=[0, 1, 2, \dots, N/4 - 1]$) and produces two outputs O_0 and O_1 . The phase factors of this processor are stored in the first ROM (R_0) in the following order $[0, 1, 2, \dots, N/4 - 1]$. The second processor (P_1) receives as inputs the FFT points with indexes $i + N/4$ and $i + 3N/4$ (where $i=[0, 1, 2, \dots, N/4 - 1]$) and produces two outputs O_2 and O_3 . The phase factors of this processor are stored in the second ROM (R_1) in the following order $[N/4, N/4 + 1, N/4 + 2, \dots, N/2 - 1]$. The second stage also consists of two radix-2 processors (P_2 and P_3) but one ROM (R_2) since the processors in this stage use the same factors. The inputs of P_2 are O_0 and O_2 while the inputs of P_3 are O_1 and O_3 . The phase factors of this stage are stored in R_2 in the following order $[0, 2, 4, \dots, N/2 - 2]$. Each processor output is the input of each $N/4$ -FFT

block. The output of the first $N/4$ -FFT block are the FFT points with indexes $[0, 4, 8, \dots, N - 4]$, the output of the second are the FFT points with indexes $[1, 5, 9, \dots, N - 3]$, the output of the third are the FFT points with indexes $[2, 6, 10, \dots, N - 2]$ and the output of the fourth are FFT points with indexes $[3, 7, 11, \dots, N - 1]$.

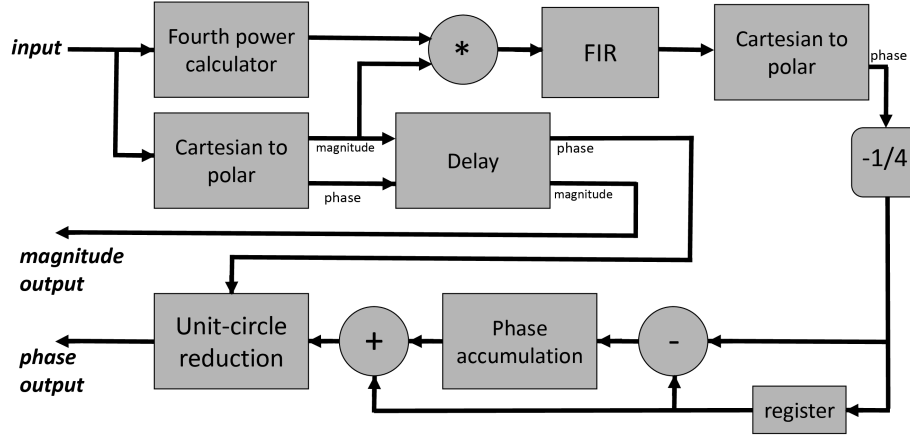


Fig. 4. The phase shift estimation and compensation module

5.2 Phase Shift Estimation and Compensation

The phase shift estimation and compensation module consists of six basic components: the fourth power calculator block, two cartesian to polar conversion blocks, the FIR filter block, the delay block, the phase accumulation block and the unit-circle reduction block (Fig. 4). The fourth power calculator block computes the fourth power of the complex input as follows: the complex input is routed to both input-ports of a complex multiplier; this multiplier computes the second power of the complex number. Similarly, a second complex multiplier computes the fourth power of the complex number. The cartesian to polar conversion block uses the Cordic algorithm to calculate the magnitude and the phase of the cartesian input. The fir block is a transposed Finite Impulsive Response (FIR) filter with L -taps and all the coefficients are equal to $1/L$. The delay block is a FIFO memory with depth $L/2$, the input is delayed for $L/2$ cycles. The phase accumulation block receives as input the phase of a complex number, which has a real number representation. The input is multiplied by the number $2/\pi$. The product of the multiplication is subtracted from the number $1/2$ and the product of this subtraction is floored. Then the floored numbers are multiplied by $\pi/2$ and the product (FN) must be accumulated each clock cycle. If the accumulated output is greater than 2π then the accumulation input

is $FN - 2\pi$ instead of FN . This method subtracts the unit-circles (note that $e^{2\pi i} = 1$) from the accumulation. The unit-circle reduction block receives as input a phase and compares it with π . If the phase is greater than π then 2π is subtracted from the phase. This method ensures that the values are between $-\pi$ and π . The product of this operation is added with the output of the delay block and the final correction is performed. The product of the addition is compared with $-\pi$ and π . If the product is greater than π then 2π is subtracted from the product; else if the product is smaller than $-\pi$ then 2π is added to the product. The output is the corrected phase and the phase values are between $-\pi$ and π . The input to the module is a complex number; this number is the input of the fourth power calculator block and the first cartesian to polar conversion block. The product of the first block is the fourth power of the module input, while the product of the second block is the magnitude and the phase of the module input. The fourth power is multiplied by the magnitude and the product is the input of the FIR block. The magnitude and the phase are the inputs of the delay block. The output of the FIR block is the input of the second cartesian to polar conversion block. The output of the cartesian to polar conversion block is negated and divided by four; then, the product is subtracted with the product of the previous clock cycle (delayed product). The result of the subtraction is the input of the phase accumulation block. Then, the output of the phase accumulation block is added to the delayed product. The product of this addition and the output of the delay block are the inputs of the unit-circle reduction block. Finally, the output of this block and the magnitude output of the delay block are the outputs of the module.

5.3 FPGA Results

The demonstration prototype required a 2 Gsps throughput design on the KCU105 board. The aforementioned FPGA achieves this throughput with the four FFT core design. The FFT was configured to process 256 points with 16-bit accuracy for the real part and 16-bit for the imaginary part for each input and output point. The scaling factor of the output points is 8-bits ($2^8 = 256$). The module achieves clock frequency 0.5GHz and utilizes the following FPGA resources: 4286 LUTs (1.77% of the available), 1311 LUTRAMs (1.16%), 8379 FFs (1.73%), 2 BRAMs (0.33%) and finally 96 DSPs (5%).

The phase shift estimation and compensation module implementation achieve the target throughput (500 Msps on the RFSoc (XCZU28DR) board) with minimum calculation complexity and minimum accuracy loss. The unit-circle reduction method was used to avoid the implementation of divisions and the scaling of the data. The proposed method is advantageous, because it utilizes comparisons and additions/subtractions, which keep the implementation cost lower than the corresponding divisions and have no impact on accuracy. This method is also safe regarding the overflow, since the design keeps the data values inside specific intervals (e.g. $[-\pi, \pi]$). The design was configured to process 32-bit words; 16-bits real part and 16-bits imaginary part for the input data, 16-bits magnitude and 16-bits phase for the output data. As noted above the data are unscaled.

The module achieves clock frequency approximately 0.5GHz and utilizes the following FPGA resources: 2235 LUTs (0.56% of the available), 126 LUTRAMs (0.06%), 2546 FFs (0.3%) and finally 13 DSPs (0.3%).

6 Concluding Remarks

The current paper summarized key requirements/directions in emerging 5G technologies that will benefit from FPGA platforms and, subsequently, in the context of the ongoing European project 5GPHOS, it presented our proof-of-concept design of a scalable baseband processor supporting ARoF links in 5G networks. The proposed design exploits a state-of-the-art system-on-chip FPGA tailored for RF applications, namely the XCZU28DR RFSoc. We utilized its integrated set of DAC, ADC, FEC, CPU, and FPGA resources, to assemble processing pipelines realizing high-performance OFDM transmitters and receivers for mmWave telecommunications. In our scalable FPGA architecture, 4+4 distinct pipelines at 500Mps will operate in parallel to input+output 4+4 streams of data comprising four bidirectional bands. Each pipeline will accelerate multiple DSP functions via efficient VHDL circuit design and customized configuration of the relevant RFSoc components. Our future work will advance the architectural design and development of each DSP function on FPGA, its optimization and integration to the system, and the testing of the final FPGA module, in-the-field. Our final FPGA module targets approximately 8+8 Gbps throughput, in total, with low-latency, low-power, and real-time performance.

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