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# Self-Timed Power-on Reset Circuit for Pseudo Dual/Two Port SRAM used in Low-Voltage IoT Applications

Vivek Nautiyal, Lalit Gupta, Gaurav Singla, Jitendra Dasani, Sagar Dwivedi, Martin Kinkade

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**Abstract.** The purpose of the Power-on Reset (POR) circuit is to reset the latches and flip-flops in an SOC to a known state when the supply is ramping up. During power-up, supply is not stable, and the ramp-up time can vary depending on the applications. A common approach is to generate a POR signal by comparing the supply voltage with a reference voltage. Pseudo dual/two port memories are used in graphic applications where parallel computing is prime factor instead of performance. IoT applications comprise significant image and video processing for which these memories are used. Conventional SRAM does not need a POR circuit but pseudo dual/two port memory face functionality issues without a POR circuit. Low-power applications, like Internet of Things (IoT) devices, comprise of SRAM arrays, sensors, and logic operating at sub-threshold or extremely low voltages. Conventional POR circuits also use a resistor divider circuit along with band gap reference. At these low operating voltages, generating a stable reference voltage is difficult because of band gap reference limitations and process variations. In this paper, we present multiple POR circuits that operates without using a reference voltage, making it robust against different sources of variation. First proposed circuit is self-timed, meaning the reset signal pulse-width varies according to the time needed to reset the latch. The designed circuit has been fabricated in 16nm FinFET technology. Silicon validation shows that the proposed POR circuit works at a minimum supply voltage of 400mv. Simulation verifies that the POR circuit is operational in sub-threshold region but is limited to 400mV on silicon due to the operational voltage of additional testchip logic. Also, the POR circuit does not consume any dynamic power during normal operation of the SOC and has minimal area overhead of 21.3 $\mu\text{m}^2$ . Second proposed circuit is latch based self-feedback circuit which resolves limitations of the initial proposed circuit.

**Keywords:** Power-on Reset (POR); sub-threshold; 16nm; FinFET; Self Timed, Internet of Things (IoT)

## 1 INTRODUCTION

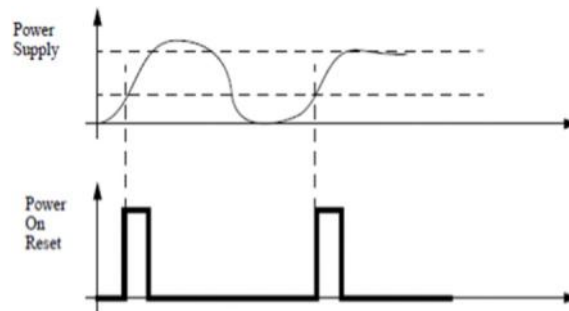
At the time of power-up, the POR signal generator senses a minimum threshold voltage, and generates a POR signal as shown in Figure 1. This POR signal is used to pre-set/reset the flip-flops, latches, and registers to a known state. The supply voltage for the POR circuit is the same as the SOC supply voltage. This presents a challenge because the POR circuit needs to operate while the supply is ramping up. Con-

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tionally, higher-voltage applications use a band-gap reference voltage to compare with supply voltage to generate the reset signal. As low-power devices continue to use supply voltages below the band-gap voltage, conventional POR circuit design becomes difficult. More specifically, the challenges occur as the supply voltage of low-power applications like IoT devices approaches the threshold voltage. Multiple factors increase the complexity of the POR circuit. Slow ramping supply voltage may not generate a POR signal with sufficient voltage level and pulse width to reset the logic circuit. Sharp supply rise times can extend the pulse width of the POR signal, even when supply has fully ramped up because of the longer reaction time of the circuit and the coupling capacitance with supply voltage. The circuit presented in this paper uses a self-timed circuit, to ensure that the reset signal pulse-width varies according to the time needed to reset the latch. The proposed circuit is designed to operate without any reference voltage, thus eliminating these limitations.

The supply voltage requirement of the SOC is based on the maximum supply requirement of all the components. The amount of on-chip decoupling capacitance is also designed based on regular circuit activity. However, at the time of power-up, unpredictable activity of the components causes the supply ramp-up rate to be non-linear. With technology scaling, process variation increases as device dimensions, threshold voltages, and supply voltages have decreased. Device simulation models fit to silicon behavior in limited voltage range, for example nominal voltage, with some tolerance. It is possible that a fully functional POR pulse generator operating in a simulation fails in silicon. To avoid such a situation, the POR signal generator must be simple, and must be thoroughly analyzed. To verify our design, we performed exhaustive simulations involving Monte Carlo tests on different PVT corners with a post-layout netlist. After that, we performed digital testing on silicon.



**Fig. 1.** General POR circuit waveform

This work is an extension of the POR circuit presented in [1]. We propose 2 circuits to set/reset latch at power up correctly.

1. Self-Timed POR circuit [1]
2. Latch based self-feedback POR circuit [2]

First the self-timed circuit is explained. Although it resolves the issue, it comprises of some limitations in terms of its implementation in all scenarios. The latch based self-feedback circuit resolves these issues based self-feedback circuit.

In summary, the major contributions of the proposed circuit are as follows:

- Removing the requirement for a reference voltage. This is useful for low-voltage applications
- Implementation of a self-timed circuit, to ensure that the reset signal pulse-width varies according to the time needed to reset the latch.
- Use of NAND latch in POR Circuit: - NAND gate resets with 0 voltage level which is the case for all the nodes at power up, making it easier to ensure reset at lower voltage level. Reset of the NAND latch is further used to reset all other latches in the design.
- Latch based self-feedback circuit: To resolve limitations of self-timed circuit.

The paper is organized as follows. Related Work is presented Section 2. Requirement of POR circuit in SRAM memories is explained in Section 3.1. Overview of the first proposed self-timed circuit is mentioned in Section 3.2. Detailed working of the self-timed circuit is provided in Section 4. Verification of the proposed circuits is presented in Section 5. Section 6 comprises of limitations of self-timed circuit and working of the self-feedback latch-based circuit to avoid these issues. Finally test-chip results and silicon validation are provided in Section 7, followed by conclusion in Section 8.

## 2 RELATED WORK

Researchers have been studying and developing POR circuits for a long-time because of their need in analog and digital integrated circuits (ICs). It began with traditional RC circuits, and then researchers explored the use of diodes, BJTs, and MOSFETs as circuit complexity increased [3, 4]. POR circuits are now used in various applications such as automotive and RFID tags [5, 6]. Further research in this field led to the development of circuits focused on low-voltage and low-power applications [7, 9, 13]. A current-source-based POR is also proposed in [12] for on-chip applications.

The circuits have been designed and enhanced to support multiple I/O power supplies [8]. Temperature, ramp-up rate, and threshold voltage variation affect the reliability of a POR circuit. Designs have been proposed in [10, 11] to overcome these variations and offer robust circuits.

Discrete ICs for POR functionality is available. However, designing on-chip POR offers an area reduction advantage. In this study, we propose an on-chip, self-timed, low-voltage POR circuit that is functional at a minimum of 400mV on 16nm FinFET technology. The technique uses multiple delay stages and uses a combination of coupling capacitances and resistor divider circuits to generate a reset signal. The area overhead of the POR circuit is minimal, the circuit uses no dynamic power during normal SOC operation, and the pulse width of the reset signal is self-timed.

### 3 OVERVIEW OF SELF-TIMED POR CIRCUIT

#### 3.1 Problem Statement

Conventional SRAM architectures have latches to latch data, address and other input signals. These latches are provided CLK input such that it resets the latch as desired for expected functionality. Hence POR circuit is not usually needed in such designs. In latch-based pseudo dual port SRAM memories [14], latches are used for portA but using latch for portB creates the need of POR circuit as will be explained in this section. To resolve this issue flip-flops can be used but at the cost of significant impact on area. Thus, latches were used instead of flip-flop for portB inputs to save area. Figure 2 shows NOR based SR latch that was used in dual/two port memories, to optimize the portB hold time and area. For dual port memories, CLK signal generates 2 internal clocks known as global timing pulse (gtp). Initially data for portA is passed through the mux by selecting the mux\_sel signal accordingly. Until then data for portB is latched. At power-up, it is essential that signal qi, which further generates clk\_latb and iclk for the latch operation is set to the desired state.

Figure 3 shows both cases where signal qi can be set to different values. When set to low level, data for portB is latched as expected because clk\_latb is low. When qi is set to high level, data for portB is not latched correctly. This will result in write failure for the first cycle. Since NOR latch needs a high pulse to reset it, conventional method of resetting it through delaying the supply at the input of NOR latch was showing failures in Monte Carlo simulations.

To resolve this issue, well-known solutions can be implemented but such conventional POR circuit has its own limitations and penalties. To have a high pulse which is enough to latch correctly, amount of required RC is huge. Hence RC and stage delay-based POR circuit costs a lot of area. Stage delay suffers from variability and need big area to provide a reasonable big delay at slow supply ramp. Voltage divider-based POR circuit suffers from significant DC current requirement and are analog in nature. These kind of Power-On-Reset circuits needs silicon validation and are not needed for memory circuits which are supposed to be simple in nature. Based on the mentioned analysis, we propose the following self-timed POR circuit which resolves the SR NOR latch problem and its use is not limited to this scenario.

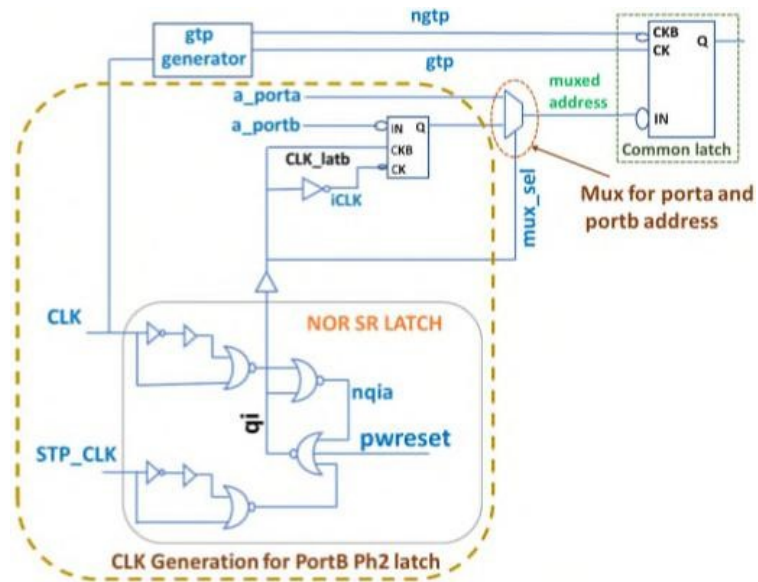


Fig. 2. POR requirement in latch-based pseudo dual port SRAM

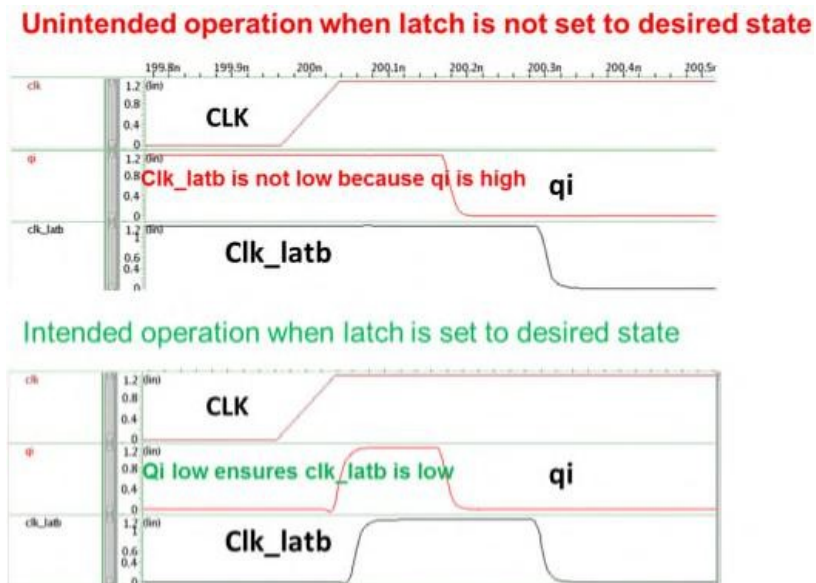


Fig. 3. Signal generation sequence for data latching

### 3.2 Self-Timed POR Circuit

Figure 4 shows the block diagram of the proposed self-timed POR circuit. Initially the supply to POR circuit is delayed by circuit explained in section 4A. When the supply is ramping up, PCTRL and NCTRL signals explained in section 4B and 4C respectively are low. The generation of PCTRL and NCTRL causes the RESET signal explained in section 3D to pulse HIGH which resets the SR latch. After this the feedback circuit switches the PCTRL and NCTRL signals high, such that POR signal remains low until next supply ramp up.

Figure 5 shows the detailed transistor-level diagram of the POR circuit. PCTRL is delayed as compared to the ramping supply. The feedback circuit also generates NCTRL, which prevents any DC current through the POR circuit. This enables the POR circuit to be used in low-power applications. When the supply is ramping up, capacitors C0, C1 and C2 couples with VDD and turns PCTRL and NCTRL signals low causing the latch to reset. After reset output NQ follows the supply, while Q stops following the supply voltage. NQ generates a feedback signal when the reset is complete. The feedback output switches PCTRL and NCTRL signals such that it makes NOR output independent of NQ. The circuit is self-timed, which means that the reset signal turns off depending on the delay of the circuit and the ramp-up time of the power supply. This will help in providing sufficient pulse width for the reset signal.

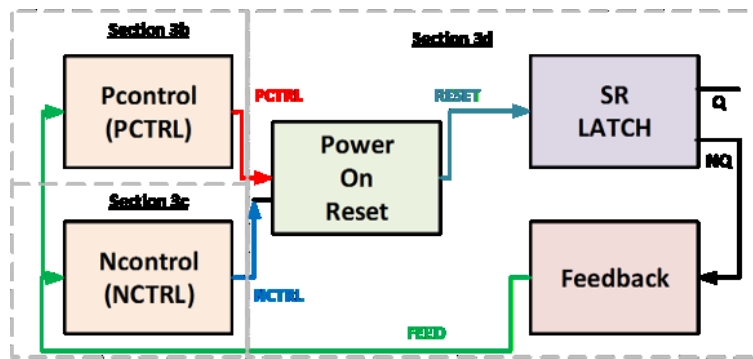


Fig. 4. Block Diagram of Self-Timed POR circuit components

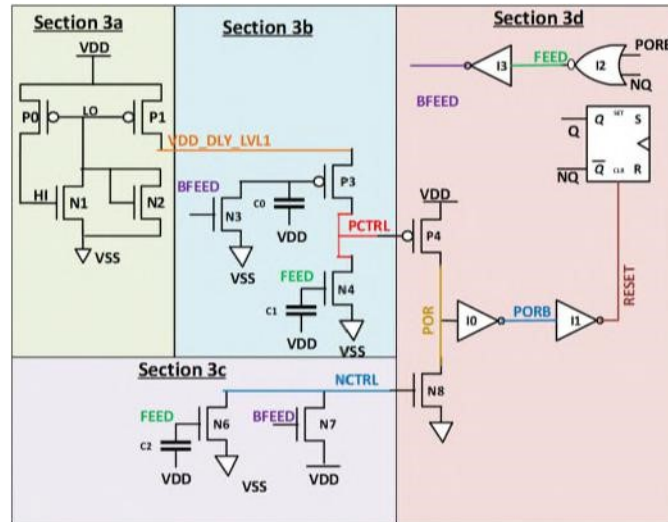


Fig. 5. Overview of Self-Timed POR circuit components

## 4 COMPONENTS OF SELF -TIMED POR CIRCUIT

### 4.1 Delayed VDD generation

Generation of delayed VDD is shown in Figure 6. The output of this circuit, VDD\_DLY\_LVL1, is used to generate a supply-delayed PCTRL signal. Before the power-up operation, all nodes in the circuit are at ground (VSS) level. When power-up begins, the supply starts ramping up, the LO node is coupled because of the Miller capacitance of P0 and P1. This delays the ramping of HI node which in turn helps LOW node to remain at high state. The Vds of the PMOS transistor P0 causes a slight delay in the HI node. The HI node voltage is much lower than the threshold voltage of the NMOS transistor when the ramp-up is slow delaying P1 conduction. The LO node falls with a delay, thus delaying VDD\_DLY\_LVL1 output supply. N2 acts as a clamping node in case the LO node is coupled higher than  $V_t$  as this would turn off the PMOS transistor.

### 4.2 PCTRL generation

Figure 7 shows that the VDD\_DLY\_LVL1 from Figure 6 and feedback circuit output FEED/BFEED from Figure 9 generate the PCTRL signal. This signal is also delayed with respect to the VDD supply. Initially at ramp up BFEED = '0', and FEED is ramping up. PCTRL is a delayed VDD signal because of coupling of capacitors C0 and C1 with VDD. When BFEED = '1', PCTRL follows VDD. PCTRL is delayed VDD because of three mechanisms. First, VDD\_DLY\_LVL1 is used as a source bias for the PMOS transistor P3, whose drain generates the PCTRL signal. The gate of the



transistor P3 is connected to coupling capacitance C0. The other node of the coupling capacitor C0 is connected to the supply. As the supply rises, the coupling capacitor makes the gate of the PMOS rise, thereby turning it off. The FEED node at the gate of the NMOS N4 of the PCTRL generator is coupled HIGH through the coupling cap C1. This causes some charge of the PCTRL to leak through the NMOS transistor.

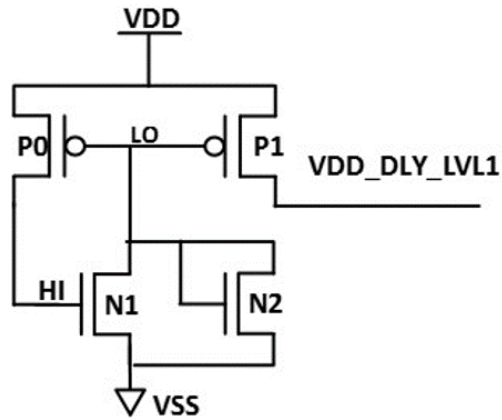


Fig. 6. Circuit for delayed VDD generation

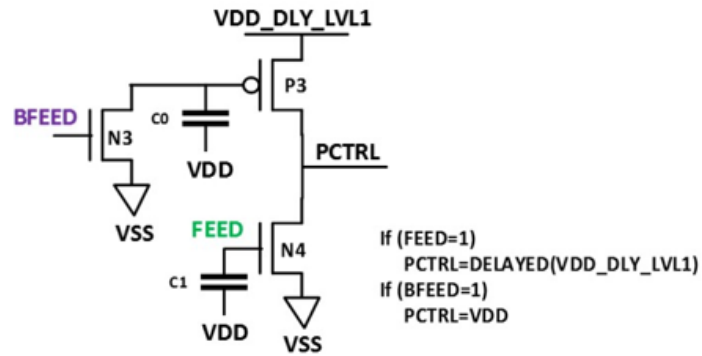


Fig. 7. Circuit for PCTRL generation

### 4.3 NCTRL generation

Figure 8 shows the circuit diagram for NCTRL signal generation. At power up, the BFEED signal is LOW while the FEED is coupled HIGH. FEED is coupled HIGH due to C2 as well as it being driven by feedback circuit in Figure 9. This ensures that at the start of supply ramp-up NCTRL signal remains at VSS. When the RESET operation is complete, the BFEED signal goes HIGH, making NCTRL go HIGH ( $VDD - V_T$ ) because of the NMOS N7.

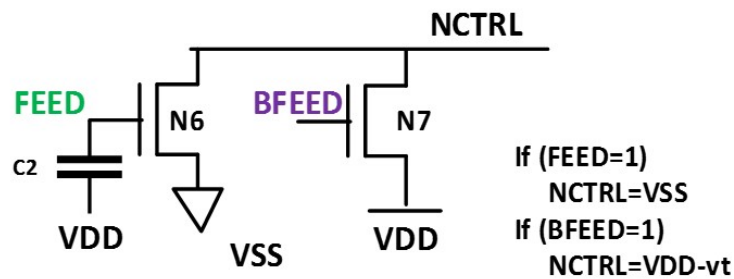


Fig. 8. Circuit for NCTRL generation

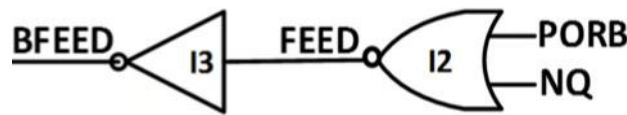


Fig. 9. Feedback Circuit

### 4.4 POR and the feedback circuit

The POR circuit is shown in Figure 10 which corresponds to Section 3d in Figure 5. PCTRL and NCTRL are the inputs to this circuit and the output is a reset signal for the SR latch. PORB and NQ signals are inputs to the feedback circuit shown in Figure 9. Since PCTRL is delayed with respect to the ramping supply, the POR signal which follows VDD is also delayed. After POR goes HIGH, then the SR latch RESET goes HIGH. When the SR latch is reset, the corresponding output Q becomes LOW and after the latching operation, output NQ starts following supply. As shown in Figure 9, logic NOR of NQ and the PORB signal generate a feedback signal. When reset is executed, the NQ signal goes HIGH making FEED go LOW and BFEED go HIGH.

The FEED and BFEED signals will switch the PCTRL signal HIGH, turning off the PMOS transistor P3 in Figure 7. Similarly, BFEED turns on the N7 transistor in Figure 8, making NCTRL go HIGH. Now, PCTRL, which is HIGH, and NCTRL,

which is also HIGH, turn off the reset signal as per the circuit in Figure 10. The PORB signal in the feedback circuit also turns HIGH.

When PORB turns HIGH, the state of reset, FEED, BFEED, and all other signals stay the same and becomes independent of NQ, making normal operation of SR latch independent of RESET signal. Based on process variation, the forward path, or feedback path, of the SR latch will make one of the nodes go HIGH and other go LOW. This state of the SR latch is probabilistic. If the state of the SR latch is as desired, an initial RESET pulse will be generated, which will do nothing to latch as it is already in the desired state. After some time, when NQ disables the RESET pulse operation, the SR latch will become independent of the POR circuit. If the state of the SR latch is not as desired, the initial HIGH pulse on the SR latch will make sure that the latch flips to the desired state, and afterwards the RESET pulse will be disabled. Since this is a simple feedback mechanism it doesn't need any reference voltage generation; hence it operates very well at low voltages. In proposed circuit, a feedback circuit is used. In case there are multiple flip-flops and latches that need to be reset, it is not possible to take feedback from all the latches. The circuit can be used in such cases as well. Instead of taking feedback from all the latch outputs, feedback will be still taken from a single latch. However, the output NQ of that latch will act as RESET signal for all the other latches. the feedback with a single latch will not be enough for timing if a reset signal is propagated through a buffer tree. This is resolved by considering worst RC distance for the POR latch. Additionally, the latch is skewed to account for variation and a buffer is inserted in the feedback path.

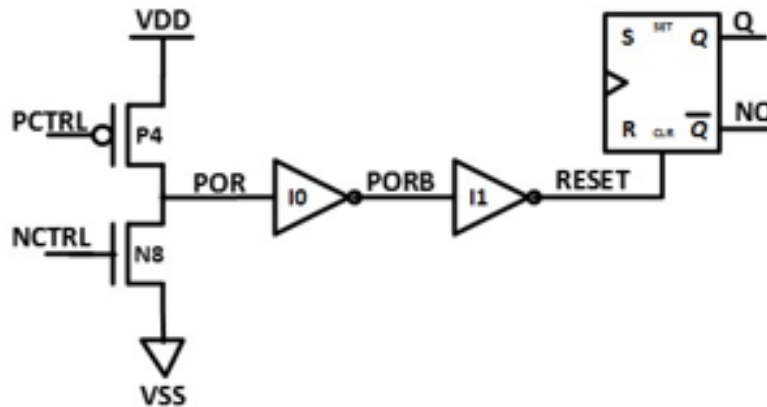


Fig. 10. Self-Timed POR circuit

## 5 SPICE VERIFICATION FOR SELF-TIMED POR CIRCUIT

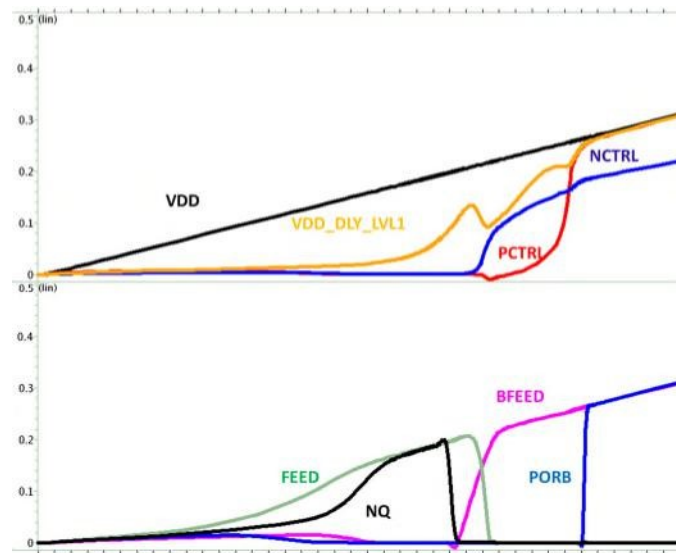
Figure 11 shows timing waveform from self-timed POR circuit simulation. All the internal signals along with the reset signal can be seen in the figure. The VDD signal is ramping up which generates the reset signal and turns PORB high. As mentioned earlier, factors such as temperature and process variation, device models, supply ramp-up rate, and supply noise increase complexity of the POR circuit. To make sure, that our proposed POR circuit functions correctly, we exhaustively verified it. For global variation, we took different global process corners and for local variation, we ran 5000 Monte Carlo simulations for each of the global corner with the criteria shown in Table 1.

**Table 1.** Simulation Criteria

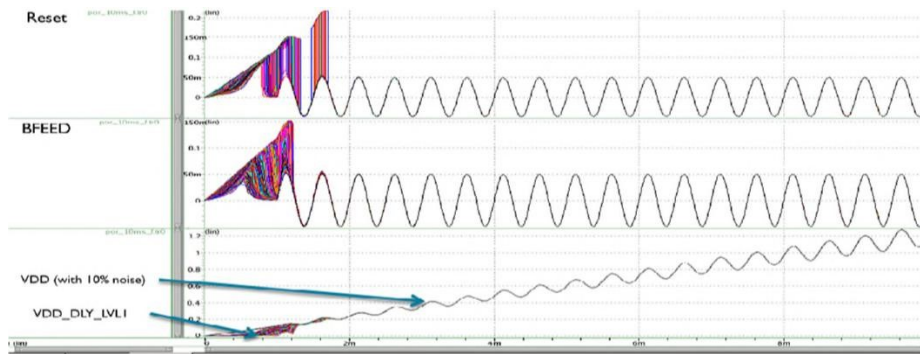
Simulation type	Post layout full chip extraction
<b>Supply ramp up time</b>	100ns, 1us, 1ms, 10ms
<b>Temperature</b>	-40c, 85c, 125c
<b>Supply Voltage</b>	0.4v, 0.51v, 1.2v
<b>Parasitic Extraction- RC extraction for metals</b>	-40c and 125c for worst R and worst C
<b>VSS noise</b>	50mV sinusoidal wave
<b>Supply noise</b>	Sinusoidal wave of 10% of instant supply value
<b>Process Corners</b>	SS, TT, SF, FF, FS
<b>Monte Carlo Simulations</b>	5000

On-chip or on-board supply and ground are not always ideal. They are susceptible to different kinds of variations and noises. For simulating noise at power up, we superimposed 50mV sinusoidal noise on VSS and 10% of instant supply sinusoidal noise on the supply for the POR block. As shown in Figure 12, when RESET or BFEED signals are at VSS level, 50mV noise is present. Also, the supply ramping up shows 10% instant supply value as noise in the VDD. As shown in Figure 11, when the BFEED signal switches from HIGH to LOW, after some delay. The reset signal also switches from HIGH to LOW. Before that, the RESET signal has

been following supply because of the POR circuit. 5000 Monte Carlo simulations returned zero defects. Different voltages, temperatures, and supply ramp-up slopes, supply and ground noise for different process split verify the working of the circuit.



**Fig. 11.** Simulated waveform for self-timed POR circuit



**Fig. 12.** MC simulations of POR with 10ms supply slope

## 6 LATCH BASED SELF-FEEDBACK POR CIRCUIT

To address dual/two port latch wrong initialization issue, if we use flip-flop for portB, we don't need power on reset circuit. That will not be area efficient for dual port ultra-high-density design where area is most important.

Although the self-timed circuit resolves the latch issue discussed in Section 3.1, it comes with some limitations. The proposed self-timed circuit is completely based on capacitive coupling. Since it was implemented on 16nm technology where advanced technology helped with the coupling, older technology nodes comparatively have lesser coupling capacitance. In some cases, at lower voltages, coupling might not be as desired for functional operation of the circuit. These issues can lead to limitation of the circuit to be used for older nodes. Here latch based self-feedback circuit is proposed which overcomes these limitations of the self-timed circuit.

Figure 13 shows the block diagram of self-feedback circuit. The idea is to receive feedback from the NOR SR latch, and provide a reset signal to the NOR latch using the NAND SR latch. As shown in the figure, the NAND SR latch uses delayed VDD. Figure 14 shows the detailed diagram for self-feedback POR circuit. Vdd is delayed using RC circuit and logic gates. A NAND SR latch is used after delayed supply Vdd. Since i/p of NAND latch, 'Vdd\_delay' starts with 0v, o/p 'pwreset' will follow Vdd, assuming when latch is in wrong state, nqia=low, feed will follow Vdd. NAND latch will fast latch the pwreset signal. Latched pwreset from NAND latch makes latching of NOR latch independent of logic delay in vdd\_delay.

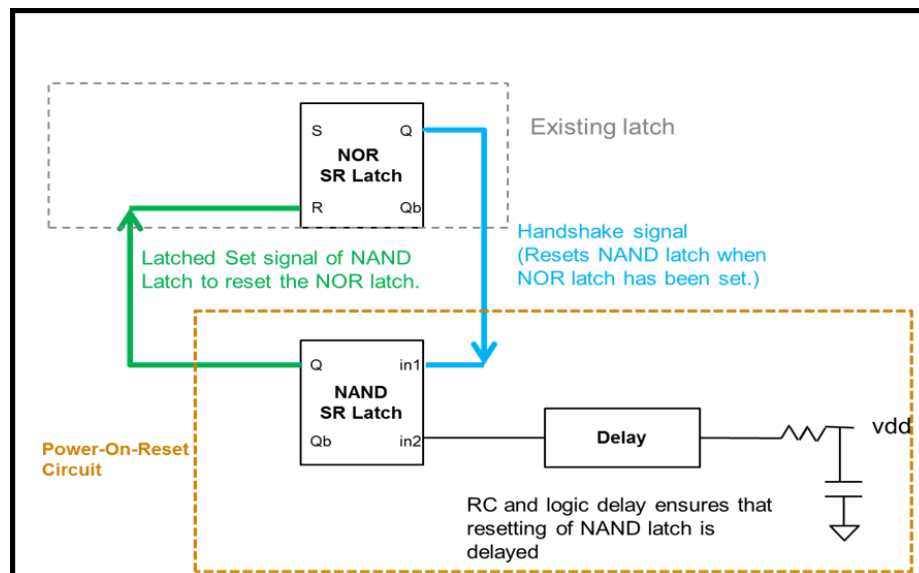


Fig. 13. Block Diagram for Self-feedback POR circuit

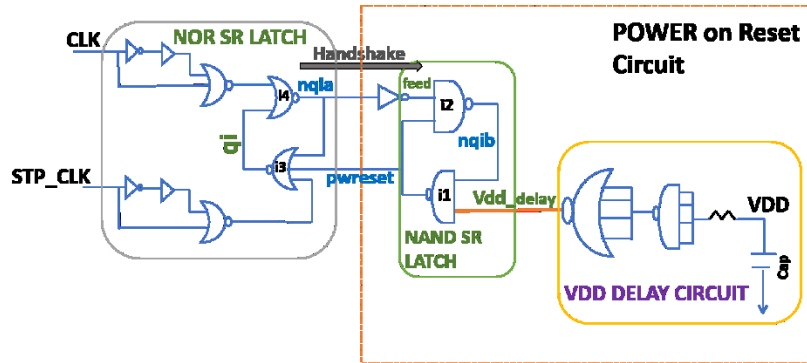


Fig. 14. Detailed Diagram for Self-Feedback POR Circuit

Figure 15 shows the simulated waveform for self-feedback circuit shown in Figure 14. As shown in the figure, initially nqia is low, once it goes high, feed signal turns low making nqib high. Once nqib turns high, the NAND gate i1 turns pwreset low. Pwreset signal stays low thus making nqia stay high. Our assumption is when latch is in wrong state, nqia=low, feed will follow Vdd but this assumption is not always correct. Nqia can initially follow Vdd before finally setting to wrong low state, and so feed is not following Vdd. In this case we do not get benefit of NAND latch.

Figure 16 shows a case where Vdd\_delay is not enough with circuit shown in Figure 14. This can lead to pwreset signal turning low earlier, further leading to make nqia signal stay low. If nqia signal stays low, portB data will not be latched as explained in Section 3A. To delay pwreset signal and make sure the circuit is functional, we increase the delay of Vdd\_delay going high. We do this by using Vdd\_delay as a supply to NAND i2 as shown in Figure 17. When feed is not following Vdd (is less than Vdd) and pwreset is also going high there is a current through resistive divider and vdd\_delay rising is delayed thus getting benefit of NAND

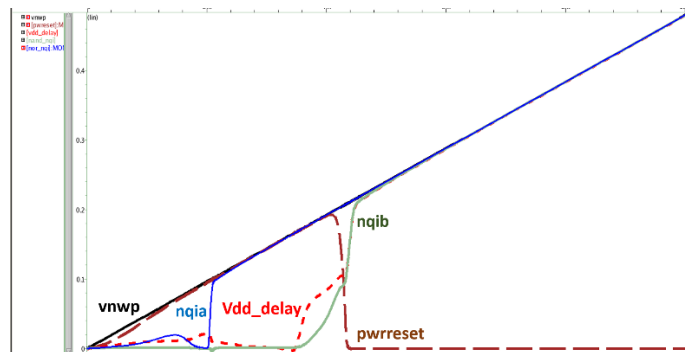


Fig. 15. Simulated waveform for self-feedback POR circuit

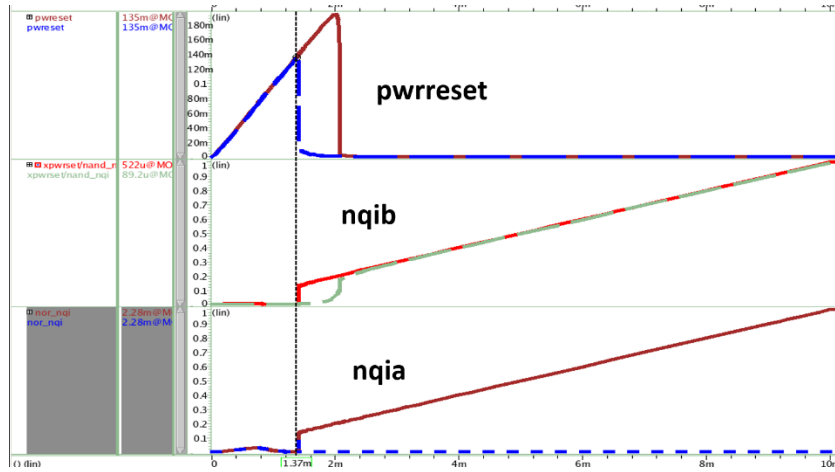


Fig. 16. Simulated waveform for pass and failure depending on nqia voltage level

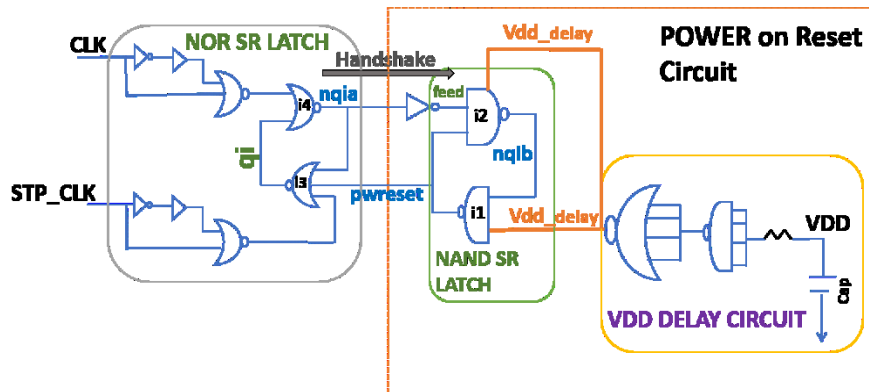


Fig. 17. Modified Self-Feedback POR circuit

The self-feedback circuit was tested and validated under stress conditions like self-timed POR circuit. The stress conditions are listed below: -

— Validation:

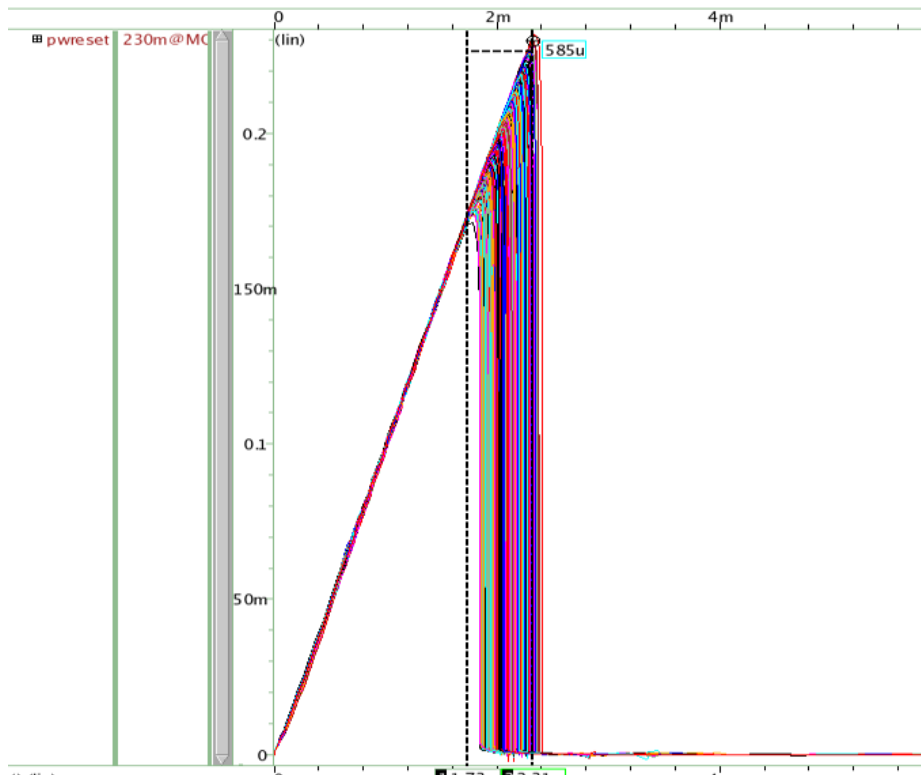
- Vddpe ramp-up slews (10ns,100ns,1ms)
- SS/FS/SF/FF with -40c/125c at low voltage and high voltage margin corners.
- 5000 Monte Carlo Simulations with not a single failure



— Stressed the circuit under below conditions:

- Connected vddpe to 4 I/p NAND and changed 4 I/p NAND and NOR gate to different VT mode.
- Skewed manually all gates 25% in opposite direction and ran 5k monte carlo.
- Added 10% of Vdd noise at pwreset signal and verified circuit.
- Added 10% of Vdd noise at Vdd\_delay signal and verified circuit.
- Added 20% of Vdd noise at input of NOR gate and monitor Vdd\_delay and pwrset with 4 I/p NOR and 3 I/p NOR gates.

Figure 18 and figure 19 shows monte carlo simulation results for the self-feedback results at 10msec and 100nsec slope of pwreset signal respectively. Both figures show that all the 5000 monte carlo simulations passed with the circuit show in figure 17.



**Fig. 18.** Monte Carlo simulation at 10msec slope of pwreset signal

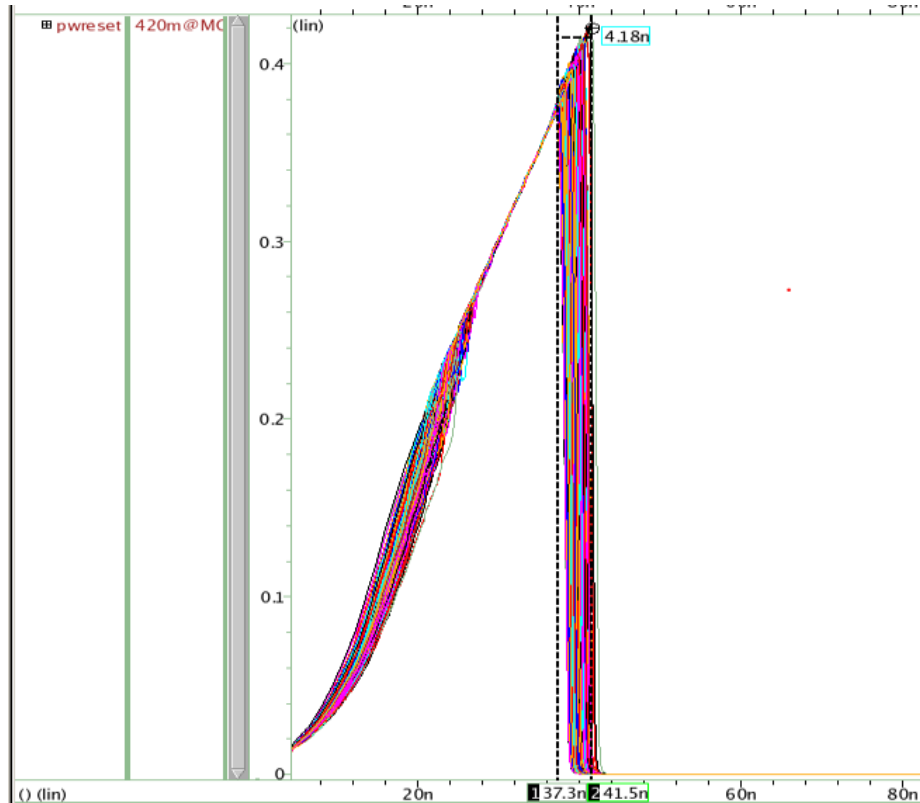


Fig. 19. Monte Carlo simulation at 10msec slope of pwreset signal

## 7 TEST CHIP AND SILICON TEST RESULTS

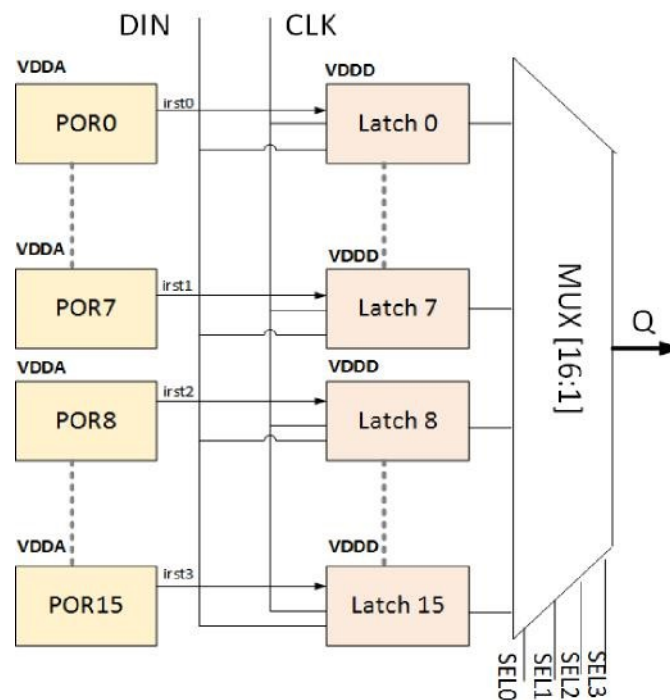
To do silicon validation of designed POR circuit and to get statistical yield data we designed and fabricated a POR validation IP. This IP consists of 16 samples of POR; it has two different latch structures which need to be reset. Figure 20 is the block diagram of POR validation IP. 16 latches, each associated with one POR circuit can be written parallel with the help of D and CLK pin. This is used to initialize the latch with a value opposite to the reset value. Output of 16 latches can be read serially through output Q of a 16:1 mux. The POR validation IP has two supplies: VDDD for digital latches and isolated supply VDDA for POR block. For testing purpose, it is important to initialize the latches. Since supply is ramping up for the POR circuit, we need to have 2 supplies, one of which VDDD is used to initialize, while VDDA is used to generate POR pulse.

We tested multiple samples per process split. For each process split we had 20 packaged chips, each packaged chip contains 16 POR circuits. In total, we tested 320

samples per process split. The process split included “SS, TT, FF, SF, and FS”. Based on the number of silicon samples tested on different process splits, we observed the self-timed POR circuit is fully functional at a minimum voltage of 400mv. Low voltage operation makes the POR circuit an attractive choice for low power applications like IoT. Also, the 400mv limitation is because of the SR latch. If sub-threshold flip-flops/latches are used, the circuit can be used even below 400mv. Figure 21 shows the timing diagram followed for testing of the POR circuit.

First, VDD is supplied and DIN and CLK is used to write a predetermined data into the latches. Then the data is read out serially by the Q pin. Figure 22, shows chip layout of POR validation IP fabricated in 16nm FinFET process.

Once that is done, power VDDA is provided with different ramp-up times and a reset signal is generated. POR circuit should overwrite previously written data in the latches. Once again, the data is read out of the latch to validate the working of the POR circuit. If the output Q of the MUX changes from are used to select data from a single latch amongst the 16 latches present. The self-feedback circuit was tested and validated under stress conditions like self-timed POR circuit.



**Fig. 20.** POR validation IP block diagram

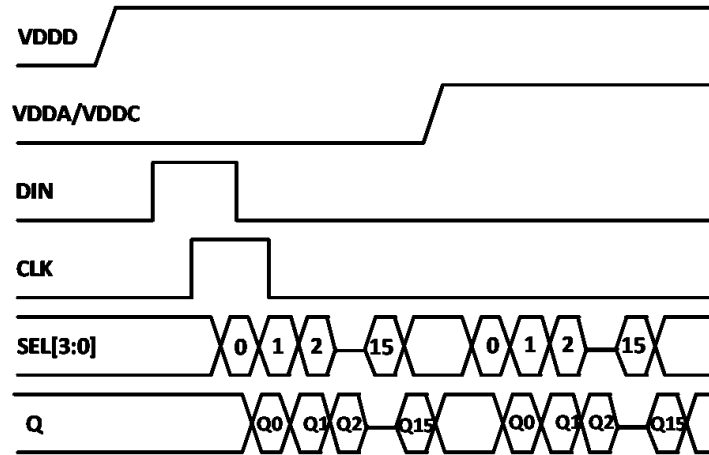


Fig. 21. Timing waveform for POR testing

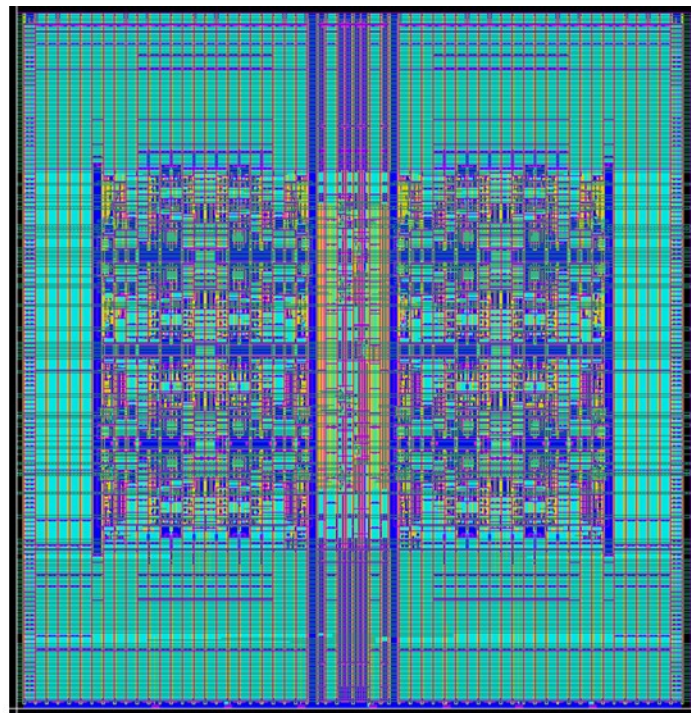


Fig. 22. 16nm chip layout

## 8 CONCLUSION

To initialize flops and latches, a POR circuit is needed. The circuit must work with different temperatures, process corners, process variation, supply ramp-up time, and supply noise. For low-power circuits such as IoT devices, the circuit must be functional at low voltages. A robust POR circuit is designed and exhaustive verification with SPICE models for several global corners and 5000 Monte Carlo simulations for local variations was done. In these simulations, the supply ramp-up time was varied from 100ns to 10ms, and supply and ground noise was introduced. The proposed POR circuit operates at low voltage and has no DC power consumption after the supply has ramped up. The self-timed pulse width of the reset signal varies with the time needed to reset the latch. In 16nm FinFET process, we fabricated a validation testchip and performed pass/fail testing of the POR circuit. We found 100% yield for samples of the POR circuit across different process splits, temperatures, and voltages. The circuit has minimal area overhead of  $21.3\mu\text{m}^2$ . Silicon validation, demonstrates that the proposed POR circuit works at a minimum supply voltage of 400mV.

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