The INRIA ZEP project: NVRAM and Harvesting for Zero Power Computations
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**The INRIA ZEP project: NVRAM and Harvesting for Zero Power Computations**

### ZEP project: Context and Objectives

- **Context**
  - The Internet of Things scenario predicts billions of communicating objects in a near future.
  - Maintenance cost and pollution issues are major bottlenecks for IoT.
  - Emerging non-volatile memory (NVRAM) technologies and harvesting techniques predict new kind of batteryless embedded sensors.
  - Checkpointing [1] of platform state will be a central technique in these systems.

- **Challenges**
  - Provide a new computation model adapted to NVRAM based micro-systems.
  - Master harvesting techniques and energy control in ultra-low power domain.
  - Provide real computer science contributions (language, compiler, operating systems, etc…).
  - Deliver innovative prototypes and a useful system-level simulator.

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**Expected Results**

- After 4 years, the project should have achieved the following:
  - A NVRAM based platform demonstrator powered by harvesting.
  - An innovating NVRAM based processor architecture designed for VLSI integration.
  - A solid system-level simulator for a generic NVRAM platform.
  - A compiler leveraging WCEC (Worst Cases Energy Consumption) analysis.
  - A primitive operating system including NVRAM management techniques and power management policies.
  - Publications of course…
  - Lobbying, communication, new research directions etc.

### References


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**Partners and Methodology**

- **Inria and CEA**
  - Inria, the French National Institute for computer science and applied mathematics, promotes scientific excellence for technology transfer and society. Inria is structured in research teams called project-teams.
  - CEA, the French Alternative Energies and Atomic Energy Commission is a key player in technological research for industry. CEA research institutes (List and Leti) are structured in research teams called labs.
  - Other institutes such as Insa-Lyon or University of Rennes are involved in Inria project-teams.
  - The ZEP project is an Inria Project Lab (PL), funded by Inria with more than 15 person-years hired over 4 years, including 3 PhDs. The Insa-Spie IoT Chair is also participating to the research effort of Citi Lab on IoT.

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**Work Packages**

- **Task 0: IPI management**
  - NVRAM architecture
  - Worst Case Energy Consumption
  - NVRAM OS
  - Demonstrators

- **Task 1: NVRAM-based Architecture**
  - NVRAM technology study
  - NVRAM-based sensor node platform
  - NVRAM-based processor architecture
  - NVRAM-based compiler optimization
  - NVRAM-based execution time energy evaluation

- **Task 2: Compiler Optimizations and Worst-Case Energy Consumption**
  - Energy Model: we will derive a precise energy model of a NVRAM-based processor.
  - Code Generation: we will provide a Worst Case Energy consumption (WCEC) driven code generation.
  - Checkpoints: The code generator could influence the checkpointing strategy.

- **Task 3: Runtime memory management**
  - Provide support to the NVRAM architecture: the runtime system will have to share the non-volatile memory across the various applications, according to their needs and priorities.
  - Choose how energy is used: energy policy must define the way the system should spend the available energy depending on the length of each task to execute for instance.
  - Ensure memory consistency: problems to be solved: processor state is volatile, devices’ states are volatile and a priority between applications when saving data of must be established [1].

- **Task 4: Experimental platforms and use cases**
  - Use cases: Use cases will include a sensing application, a cryptography application, and a video decoding application.
  - Experimental platform: the ZEP prototype will consist in the integration of recent FRAM from Texas Instrument (MSP430) and an FRAM-based MSP430FR5739 will provide a first and quickly available prototype.
  - Simulation platform: for more advanced design issues, we will use simulation tools provided by CEA (for L-IOT) and other vendors for NVRAM to provide a precise system-level simulator.