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# An Efficient Polarity Optimization Approach for Fixed Polarity Reed-Muller Logic Circuits Based on Novel Binary Differential Evolution Algorithm

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**Abstract.** The bottleneck of integrated circuit design could potentially be alleviated by using Reed-Muller (RM) logic circuits due to their remarkable superiority in power, area and testability. In this paper, we propose a Novel Binary Differential Evolution (DE) algorithm (NBDE) to solve the discrete binary-encoded combination optimization problem. Moreover, based on the NBDE, we propose an Efficient Polarity Optimization Approach (EPOA) for Fixed Polarity RM (FPRM) logic circuits, which uses the NBDE to search the best polarity under a performance constraint. To the best of our knowledge, we are the first to use DE to optimize RM circuits. The experimental results on 24 MCNC benchmark circuits show the effectiveness and superiority of EPOA.

## 1 Introduction

Traditional IC design based on the Boolean logic is facing serious power, area and delay challenges. Plenty of studies (e.g., [1-4]) demonstrate that compared with the circuits implemented by Boolean logic, the circuits implemented by RM logic are capable of achieving lower power and area. However, the existing polarity optimization approaches, which are based on GA or its variants, have a low convergence speed or are easily trapped into the local optimal solution [5-6].

In this paper, we propose a binary version of the Differential Evolution (DE) algorithm according to the polarity characteristic of FPRM logic circuits, called Novel Binary Differential Evolution algorithm (NBDE), to find the optimal solution in binary optimization space. Moreover, based on the NBDE, we propose an Efficient Polarity Optimization Approach (EPOA) for FPRM logic circuits, which uses the NBDE to search the best polarity.

## 2 An Efficient Polarity Optimization Approach for FPRM Logic Circuits

To enhance the global convergence ability, we introduce the elitism strategy to the NBDE. In addition, we propose a binary random mutation operator to increase the population diversity and improve the global searching ability.

### 2.1 Population Initialization

Firstly, a random number  $r$  is generated in  $[0,1]$ . Then, the  $j$ -th element of  $i$ -th individual  $x_{ij}$  is set to 1 (which represents polarity 1) if  $r$  is less than  $1/2$ ; otherwise,  $x_{ij}$  is set to 0 (which represents polarity 0).

### 2.2 Mutation Operator

To avoid the premature convergence and increase the population diversity, we propose a binary random mutation operator, which is represented as follows:

$$v_{i,j} = \begin{cases} x_{i,j} + (-1)^{x_{i,j}} \cdot |x_{r2,j} - x_{r3,j}|, & rand \geq 0.5 \\ x_{best,j} + (-1)^{x_{best,j}} \cdot |x_{r2,j} - x_{r3,j}|, & rand < 0.5 \end{cases} \quad (1)$$

where  $v_{i,j}$  represents the  $j$ -th element of mutation vector  $v_i$ .  $r2, r3 \in \{1, 2, \dots, NP\}$  and  $r2 \neq r3 \neq i$ .  $x_{best}$  is the optimal individual in current population, and  $rand$  is a random number in  $[0,1]$ .

Since the polarity of FPRM expression is taken as 0 or 1, the absolute value of difference vector is only 0 or 1 and the mutated variable is still 0-1 variable. Therefore, the mutation operator satisfies the closure. Moreover, whether one dimension variable can be mutated or not depends on the difference vector. Specifically, the  $x_{i,j}$  or  $x_{best,j}$  can be mutated (from 0 to 1 or from 1 to 0) when  $|x_{r2,j} - x_{r3,j}| = 1$ , which could increase the population diversity, improve the global searching ability and prevent the algorithm trapping into the local optimal solution. In addition, the probability of  $x_{r2,j}$  is equal to  $x_{r3,j}$  is increasing along with the population evolution. The  $x_{i,j}$  or  $x_{best,j}$  remain the same when  $|x_{r2,j} - x_{r3,j}| = 0$ , which could accelerate the convergence speed.

## 3 Experiments Results

The EPOA has been implemented in C and compiled by the GNU C compiler. The results were obtained by using a PC with Intel Core i7 3.40GHz with 4G RAM under Linux. In this paper, we set the logic minimization as the polarity optimization goal to validate the effectiveness of the EPOA.

We compared the EPOA with the GA based Polarity Optimization approach (GAPO) [7] and Whole Annealing GA based Polarity Optimization approach (WAGAPO) [8] on 24 randomly selected MCNC benchmark circuits. Moreover, we

ran the GAPO, WAGAPO and EPOA 10 times on each circuit to reduce the impact of randomness on the results. The population size is set to 100, and termination criterion is that there is no improvement on the optimal solution in population over 10 iterations.

The comparison of GAPO, WAGAPO and EPOA on the average number of iterations and run time (in CPU seconds) over 10 independent run are listed in Table 1. Columns 9 and 10 denote the percentage of the number of iterations and run time saved by EPOA compared to GAPO. Columns 11 and 12 denote the percentage of the number of iterations and run time saved by EPOA compared to WAGAPO.

**Table 1.** Comparison of GAPO, WAGAPO and EPOA on the average number of iterations and run time

Name	Input	GAPO		WAGAPO		EPOA		Save1(%)		Save2(%)	
		iter	time(s)	iter	time(s)	iter	time(s)	iter	time(s)	iter	time(s)
b3	3	1	0.20	1	0.18	1	0.03	0.00	85.00	0.00	83.33
xor3	3	1	0.19	1	0.18	1	0.05	0.00	73.68	0.00	72.22
bw	5	6	0.96	3	0.42	1	0.06	83.33	93.75	66.67	85.71
xor5	5	8	0.82	4	0.57	1	0.05	87.50	93.90	75.00	91.23
m1	6	12	1.18	4	0.61	1	0.06	91.67	94.92	75.00	90.16
Z5xp1	7	12	1.22	5	0.63	1	0.06	91.67	95.08	80.00	90.48
lin	7	14	7.34	6	3.70	1	0.14	92.86	98.09	83.33	96.22
ex5	8	15	2.85	8	1.44	2	0.37	86.67	87.02	75.00	74.31
m3	8	14	2.21	6	1.28	3	0.55	78.57	75.11	50.00	57.03
rd84	8	22	14.92	7	5.62	4	0.62	81.82	95.84	42.86	88.97
1020	10	24	23.03	9	7.76	6	4.60	75.00	80.03	33.33	40.72
ex1010	10	20	15.78	12	6.14	7	4.81	65.00	69.52	41.67	21.66
br1	12	31	17.02	16	9.37	8	3.44	74.19	79.79	50.00	63.29
14_4color	14	55	30.08	23	15.26	10	7.05	81.82	76.56	56.52	53.80
table3	14	70	37.40	27	18.70	18	11.62	74.29	68.93	33.33	37.86
dk48	15	62	36.32	26	16.43	20	9.59	67.74	73.60	23.08	41.63
alcom	16	69	67.85	31	34.41	23	17.53	66.67	74.16	25.81	49.06
table5	17	81	84.99	52	52.90	31	22.42	61.73	73.62	40.38	57.62
src1	18	73	173.55	37	139.34	29	54.63	60.27	68.52	21.62	60.79
in2	19	84	158.64	41	127.88	33	32.26	60.71	79.66	19.51	74.77
mark1	20	127	240.91	40	195.61	30	60.75	76.38	74.78	25.00	68.94
mux	21	95	226.33	34	174.26	27	68.90	71.58	69.56	20.59	60.46
duke2	22	116	262.72	45	223.15	34	75.18	70.69	71.38	24.44	66.31
cordic	23	145	318.05	67	257.18	42	95.84	71.03	69.87	37.31	62.73

Compared with the GAPO, the greatest improvement in the number of iterations and run time, which were made by EPOA, are 92.86% and 98.09%, respectively.

Moreover, compared with the WAGAPO, the greatest improvement in the number of iterations and run time, which were made by EPOA, are 83.33% and 96.22%, respectively.

## 4 Conclusion

In this paper, we propose a novel binary DE algorithm, called NBDE, which can solve the binary-encoded combination optimization problem. Additionally, based on the NBDE, we propose a polarity optimization approach, called EPOA, which uses the NBDE to search the best polarity of FPRM logic circuits. The experimental results over MCNC benchmark circuits show that the EPOA performs better than, or at least comparable to, the existing GA or its variants based polarity optimization approaches in terms of solution accuracy and convergence speed.

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## References

1. He, Z X., Xiao, L M., Ruan, L.: A Power and Area Optimization Approach for Mixed Polarity Reed-Muller Expressions for Incompletely Specified Boolean Functions. *Journal of Computer Science and Technology*, vol.32, no.2, (2017) 297-311
2. Ma, X J., Li, Q Y., Zhang, J L., Xia, Y S.: Power Optimization Technique Based on Dual-logic Diagram Expression at Gate Level. *Journal of Computer-Aided Design & Computer Graphics*, vol.29, no.3, (2017) 509-518
3. He, Z X., Xiao, L M., Gu F.: An Efficient and Fast Polarity Optimization Approach for Mixed Polarity Reed-Muller Logic Circuits. *Frontiers of Computer Science*, (2017) 1-15
4. Rahaman, H., Mathew, J., Pradhan, D K.: Secure Testable S-box Architecture for Cryptographic Hardware Implementation. *Computer Journal*, vol.53, no.5, (2010) 581-591
5. Wang, P J., Wang, D S., Jiang, Z D.: Area and Power Optimization of ISFPRM Circuits Based on PSGA Algorithm. *ACTA ELECTRONICA SINICA*, vol.41, no.8, (2013) 1542-1548
6. He, Z X., Xiao, L M., Zhang L B.: EMA-FPRMs: An efficient minimization algorithm for fixed polarity Reed-Muller expressions. *International Conference on Field-Programmable Technology*, (2016) 253-256
7. Sun, F., Wang, P J., Yu, H Z.: Ternary FPRM Circuit Area Optimization Based on Genetic Algorithm. *Journal of Shandong University (Natural Science)*, vol.48, no.5, (2013) 51-56
8. Yang, M., Almaini, A.E.A.: Optimization of Mixed Polarity Reed-Muller Functions Based on Whole Annealing Genetic Algorithm. *Journal of Fudan University (Natural Science)*, vol.52, no.3, (2013) 303-308