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IBIS-AMI based PAM4 Signaling and FEC Technique for 25 Gb/s Serial Link

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Abstract. This paper investigates Input/Output Buffer Information Specification Algorithmic Model Interface (IBIS-AMI) model extension for 25Gb/s PAM4 (4-level Pulse Amplitude Modulation) serial link to improve the development efficiency. By using the ADS (Advanced Design System) Channel Simulator, the effects of device package, jitter and crosstalk on the actual performance are studied at first. Then, for forward error correction (FEC) technique, the bit error rate (BER) performance and the bathtub curves are analyzed in detail. Simulation results show that device package, jitter and crosstalk can make the link performance worse. And much better performance can be obtained by using the combination of equalization and FEC techniques compared with using the equalization technique separately.

Keywords: IBIS-AMI Model, PAM4, FEC, Reed-Solomon (RS) Code, Bit Error Rate (BER)

1 Introduction

To meet the increasing demand of data rate and overcome the bandwidth limitation of channel, PAM4 (4-level Pulse Amplitude Modulation) signaling [1-2], as an alternative of NRZ (non-return-to-zero), has drawn more and more attention in high-speed serial link systems, especially for backplane applications. For example, it has been adopted for some aspects of the 400 Gb/s Ethernet standard [3]. However, the high complexity of PAM4 transceiver contributes to the low development efficiency, as well as the increasing simulation time. Furthermore, this may pose a challenge to the whole system simulation since system engineers may not have a lot of experience with PAM4 link design.

An effective approach to shorten the developing time of PAM4 serial link system is to adopt Input/Output Buffer Information Specification Algorithmic Model Interface (IBIS-AMI) [4-5], which allows an encapsulated transceiver model by defining a common serial model interface. Furthermore, AMI simulation allows designers to run millions of bits to predict a link performance accurately at low BER level since an efficient convolution method which can be used to calculate signal waveforms at channel output is employed in it.

This paper investigates the IBIS-AMI model extension for PAM4 serial link. Not only the device package [6] but also the jitter and crosstalk [7] are considered in the model to evaluate their impacts on the actual performance. Furthermore, Forward Error Correction (FEC) technique, which is commonly combined with certain advanced equalization techniques in the serial link, is also introduced to improve the bit error rate (BER) performance.

The rest of the paper is organized as follows. In Section 2, we construct the IBIS-AMI model for PAM4 link. Section 3 introduces FEC technique to improve BER performance. In Section 4, we present the simulation parameter and platform for PAM4 link. Section 5 analyzes the performance of our proposed link. Finally, we draw conclusions and discuss future work in Section 6.

2 IBIS-AMI Modeling for PAM4 Link

Figure 1 presents a simplified end-to-end serial link system. It can be seen that a pseudo random binary sequence (PRBS) is first modulated into PAM4 signaling by a modulator (MOD). Then, a feed forward equalizer (FFE) is adopted to compensate the high frequency loss of channel at the transmitter side (Tx). For the receiver (Rx), decision feedback equalizer (DFE) is employed to equalize the receive signal with inter-symbol interference (ISI), outputting equalized data into a de-modulator (DeMOD). Although some equalization techniques have been applied to remove ISI, it is hard to achieve the desired BER, *e.g.* 10^{-12} or below. To improve the BER performance, some FEC techniques such as Reed-Solomon (RS) or BCH code can also be employed.

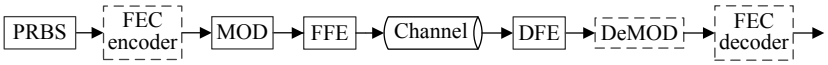


Fig. 1. An end-to-end serial link system

In order to accurately simulate the serial link, IBIS and AMI should be modeled for Tx and Rx separately as illustrated in Figure 2, where IBIS defines termination electrical characteristics for Tx output and Rx input buffers, while AMI concerns the algorithm model employed in Tx and RX, such as modulation, FFE and DFE.

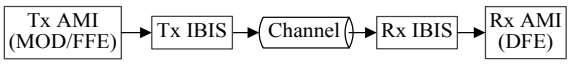


Fig. 2. IBIS-AMI modeling of link system

2.1 IBIS for Tx and Rx

Generally, IBIS model mainly concerns input/output buffer electrical characteristics and package information. For IBIS buffer there are three data tables: *i*) Voltage-Time (V-T) tables for transition speed, *ii*) Current-Voltage (I-V) tables for nonlinear termination resistance and PowerClamp/GroundClamp for clamping feature, *iii*) C_comp section for lumped capacitance.

As shown in Figure 3, we can see that RisingRamp/FallingRamp, Pullup/Pulldown, PowerClamp/GroundClamp and C_comp are considered for Tx buffer, while PowerClamp/GroundClamp and C_comp are included for Rx buffer. It can also be observed that device package is modeled as a network of resistance (*R*), inductance (*L*) and capacitance (*C*).

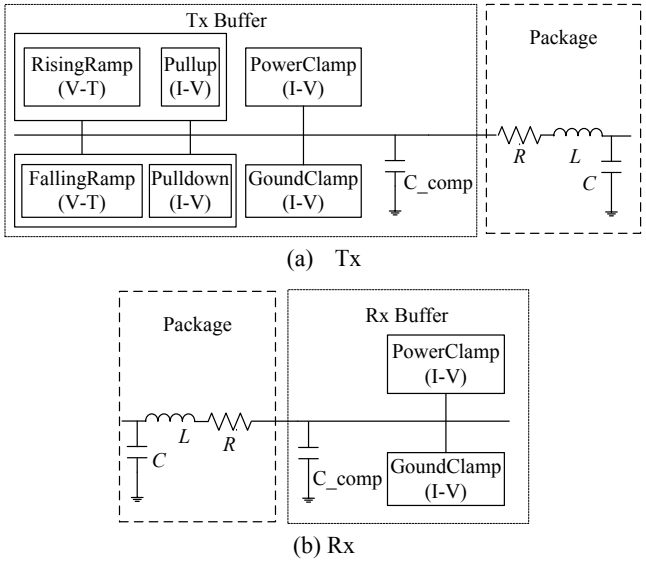


Fig. 3. IBIS buffer and package

2.2 AMI Parameter and Simulation Mode

Different from IBIS, AMI mainly concerns the algorithm models in the transceiver. Therefore apart from a section Reserved_Parameter which is used to describe some pre-defined parameters, another section Model_Specific for user-defined parameters is also included in Tx/Rx AMI parameter. Figure 4 only indicates Tx AMI parameter list. The Boolean values of Init_Returns_Impulse and GetWave_Exists in the Reserved_Parameter depend on whether the algorithm model is linear time-invariable (LTI) or not. For example, for Tx AMI, the values of these two parameters are true and false respectively since FFE is a linear element, while they are false and true for Rx AMI because DFE is a nonlinear one.

Meanwhile, several optional parameters in the Reserved_Parameter such as Tx_Jitter and Tx_DCD are also provided to model various Tx jitters. Use_Init_Output and Max_Init_Aggressors are used to define the AMI_Getwave input and the maximum number of aggressor, respectively.

In the second section, *i.e.* Model_Specific, the items FFEcoefficients and PAM4 define the tap coefficients of FFE and modulation scheme, respectively.

The AMI simulation mode also depends on the algorithm characteristic of FFE and DFE. See Table 1, when the algorithm is LTI, both statistical and bit-by-bit are supported in the function of AMI_Init. Otherwise, only bit-by-bit mode is supported

by AMI_GetWave. In the latter case, AMI_Init is only used to set up the parameters and allocate memory for AMI_GetWave. As a result, bit-by-bit simulation mode is chosen in ADS Channel Simulator.

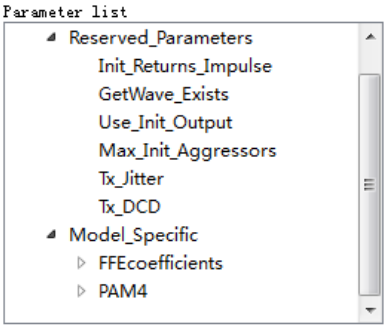


Fig. 4. Tx AMI parameter list

Table 1. IBIS-AMI simulation mode

Algorithm characteristic	Init_Returns_Impulse	GetWave_Exists	Simulation mode	Interface function
LTI	True	False	Statistical & Bit-by-Bit	AMI_Init
non-LTI	False	True	Bit-by-Bit	AMI_Init and AMI_GetWave

2.3 AMI Model Extension for PAM4 Signaling

Let's consider Tx first. A 4-tap FFE is used which can be modeled as a four-tap finite impulse response (FIR) filter in AMI_Init function, *i.e.*:

$$y[n] = \sum_{i=0}^{M-1} w_i x[n - iN] \tag{1}$$

where $x[n]$ and $y[n]$ denote input and output sample data, respectively, w_i and M denote tap coefficients and tap number, respectively. N is the number of samples per bit, which is passed through the SamplesPerBit in the AMI_Init function.

Default NRZ stimulus uses [-1/2|1/2] to represent logic low and high, respectively. For PAM4, however, four stimulus levels are needed. So some current IBIS-AMI standards need to be extended for PAM4 signaling. We use [-0.5 | -0.5/3 | 0.5/3 | 0.5] to represent logic levels -3, -1, 1 and 3, respectively. Thus, by converting the original NRZ bit pattern to a PAM4 one, the simulator can generate a stimulus square wave according to the above mapping scheme.

Another modification is about Rx DFE slicer levels [8-9]. We need to add TSL, MSL and BSL (top/middle/bottom slicer level) to the reserved parameter list. Figure 5 shows the block diagram of a PAM4 DFE with TSL, MSL and BSL. For simplicity, MSL can be fixed at 0 and TSL=−BSL=0.5*2/3=1/3. As mentioned earlier, when

considering its nonlinearity, Rx AMI is required to return TSL and tap coefficients (C_i) through AMI_Parameter_Out string for each AMI_GetWave call.

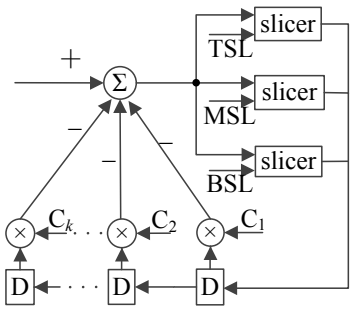


Fig. 5. Block diagram of PAM4 DFE

3 Forward Error Correction (FEC)

As required bandwidth increase, the increasing link rate poses a challenge for the serial interface communication [10]. Therefore, data rate 400 Gb/s [11] attracts the attention of some groups for next-generation Ethernet development, such as IEEE and OIF. In the research process of 400 GbE, a number of FEC options have been proposed and discussed with the aim of achieving the desired BER performance. See Table 2, BCH (2858, 2570) can provide a coding gain of 3.8 dB at BER of 10^{-12}, while the coding gain for RS (528, 514), RS (536, 514) and RS (544, 514) over GF(2^{10}) are 5.28 dB, 5.97 dB and 6.39 dB at 10^{-13} BER, respectively. Obviously, RS codes are more attractive for their high coding gains compared with BCH code.

In this paper three RS codes are employed for high-speed serial link to evaluate the improvement in BER performance.

Table 2. Coding gain comparisons

FEC scheme	Coding gain (dB)	Data rate (Gb/s)	Target
BCH(2858, 2570)	3.8	111.875	400 GbE@10^{-12} [12]
RS(528, 514)	5.28	25.78	400 GbE@10^{-13} [13]
RS(536, 514)	5.97	26.17	
RS(544, 514)	6.39	26.56	

4 System Simulation

4.1 Simulation Parameters

In this paper, two backplane channels A and B are simulated. Figure 6 depicts the frequency response of the two channels and their combinations with a package model

in which the equivalent *R*, *L* and *C* value at the Nyquist frequency is 40 mΩ / 1.1 nH / 0.7 pF, respectively. In addition, Figure 6 also shows far end crosstalk (FXET) and next end crosstalk (NEXT) for channel B. We find that with the frequency increasing, the crosstalk especially the NXET interference has a more remarkable influence on the transmission link. Table 3 lists their insertion loss (IL) for PAM4 at 25 Gb/s and

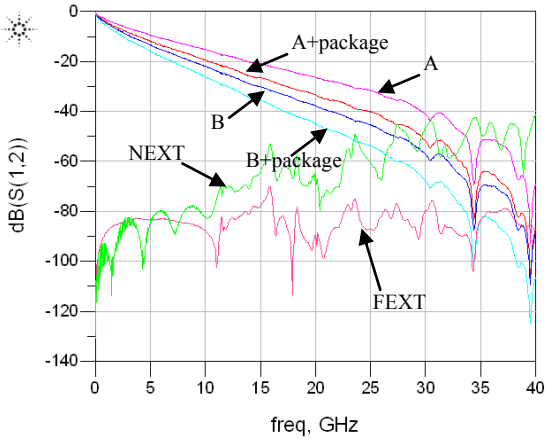


Fig. 6. Frequency responses of Channel

Table 3. Channel insertion loss

Channel	Insertion Loss (dB)	
	6.25 GHz	12.5 GHz
A	10.98	18.2
B	15.7	26.1
A + package	14	23
B + package	18.7	31

Table 4. Simulation parameter

Data Pattern	PRBS31
Symbol Rate	12.5 Gbaud
Tx Launch	1 V diff p2p (0.5 V diff pk)
Modulation Scheme	[2/3,0,1/3]
Tx/Rx Package	Pkg35mm_T21mm115ohmHiXtalkBGAHiXtalk.s8p
Tx DCD	0.04 UI
Tx RJ	0.01 UI
Rx RJ	0.01 UI
NEXT	TEC_Whisper42p8in_Meg6_NEXT_B5B6_C8C9.s4p
FEXT	TEC_Whisper42p8in_Meg6_FEXT_B5B6_C8C9.s4p

50 Gb/s.

Table 4 summarizes the simulation parameters. The symbol rate and the peak-to-peak magnitude of NRZ, as the launching signal, are 12.5 Gbaud and 1 V, respectively. Then, the modulation scheme [2/3, 0, 1/3] can realize the signal conversion. For the device package and the crosstalk, they are given in the form of S-parameter. As for the jitter, the Tx duty cycle distortion (DCD) and random jitter (RJ) and the Rx RJ are 0.04 UI, 0.01 UI, 0.01 UI, respectively.

4.2 PAM4 Simulation Platform

An IBIS-AMI serial link simulation platform based on ADS is established which contains the transmission channel and crosstalk channel, shown as Figure 7. In the transmitter, Tx_AMI module generates a PRBS31, and maps the signal into PAM4 pattern, and then sends it to FFE. Following the Tx_AMI module is the package. In Rx_AMI, attenuated signal is received and equalized with DFE. An eye probe is attached to the Rx_AMI component to display the eye diagram as an oscilloscope. Various jitters can also be added by AMI reserved parameter Tx_Jitter and Rx_Jitter.

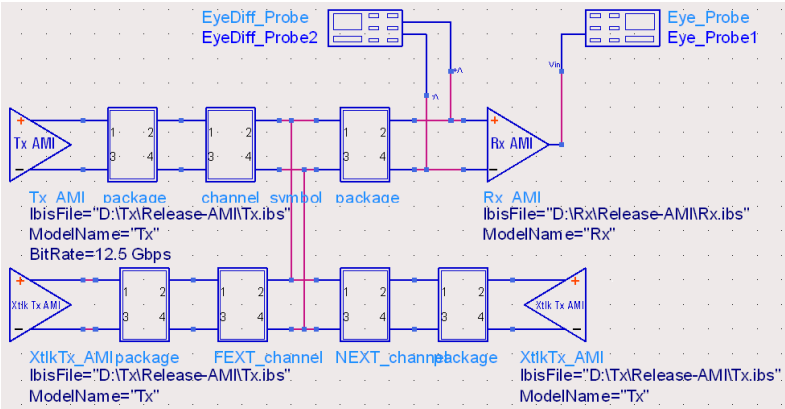


Fig. 7. IBIS-AMI simulation platform

5 Results Analysis

5.1 Eye Diagrams

Figure 8 gives the simulation results of eye diagram, in which Figure 8(a)~(d) represent the case of channel B, channel B with package, channel B with package and jitter, and channel B with package, jitter and crosstalk, respectively. We can see that when only channel loss is considered, the output eye diagram is the best since ISI introduced by channel is well mitigated by equalization. After DFE, the horizontal and vertical opening of eye diagram can be up to 45.4 mV and 37.96 ps.

When only device packages are added into the link, the horizontal opening and the vertical opening reduce to 36 mV and 36.4 ps in the receiver. It is because that device

package can aggravate ISI, making the eye worse. When jitter is also injected into the link, the eye becomes smaller further with a horizontal and vertical opening of 32.8 mV and 34.6 ps, respectively. Finally, when all these impairments are present, more ISI is introduced, making the eye almost closed. In this case only FFE and DFE cannot satisfy the BER requirement and FEC can be applied to improve the link performance.

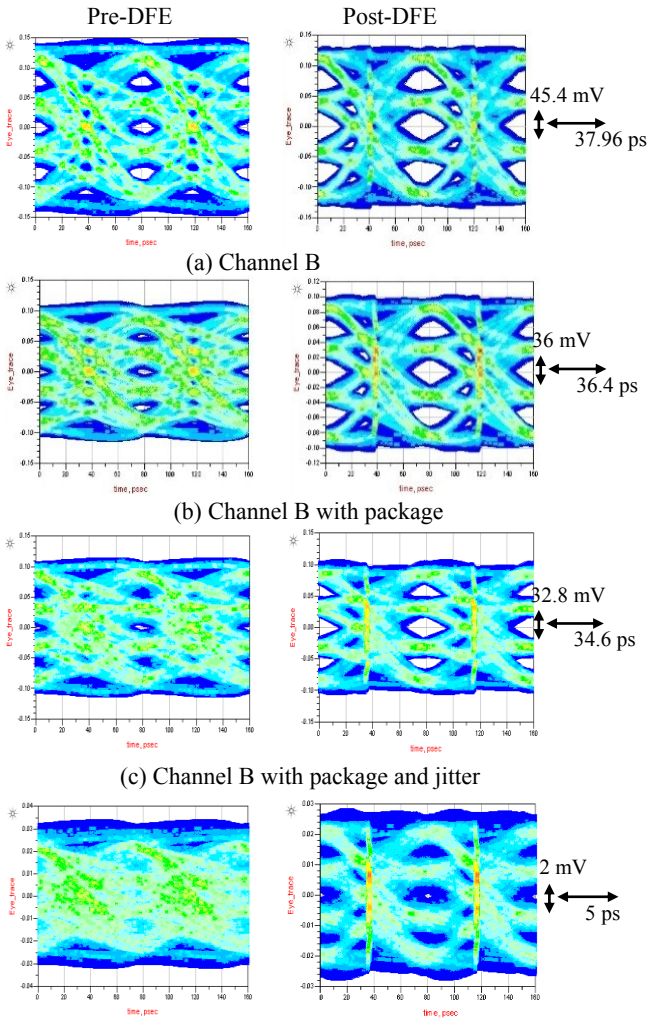


Fig. 8. Eye diagram simulation results

5.2 BER Performance

Figure 9 shows BER versus SNR (signal-to-noise ratio) for RS codes (528, 514, 7), (536, 514, 11) and (544, 514, 15). The y-axis of Figure 9 and Figure 10-11 in the 5.3

section is base 10 logarithmic. From Fig.9, we learn that RS code can significantly lower the output BER at the same SNR, namely achieving a better performance in the receiver. We can also see that RS codes with error correcting capability t=7, 11, 15 can provide approximately 6 dB, 6.75 dB, 7.25 dB coding gain at the BER of 10^{-15}, respectively. This explains that RS codes with larger t can always obtain larger coding gain than those with smaller t.

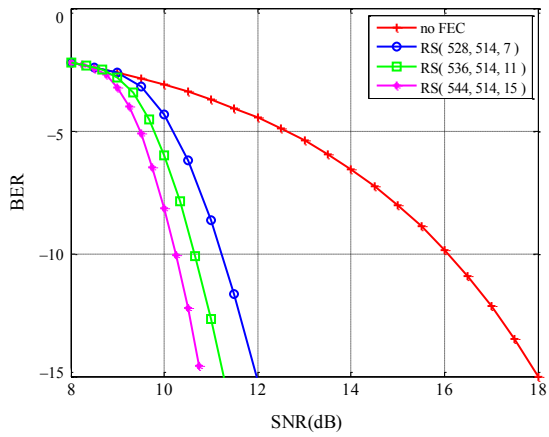
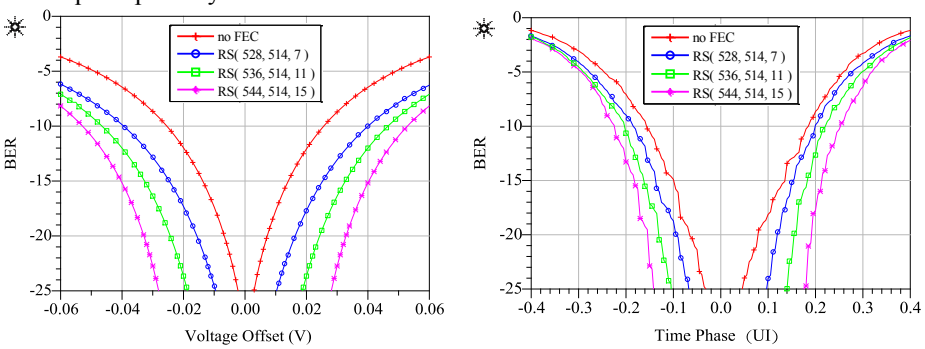


Fig. 9. BER performance

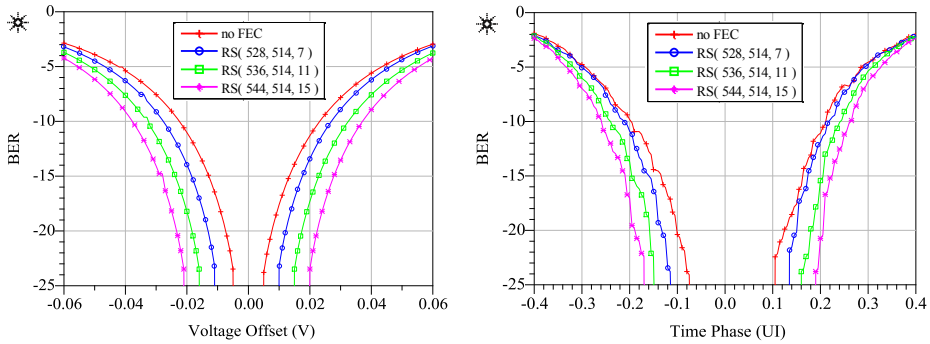
5.3 Bathtub Curves

Based on the previous analysis, the equalizer and FEC techniques are employed to evaluate the link performance through the bathtub curve. Shown as Figure 10 and Figure 11, their voltage bathtub curve and timing bathtub curve with three RS codes are plotted for channel A and B respectively. It is obvious that the better performance margin can be achieved by RS code with larger t. This explains the combination of the equalization technique and RS code performs better than the equalization technique separately.



(a) Voltage Bathtub curve (b) Timing Bathtub curve

Fig. 10. Bathtub curves for channel A



(a) Voltage Bathtub curve (b) Timing Bathtub curve

Fig. 11. Bathtub curves for channel B

6 Conclusions and Future Work

In this paper, the simulation link of a 25 Gb/s PAM4 link system over backplane channel is constructed with IBIS-AMI model. By using the ADS Channel Simulator, the effects of device package, jitter and crosstalk on the actual performance are studied, which is shown to continually decrease the eye opening. Meanwhile, the combination of the equalization and FEC techniques are studied with the bathtub curve. As expected, their combination performs better than the equalization technique separately.

In the future, a trade-off between complicated equalization and FEC coding will be studied for the optimization of the link performance. Moreover, transcoding [14] will be considered to reduce total overhead, as well as discuss the trade-off between the overclocking and the link performance margin. This can provide a design guide on improving signal reliability for 400 GbE.

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