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Yinhang Zhang, Qingsheng Hu, Yongzheng Zhan. A 20 Gb/s Wireline Receiver with Adaptive CTLE and Half-Rate DFE in 0.13 μm Technology. 15th International Conference on Wired/Wireless Internet Communication (WWIC), Jun 2017, St. Petersburg, Russia. pp.292-303, 10.1007/978-3-319-61382-6_24 . hal-01675415

HAL Id: hal-01675415

<https://inria.hal.science/hal-01675415>

Submitted on 4 Jan 2018

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A 20 Gb/s Wireline Receiver with Adaptive CTLE and Half-rate DFE in 0.13 μm Technology

Yinhang Zhang, Qingsheng Hu^(✉), and Yongzheng Zhan

Institute of RF- & OE-ICs, Southeast University,
Nanjing, 210096, China
736671385@qq.com, qshu@seu.edu.cn

Abstract. This paper presents a 20 Gb/s receive equalizer including an adaptive continuous time linear equalizer (CTLE) and a 2-tap half-rate decision feedback equalizer (DFE) in 0.13 μm BiCMOS technology for high speed serial link. The CTLE can adjust the ratio of high frequency and low frequency components adaptively by detecting the energy at both ends of a slicer and then generating a control signal by an integrator. Following the CTLE is a half-rate DFE which can get a better trade-off between the working speed and design complexity especially for the case of 20 Gb/s or above. The chip area including pads and chipguarding is about $0.72 \times 0.86 \text{ mm}^2$ and the power consumption is about 528 mW. Post simulation results show that the horizontal eye opening of the equalized data can be up to 0.9 UI at 20 Gb/s.

Keywords: CTLE · DFE · Serial link · Design complexity

1 Introduction

The requirement of high data rate in wire-line communications has been becoming more and more intense. The chip-to-chip and board-to-board communication are moving towards 20 Gb/s or above. The channel loss, jitter, cross-talk and noise will become more and more serious with the increase of velocity [1-3]. In order to compensate channel loss or combat the inter-symbol interference, a variety of equalization schemes are widely used at the near or far end. Partial response maximum likelihood equalization based on sequence detection can find the most probable transmission sequence from all possible sequences and get the lowest bit error rate [4, 5]. Because the structure of Viterbi decoder is too complex, and difficult to implement with high speed circuit, it is seldom used in high speed serial link.

In the receiver, the feed forward equalizer (FFE) has a simple structure and can cancel pre-cursor ISI and post-cursor ISI simultaneously. At high speed, e.g. 20 Gb/s or beyond, it is difficult to design high precision delay line which is easily affected by the process, voltage, temperature (PVT) [6-8]. Similarly, the continuous time linear equalizer (CTLE) can also eliminate the pre-cursor and post-cursor by increasing the high-frequency components of the signal. But the noise and crosstalk is potentially amplified by the CTLE [9, 10]. DFE is a nonlinear structure and it is the most effec-

tive equalizer to eliminate the post-cursor. In order to eliminate the influence of the previous symbol on the current symbol, the previous symbol is fed back and subtracted from the current symbol. Since the feedback signals are hard decision signals, the feedback signals do not enhance crosstalk and noise. The structure of DFE equalizer is simple and easy to operate at relatively high rate. [11-14].

The reminder of the paper is structured as follows. We review the principle of the adaptive CTLE based on the slope detection and the half-rate DFE. Then, the circuit design of the key modules is introduced in Section 3. We give the circuit layout and post-simulation results in Section 4. Finally, we draw conclusions in Section 5.

2 Arcitecture

The overall structure consists of an adaptive CTLE and a half-rate DFE, as shown in Fig. 1. Adaptive CTLE can provide high frequency gain and compensate the loss caused by channel bandwidth degradation. In addition, CTLE can not only make up for some of the shortcomings of DFE, but also reduce the number of taps, which reduces power consumption [15-17]. Due to the inherent drawbacks of linear equalizers, it is necessary to follow a half-rate decision feedback equalizer.

Due to the change of the environment, the different backplane materials and the change of the data rate, the improvement of the adaptive ability of CTLE is absolutely necessary. For the adaption CTLE based on spectrum balancing method, the power detector consumes large power. In order to solve these problems, the adaptive CTLE based on slope detection is presented in this paper, as shown in Fig. 2. The signal transmitted through the channel is first sent to a linear equalizer which has two paths: high-pass path and all-pass path. The high-pass path is used to compensate the high-frequency loss by high-frequency peaking, and the all-path is employed to adjust the low-frequency gain. The optimum proportion of high frequency and low frequency is adjusted by feedback control voltage V_{ctrl} . The output of the linear equalizer is adopted to produce a fixed swing and slope signal by the slicer. Slope detector & integrator are used for detecting the slope (energy) deviation between the slicer input and its output.

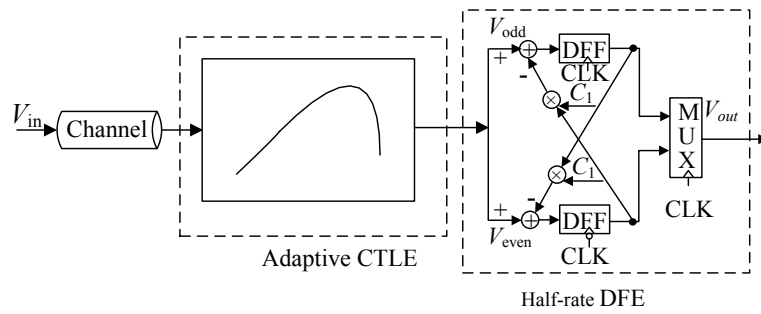


Fig. 1. A typical equalization architecture with CTLE and Half-rate DFE

3 Circuit Design

3.1 Linear equalizer

Linear equalizer is mainly used to compensate the loss caused by channel bandwidth degradation. The design of linear equalizer must consider two issues: 1) bandwidth, which determines the range of frequency compensation; 2) boost factor, which is determined by the loss of the channel [17]. The linear equalizer shown in Fig. 5 employs a high-path and an all-path path to compensate the loss of the channel. The bandwidth of high-path is completed by the inductance peaking technique and the bandwidth of the all-path is expanded by pole zero cancellation. The ratio of high frequency and low frequency is determined by the bias voltage of the tail transistor. In other words, the adaptation of the linear equalizer is performed by the feedback control voltage V_{ctrl} , which is produced by the slope detector and integrator. Fig. 6 shows the frequency response curve of the linear equalizer with different V_{ctrl} .

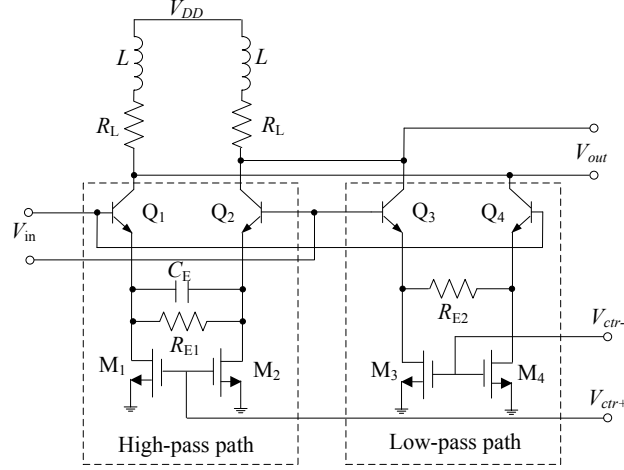


Fig. 5. Linear equalizer

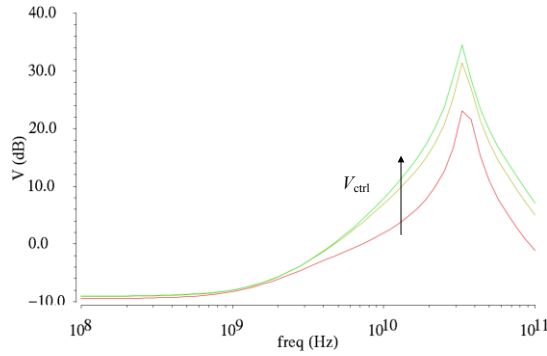


Fig. 6. Frequency response of linear equalizer with different V_{ctrl}

3.2 Slope detector and integrator

Fig. 7 shows the slope detector & integrator. Two coupled difference pairs, M_1 and M_2 , M_3 and M_4 , are used to detect the energy of the slicer input and output, respectively. The total current flowing through the coupled differential pair M_1 and M_2 can be expressed as follows:

$$I_{out1} = I_{ds1} + I_{ds2} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right) \left(2(V_{in,cm} - V_{in})^2 + \frac{V_{in,dm}^2}{2} \right) \quad (1)$$

where the I_{ds1} and I_{ds2} are the drain current of transistor M_1 and M_2 , respectively. $V_{in,com}$ is the common mode input voltage and $V_{in,dm}$ is the differential mode input voltage. The square term in the formula shows that the energy of different slope signal waveforms can be measured by I_{out1} . In Fig. 7, M_6 and M_7 are active load transistor, M_5 and M_6 are mirror current source, similarly, M_7 and M_8 are mirror current source. Therefore, the feedback control voltage generated by the integrator can be described as follows:

$$V_{ctrl} = I_{out2}R_L - I_{out1}R_L = \frac{\mu_n C_{ox}}{4} \left(\frac{W}{L} \right) (V_{in2}^2 - V_{in1}^2) R_L \quad (2)$$

According to Eq. (2), V_{ctrl} is closely related with the difference of slicer both ends signal energy. The V_{ctrl} feeding back to the linear equalizer adjusts the frequency response of the linear equalizer.

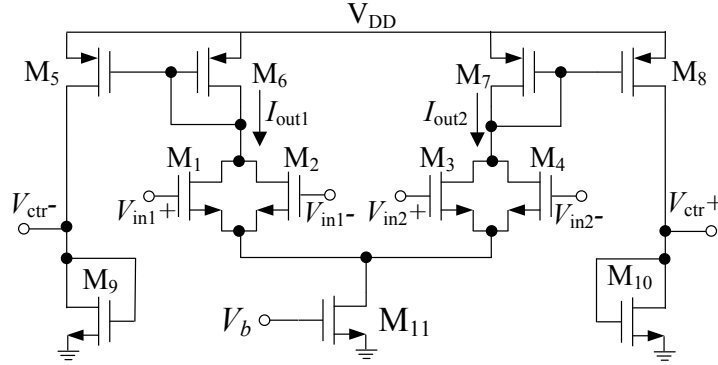


Fig. 7. Slope detector and integrator

3.3 Slicer

Slicer implemented by two cascaded current mode logic (CML) structure is shown in Fig. 8. The slicer is a limiting amplifier so that it processes the edge and amplitude of the input signal and produces fixed swing and slope signal for the feedback loop. The slicer is a high resolution comparator. The edge of the input signal is processed into

an approximate ideal binary signal, so that the slope of the slicer output is almost independent of the slope of the equalizer output signal.

3.4 SCFL based Latch

The sensitivity of latch has a great influence on the performance of DFE. The D Flip-Flop consists of two stages latches. Each stage latch contains three pairs of transistors, as shown in Fig. 9. Q_1 and Q_2 are input clock transistors, Q_3 and Q_4 consist of sampled transistors, Q_5 and Q_6 are latch transistors. When the CK_p/CK_n is high/low, the Q_1 is turned on and the Q_2 is turned off, the current I_{ss} flows through the Q_1 , and the data is sampled. When CK_p/CK_n is low/high level, the output signal is latched by the latch transistor, the data remains intact.

For latch, firstly, the size of clock signal must be large enough to ensure that the Q_1 or Q_2 can be turned off completely. Secondly, the performance of the latch is determined by the proportional relation between the latch transistor and the sampling transistor. Considering the operating speed, data retention capability and bandwidth, the proportional relation adopted in this design is 0.8.

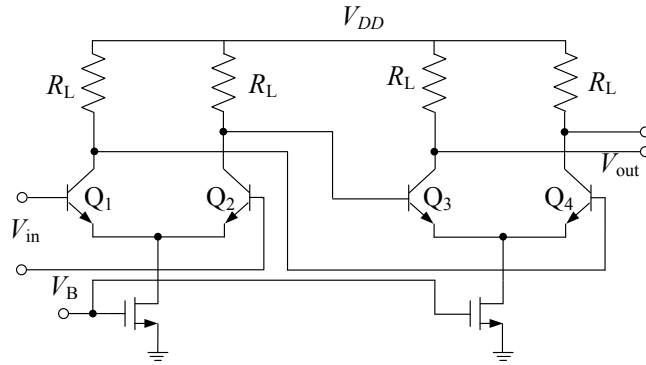


Fig. 8. Slicer

3.5 Summer

The summer based on CML is shown in Fig. 10. The input signal V_{in} and its feedback signal are summed up in the form of current, and then converted into the output voltage V_{out} . The V_{out} can be expressed as follows:

$$V_{out} = [G_0 V_{in}(t) - G_1 V_{in}(t - T) - G_2 V_{in}(t - 2T)] R_L = [C_0 - C_1 - C_2] I_{ss} R_L \quad (3)$$

where $G_i(i=0,1,2)$ are the input transconductance, $C_i(i=0,1,2)$ are the tap coefficients. In order to effectively eliminate the post-cursor and achieve a good equalization effect, it is important to select the appropriate tap coefficients $C_i(i=1,2)$. Typically, it can be obtained by the impulse response of the channel or the adaptive least mean square (LMS) algorithm.

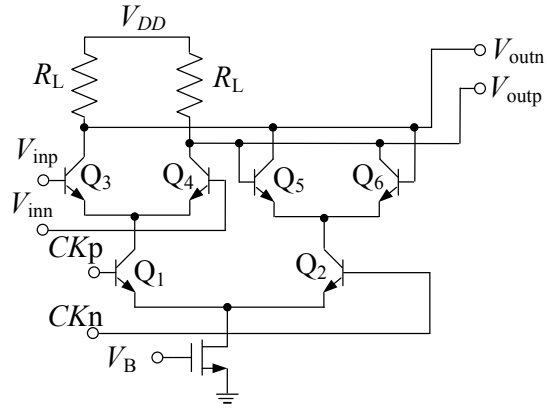


Fig. 9. SCFL based Latch

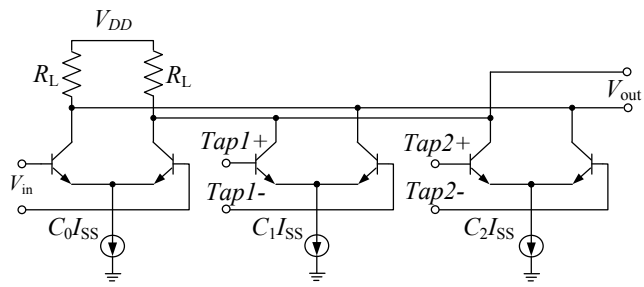


Fig. 10. Summer

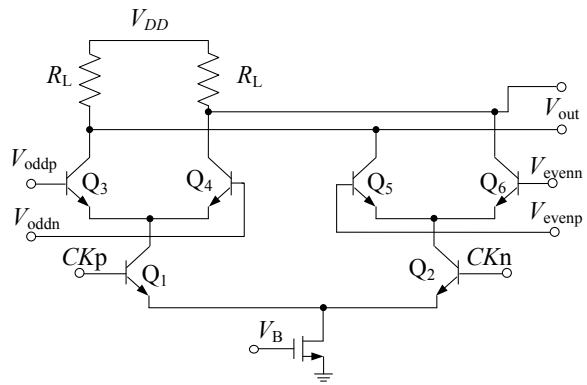


Fig. 11. Multiplexer

3.6 Multiplexer

Fig. 11 shows the architecture of multiplexer. The 2:1 multiplexer based on SCFL is mainly composed of two cross coupled differential pair transistor. This circuit is driven by half-rate clock, which is same as the master slave flip-flop. The half-rate data can be recovered to full rate data through this circuit. When the CK_p is high, the odd path is selected. When the CK_n is high, the even path is selected. In order to improve the stability of current source, the gate length of the tail current transistor should be larger.

3.7 Buffer

To drive external 50 ohm load resistance, the buffer based on CML logic was implemented in this work, as shown in Fig. 12. It is composed of multi-stage CML logic. It has the advantage of simple structure and enough bandwidth. In order to improve the driving ability, this paper adopts 3 stages. The size of tail current transistor and difference input transistor should be gradually increased, and the size of load resistance should be reduced gradually.

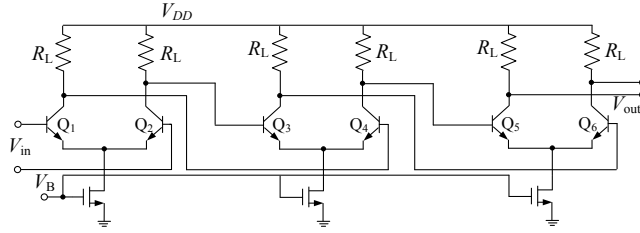


Fig. 12. Buffer

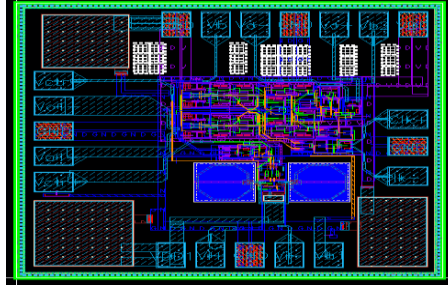


Fig. 13. Layout of the proposed equalizer

4 Layout and Post Simulation

Fig. 13 shows the layout of the proposed equalizer including adaptive CTLE and half-rate DFE. The total area including pads and chipguarding is $0.72 \times 0.86 \text{ mm}^2$. The

circuit has been submitted for fabrication. Fig. 14 shows the simulation results of feedback control voltage $V_{\text{ctrl}+}$ and $V_{\text{ctrl}-}$. It can be seen that the feedback control voltage can be stable after 5 ns.

Fig. 15(a) gives the input eye diagram. The output eye diagram of adaptive CTLE and half-rate DFE are given in Fig. 15(b) and Fig. 15(c), respectively. It can be seen that the eye opening is less than 0.6 UI after adaptive CTLE equalization, and the eye opening can be further widened by half-rate DFE at the rate of 20 Gb/s.

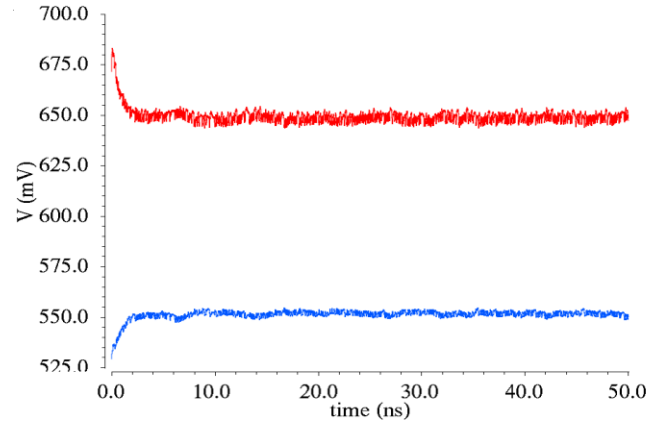
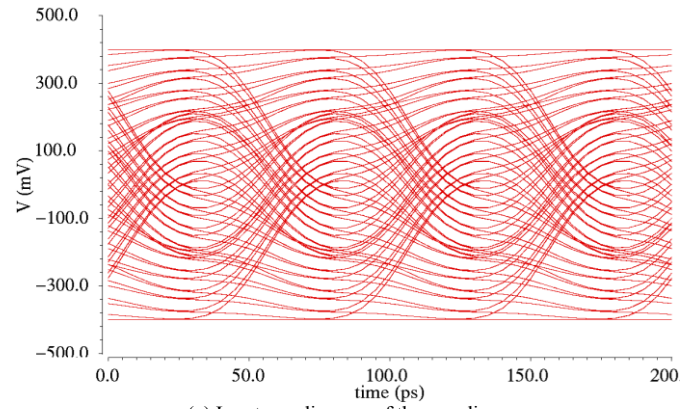
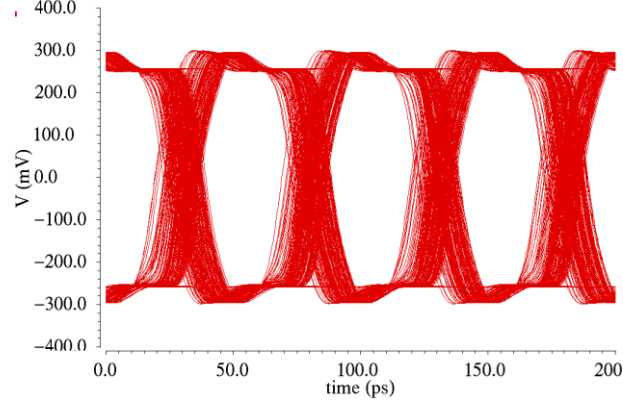


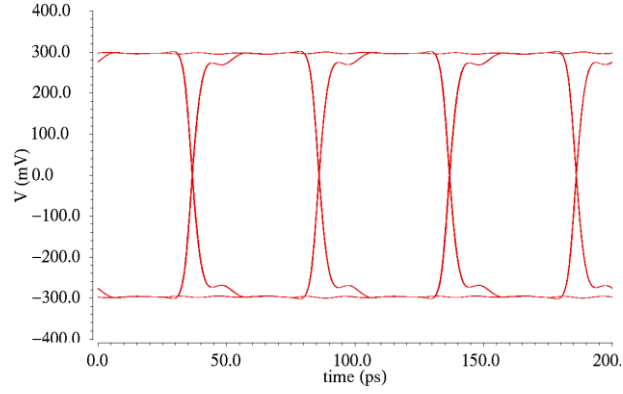
Fig. 14. Simulation results of feedback control voltage ($V_{\text{ctrl}+}$ and $V_{\text{ctrl}-}$)



(a) Input eye diagram of the equalizer



(b) Output eye diagram of the adaptive CTLE



(c) Output eye diagram of half-rate DFE

Fig. 15. Simulation results of 20 Gb/s

5 Conclusions and Future Work

In this brief, in order to deal with higher channel loss, a half-rate DFE combined with an analog adaptive CTLE based on slope detection is employed at the receiver. The adaptive CTLE can adjust the range of high-frequency peaking and compensate the channel loss. It can effectively reduce the burden of DFE and cut down the number of taps. Eye opening is up to 0.9 UI after the CTLE and half-rate DFE equalization at 20 Gb/s. It improves that the half-rate DFE can further improve the signal integrity of serial link at the rate of 20 Gb/s.

In future work, on the one hand, because the ISI is mainly caused by the post-cursor, we will focus on the adaption performance of DFE. On the other hand, when the loss of the link reaches up to 35 dB attenuation at Nyquist frequency at 25 Gb/s or above, higher order modulation mode (such as PAM4), or other modulation methods (such as ENRZ) should be deeply studied.

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