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A Broadband Power Amplifier Applied in GSM/TD-SCDMA/WLAN System

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Abstract. A broadband power amplifier operating from 0.8GHz to 2.4GHz is designed in 0.13-μm SiGe HBT process. The power amplifier adopts pseudo-differential structure, adaptive bias control technique, broadband matching network and compensated matching technique to optimize linearity, efficiency and bandwidth. The simulation results show that the maximum power gain is 25 dB, 3-dB bandwidth is 690MHz - 2470MHz. P1dB, P_{sat} and PAE are better than 26dBm, 29dBm and 38%, respectively. The chip area of DAC occupies 2.56mm^2 with pads.

Keywords: SiGe-HBT · Broadband power amplifier · Adaptive bias control · Pseudo-differential

1 Introduction

In past few decades, GaAs HBT (heterojunction bipolar transistor) has been a proper technology to design power amplifier (PA) which has excellent efficiency and linearity [1], but it is hard to integrate with CMOS (Complementary Metal Oxide Semiconductor) process. SiGe HBT has good linearity and efficiency and is much cheaper compared with GaAs, so power amplifiers designed by SiGe process are widely applied in a variety of applications [2, 3]. At the same time, the traditional PAs are generally designed for narrow band, which cannot be applied in various applications. So it is significant to design a multi-mode multi-frequency power amplifier.

There are various structures applying in broadband power amplifier [4], such as balance structure, power synthetic structure, distributed active transformer structure, traditional power amplifier structure. The bandwidth of the balanced amplifier is better than that of the other amplifier. However, at the relatively low frequency, the quarter wavelength transmission lines with 3dB coupler are not easy to integrate, so we abandon balance amplifier and synthesis power structure. The distributed active transformer structure can obtain good performance, but the Q value of inductance in this process is not high, and it is difficult to guarantee consistency of time delay. So we don't choose this structure. Finally, we chose the traditional structure. Gain flatness is more important in designing broadband PA. Considering frequency features of |S21|

which will fall with increasing frequency, so it is necessary to legitimately design the matching network and feedback network [5].

This paper is organized as follows. Section 2 describes the characteristics of the adopted temperature sensor. Details of the circuit implementation is discussed in Section 3. Section IV shows the simulation results of the chip and compares with previous PAs.

2 Process Technology

IBM 0.13-μm SiGe HBT technology has high gain, large current density and perfect substrate thermal conductivity. Moreover, the base-emission open voltage and saturation voltage are low which lead this technology is more suitable for low voltage application. This process not only provides high-performance NPN transistor with cut-off frequency up to 200GHz and breakdown voltage to 1.8V, but also provides high-breakdown NPN transistor with cutoff frequency to 57GHz and breakdown voltage (BV_{ceo}) to 3.5 V. In this paper, the width of emitter is 120nm, length of emitter is 18um. Because of PAs will process large sign and high output power. It needs large output voltage swing, so we choose high-breakdown transistor. However, BV_{ceo} is measured when base is open-circuit. BV_{cer} usually applies to decide breakdown voltage. Here BV_{cer} is 7V, so the supply voltage is 2.5V.

3 The Circuit Design

In this paper, a two-stage 0.8-2.4GHz broadband MMIC (Monolithic Microwave Integrated Circuit) PA is designs for GSM, TD-SCDMA, WLAN systems. This circuit is shown in Fig. 1. Broadband matching network applied in input, which will be impedance conjugate match with the input transistor of the first stage, so that power can be effectively transmitted to drive stage. Negative feedback technology used in drive stage and compensate technology to increase stability, expand bandwidth and obtain good input matching [6]. A low-pass low Q multi-stage LC is adopted in output matching network to achieve optimal load and maximum output power. Considering modulation in different systems, so power stage is biased in class AB to make a good compromise between linearity and efficiency [7].

3.1 The Overall Structure of Circuit

Since there is no through silicon via (TSV) in this process, and all ground wires must connect to ground through a bonding wire. Parasitic inductance of the bonding wire has great impact on the performance of PA. So pseudo-differential structure is adopted, because of the common emitter node can act as AC virtual ground to reduce influence of bonding wires [8]. At the same time, differential structure can increase voltage swing, reduce current limit. Since bandwidth is wide, second harmonic of low-frequency will be in band, using differential structure can filter out second har-

monic to a certain extent. As show in Fig. 1, the PA adopts common emitter using a two-stage pseudo-differential structure. All components are integrated on-chip except the one outside the dotted line.

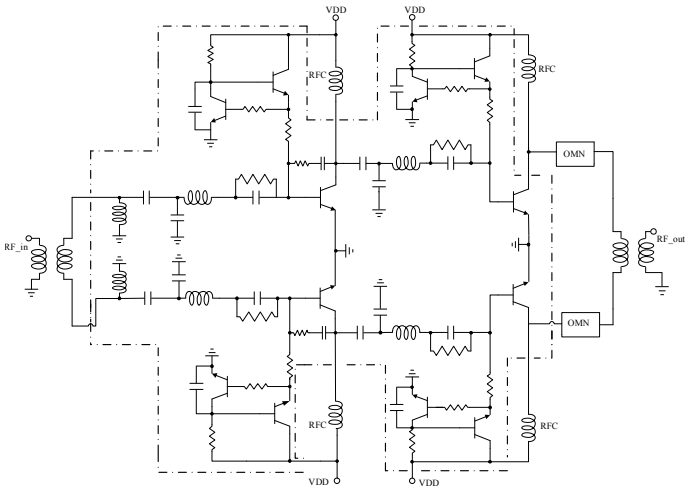

Fig. 1. Structure diagram of the power amplifier

The number of transistors in power stage is determined by output power, breakdown voltage and maximum current which single tube can withstand. In order to obtain enough output power, the number of transistors in output stage will be much more. The parasitic of those transistors can make output impedance become lower, which increases the difficult of designing output matching network. Finally, we chose the number of transistors of power stage and driver stage are 128 and 36 respectively in half-circuit. And current in half-circuit is 72mA and 270mA in driver stage and power stage respectively. Adopt a series resistor in the transistor base to increase stability, as well as in parallel with a capacitor to reduce power loss of resistors.

3.2 Adaptive Bias Control Circuit

Since PA mainly works under large signal condition, clamping feature of diode makes forward voltage and negative current signal of the power transistor is clipped when input power increases. So average current increases and average voltage decreases, which results in the loss of trans-conductance and gain reduction and phase distortion. In order to solve gain compression and phase distortion under large-signal condition, it is necessary to compensate for power transistors to make consistent trans-conductance between small signal and large signal conditions as far as possible. To improve efficiency and linearity and HBT device is a current-controlled device, so we adopt current mirror biasing circuit which can be adaptively change the bias current to raise the efficiency and linearity [9, 10].

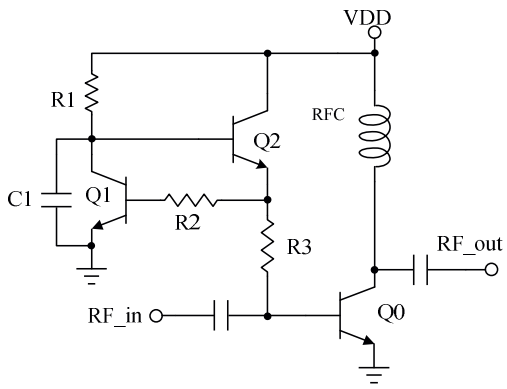

Fig. 2. Adaptive bias control circuit

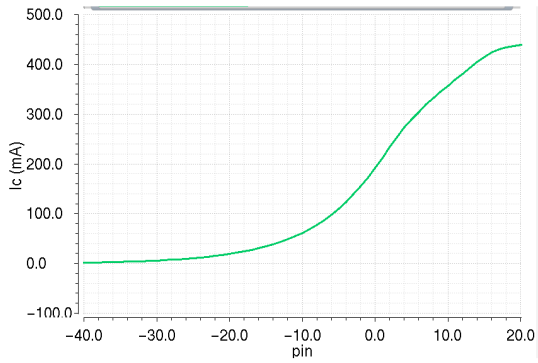

Fig. 3. Bias current changes with the input power

As shown in Fig. 2, transistors Q1 and Q2 act as current mirror which provide base bias current of the power transistor Q0. The bias current is controlled by VDD and R1. There is the relationship as follows:

$$V_{\mathrm{BE0}} + I_{\mathrm{R3}} \cdot R3 = V_{\mathrm{BE1}} + I_{\mathrm{R2}} \cdot R2 \tag{1}$$

The value of R2 and R3 are associated with emitter area ratio of Q0 and Q1. Assumed that S_{Q0}: S_{Q1} = n: 1, then I_{B0}: I_{B1} = n: 1, $V_{\mathrm{BE0}} = V_{\mathrm{BE1}} = V_{\mathrm{BE2}} = V_{\mathrm{BE}}$. We have equation like this:

$$\frac{R2}{R3} = \frac{I_{\mathrm{R3}}}{I_{\mathrm{R2}}} = \frac{I_{\mathrm{B0}}}{I_{\mathrm{B2}}} = n \tag{2}$$

After selected the value of R2 and R3, R1 can be calculated using this formula. I_{C0} is static bias current of the power transistor.

$$R1 \approx \frac{VDD - 2V_{\mathrm{BE}}}{I_{\mathrm{C1}}} = n\frac{VDD - 2V_{\mathrm{BE}}}{I_{\mathrm{C0}}} \tag{3}$$

The linearization mechanism is constituted by base-emitter junction of Q2 and by-pass capacitor C1. C1 makes RF signal short, so that base voltage of Q2 can maintain a constant value. The impedance of linear bias decreases at RF frequencies due to function of C1. Therefore, RF signal leaks to bias part increases which makes V_{BE2} decline and I_{C2} increases to compensate with decline of V_{BE0} and increase of I_{C0} with the increasing input power. It makes bias current dynamic varies from input power, which can increase average efficiency. Fig. 3 gives the bias current changes with the input power.

3.3 Broadband Matching Network

In order to integrate the proposed PA to broadband communication systems, the bandwidth of output- and input- matching network should be wide enough. To achieve broad band, we use a broadband matching technology, including matching compensation technology and low Q multistage LC matching network. The basic idea of matching compensation at inter-stage is be mismatch at low-frequency and match at high-frequency to suppress low-frequency gain and compensate high-frequency gain which can compensate transistors' gain varies from frequency characteristics and achieve gain flatness. Multi-stage broadband matching technique is adopted in input/output matching network to achieve maximum power transform over entire frequency range. The basic principle is to limit the maximum Q value of matching network in accordance with operating frequency and bandwidth. Any impedance transformation doing inside the constant curve of Q can meet the requirement and complete impedance matching. The maximum value of Q can be calculated as follows:

$$Q = f_o / BW \tag{4}$$

Here f_o is center frequency, $f_o^2 = f_{\mathrm{H}} \times f_{\mathrm{L}}$, BW is bandwidth. The load matching is applied in output and the optimum load impedance is obtained from load-pull test. Since the band is wide, we need to simulate the optimum load at multiple frequency points, and the best load at each frequency will be different. But the impedance value changes slightly, so we choose average value as Z_{opt}. Then design a matching network between 50Ω and Z_{opt} inside the constant Q contour [11].Here the optimum load shows in Fig. 4 is about 10.5+j*1.25. Fig. 5 shows impendence transformation and the matching network designed in this method. Fig. 6 shows the impedance value after transformation.

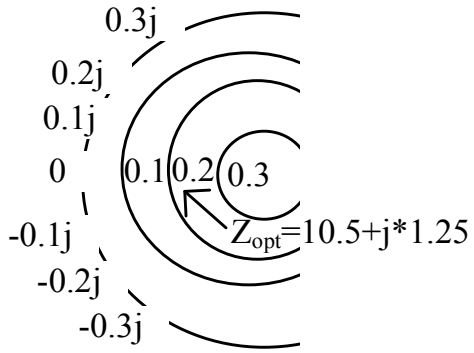

Fig. 4. Optimum load

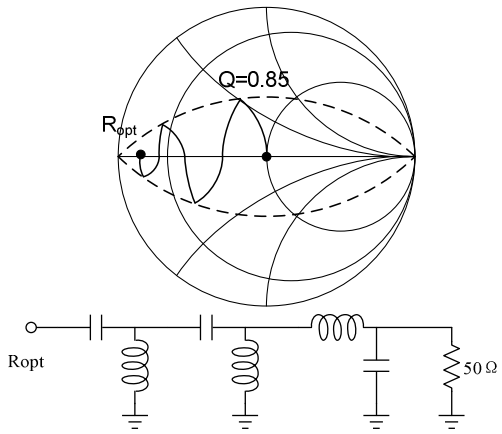

Fig. 5. Multi-stage broadband matching

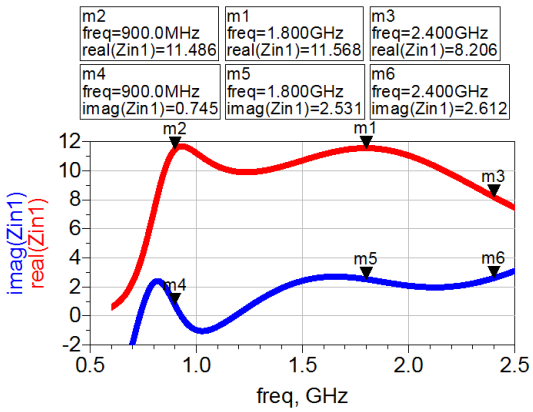

Fig. 6. The impedance after transformation

4 Layout and Simulation Results

PA will flow large current and is achieved by many cell transistors. It is significant to carefully design the arrangement of transistors. To guarantee power with same phase, the arrangement of transistors is tree structure. Fig. 7 is the layout of the PA. The chip size is 1.56 mm× 1.70mm.

The post-simulation shows the S parameter as Fig. 8. The maximum gain is 25.6dB at 781.6MHz, 3dB bandwidth is 690MHz to 2470MHz. Input VSWR (Voltage Standing Wave Ratio) is less than 2.2:1 as shown in Fig. 9. The 1dB compression point (P1dB) at 0.9GHz, 1.9GHz and 2.4GHz are shown as Fig. 10-12. P1dB are 26.38dBm, 26.49dBm, 26dBm respectively. Saturation output power ($P_{out,sat}$) is greater than 29dBm with the power added efficiency (PAE) better than 38%. Its bandwidth, Saturation output power and power added efficiency meets general requirement for GSM/TD-SCDMA/WLAN system, so the proposed PA can be integrated to corresponding electronic systems.

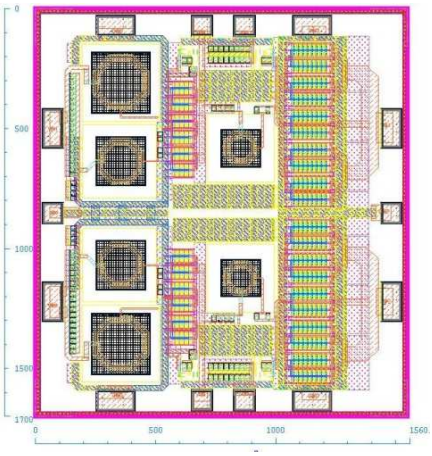

Fig. 7. The layout of power amplifier

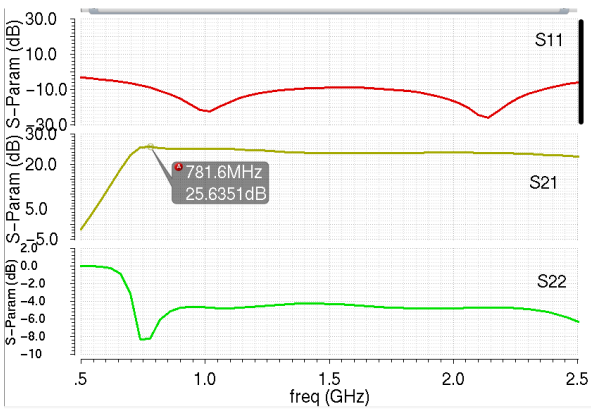

Fig. 8. S parameter

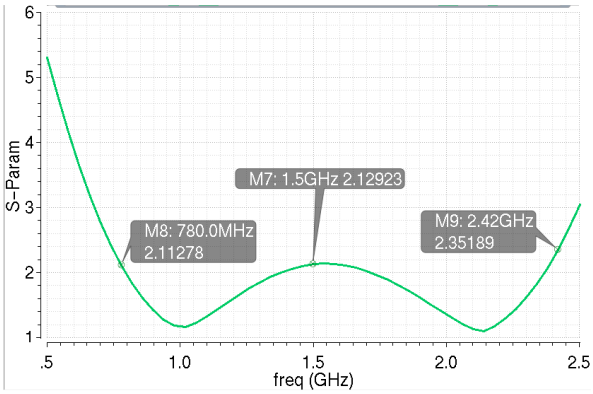

Fig. 9. Input VSWR

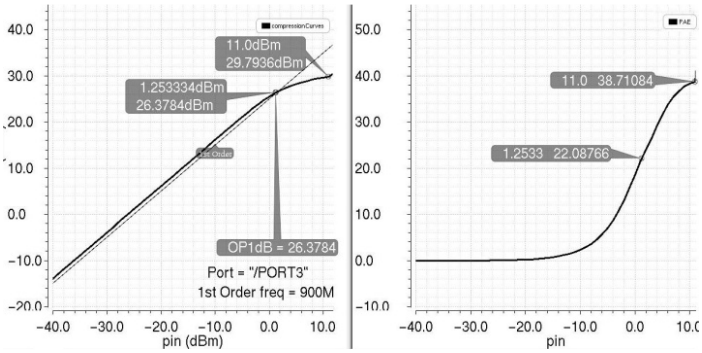

Fig. 10. P1dB/Pout and PAE@0.9GHz

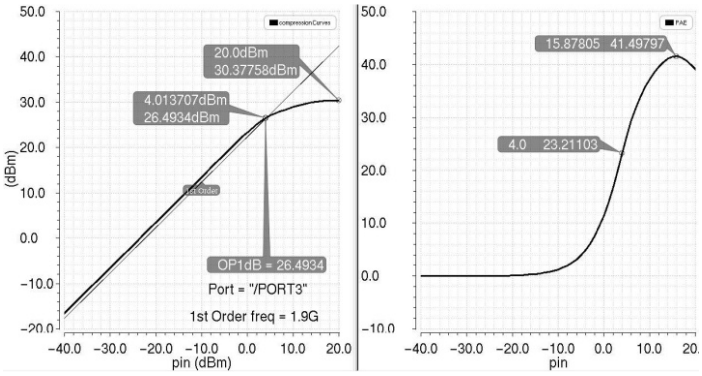

Fig. 11. P1dB/Pout and PAE@1.9GHz

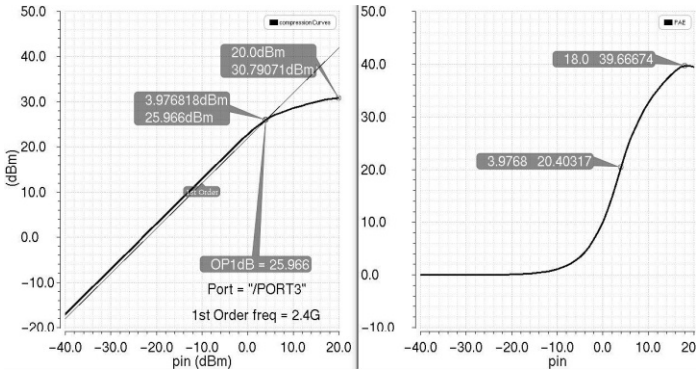

Fig. 12. P1dB/Pout and PAE@2.4GHz

The accomplished performance is compared with the earlier in Table 1.

Table 1. state-of-the-art of PA performance

Ref	Technology	Freq (GHz)	Gain (dB)	P1dB (dBm)	PAE %	Size (mm^2)
[12]	CMOS	3~7	12	7.21	38.5	0.75
[13]	SiGe-HBT	0.7-1.9	20	25	23	3.15
[14]	GaAs-HBT	1.96	30	28	22	NA
This work	SiGe- HBT	0.8-2.4	25.6	26	38	2.65

5 Conclusion

A 0.8-2.4GHz cascade pseudo-differential architecture broadband power amplifier is demonstrated in this paper. Compensated matching, broadband matching, and adaptive bias control technique are employed to optimize linearity, efficiency and bandwidth. The simulation results of S-parameter and power gain show excellent feature. P1dB and PAE at Saturated output power are better than 26dBm and 38%.

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