Co-processor-based Behavior Monitoring

Application to the Detection of Attacks Against the System Management Mode

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Computers rely on firmware

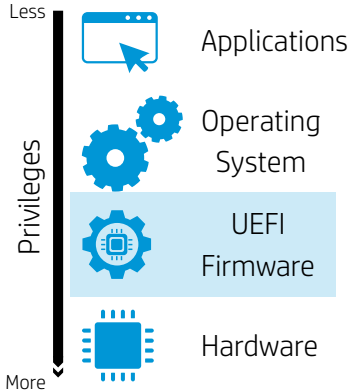
Where can we find firmware?

Mother boards (e.g., BIOS), hard disks, network cards,...

Here, we focus on BIOS/UEFI-compliant firmware

What is it?

- Low-level software
- Tightly linked to hardware
- Early execution
- Highly privileged runtime software
- Stored in a flash



What is the problem?

BIOS is often written in unsafe languages (i.e., C & assembly)

Memory safety errors (e.g., use after free or buffer overflow)

BIOS is not exempt from vulnerabilities [Kallenberg et al. 2013; Bazhaniuk et al. 2015]

Why compromise BIOS?

- Malware can be hard to detect (stealth)
- Malware can be persistent (survives even if the HDD/SSD is changed) and costly to remove

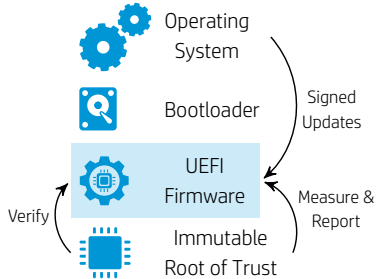
What do we want?

- Boot time integrity
- Runtime integrity

What are the currently used solutions?

Boot time

- Signed updates
- Signature verification before executing
- Measurements and reporting to a Trusted Platform Module (TPM) chip
- Immutable hardware root of trust



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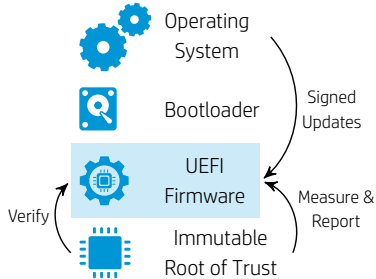


Runtime

Isolation of critical services available while the OS is running

→ our focus is with the System Management Mode (SMM)

Introducing the System Management Mode (SMM)

Highly privileged execution mode for x86 processors

Runtime services

BIOS update, power management, UEFI variables handling, etc.

How to enter the SMM?

- Trigger a System Management Interrupt (SMI)
- SMIs code & data are stored in a protected memory region: System Management RAM (SMRAM)

BIOS code is not exempt from vulnerabilities affecting SMM

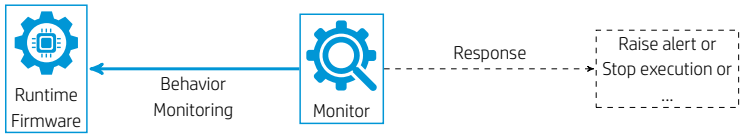
[Bazhaniuk et al. 2015; Bulygin, Bazhaniuk, et al. 2017; Pujos 2016]

Why is it interesting for an attacker?

- Only mode that can write to the flash containing the BIOS
- Arbitrary code execution in SMM gives full control of the platform

Our objective

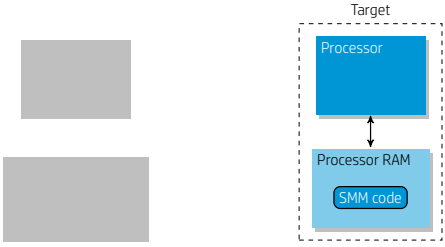
Our goal is to detect attacks that modify the **expected behavior** of the SMM by **monitoring** its behavior **at runtime**.



Such goal raises the following questions:

- How to ensure the integrity of the monitor?
- How to define a correct behavior?
- How to monitor?

Approach overview



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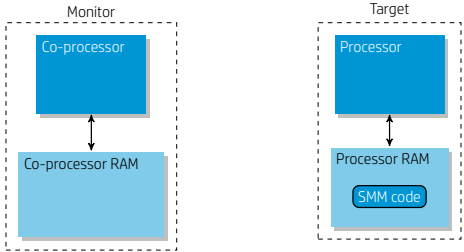

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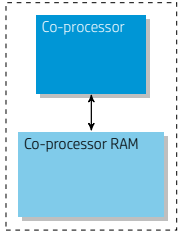
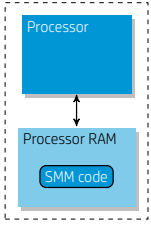


Semantic gap?



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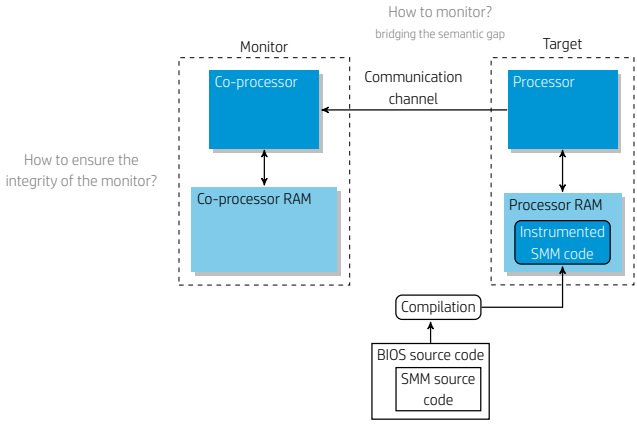
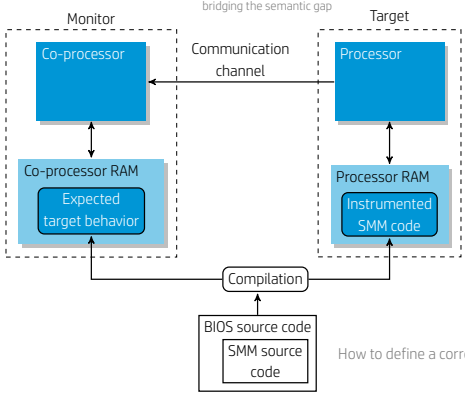


Approach overview

How to monitor?

bridging the semantic gap

How to ensure the integrity of the monitor?



How to define a correct behavior?

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Our use case: SMM code

- Written in unsafe languages (i.e., C & assembly)
  → Such languages are often targeted by attacks hijacking the control flow
- Tightly coupled to hardware
  → Such software modifies hardware configuration registers

Control Flow Graph (CFG)

Define the control flow that the software is expected to follow

→ Control Flow Integrity (CFI)

Invariants on CPU registers

Define rules that registers are expected to satisfy

→ CPU registers integrity

How to define a correct behavior?

Control Flow Integrity (CFI): principle

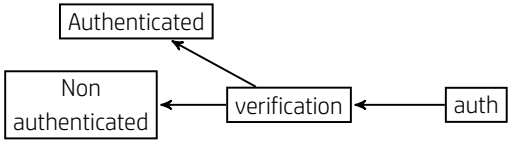
Example

```
void auth(int a, int b) {
    char buffer[512];

    [...vuln...]

    verification(buffer);
}
void verification(char *input) {
    if (strcmp(input, "secret") == 0)
        authenticated();
    else
        non_authenticated();
}
```

Simplified graph



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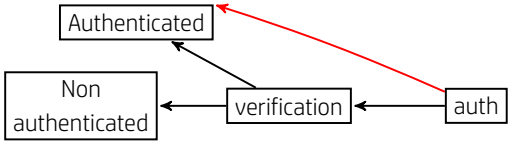

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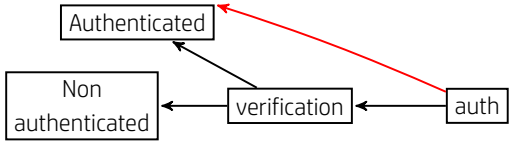

Goal: constrain the execution path to follow a control-flow graph (CFG)

How to define a correct behavior?

Control Flow Integrity (CFI): type-based verification

We focus on indirect branches integrity

Type-based verification

Ensures the integrity of indirect calls

```
typedef struct SomeStruct {
  [...]
  char (*foo)(int);
} SomeStruct;
int bar(SomeStruct *s) {
  char c;
  [...]


  c = s->foo(31);
  [...]
}
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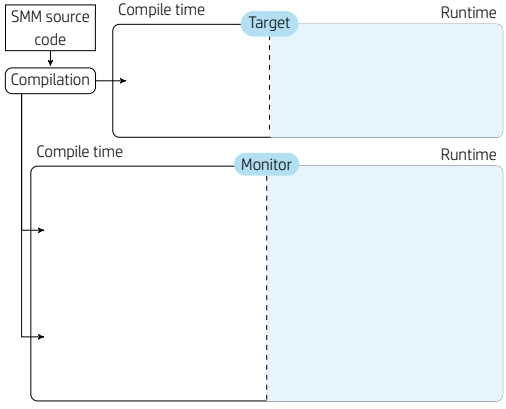

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  c = s->foo(31); /* Call Site ID = 1561 */
  [...]
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```

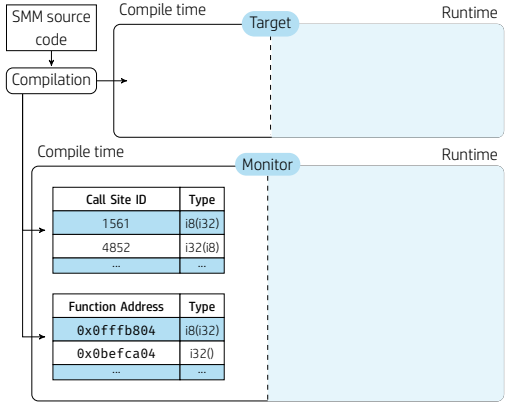

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typedef struct SomeStruct {
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int bar(SomeStruct *s) {
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  [SendMessage(1561, s->foo)]
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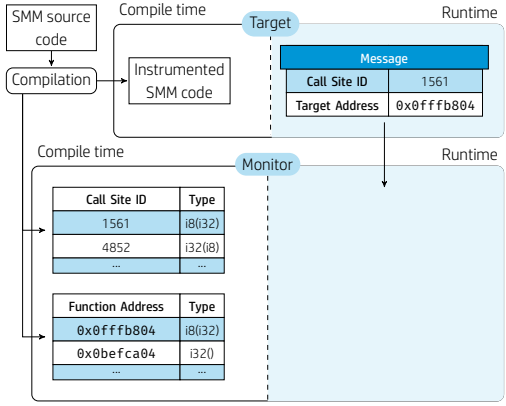

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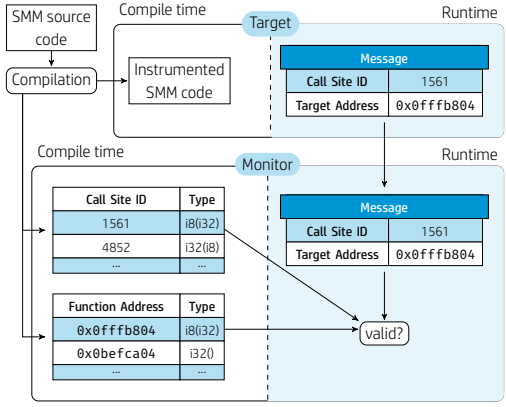
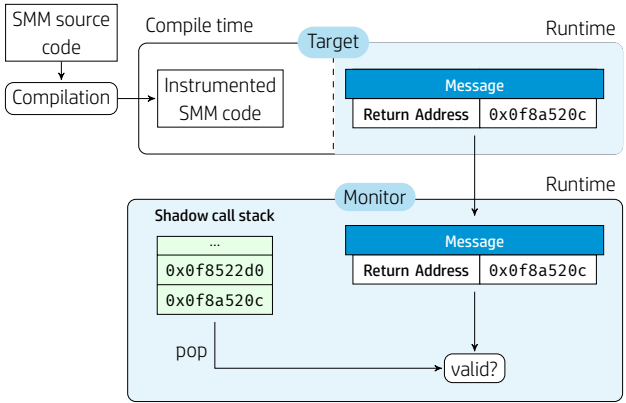


How to define a correct behavior?

Control Flow Integrity (CFI): shadow call stack

Shadow call stack

Ensures integrity of the return address on the stack



How to define a correct behavior?

CPU registers integrity

SMM code is tightly coupled to hardware

- Generic detection methods (e.g., CFI) are not aware of hardware specificities
- Adhoc detection methods are needed

Some interesting registers for an attacker

- **SMBASE**: Defines the SMM entry point
- **CR3**: Physical address of the page directory

→ Their value is stored in memory and is not supposed to change at runtime

How to protect such registers?

- Send the expected values at boot time
- Send messages at runtime containing these values to detect any discrepancy

How to monitor?

Communication channel constraints

Security constraints

- Message integrity
- Chronological order
- Exclusive access

Performance constraints

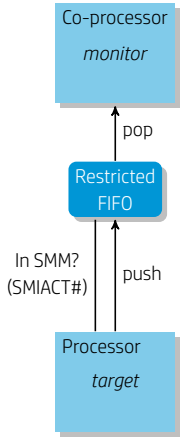
- Acceptable latency of an SMI as defined by Intel BIOS Test Suite: 150 µs
- More than 150 µs per SMI handler leads to degradation of performance or user experience

How to monitor?

Communication channel design

Additional hardware component

- Chronological order
  → FIFO
- Message integrity
  → Restricted FIFO
- Exclusive access
  → Check if CPU is in SMM (SMIACT# signal)
- Performance
  → Use a low latency interconnect



In summary

We isolate the monitor

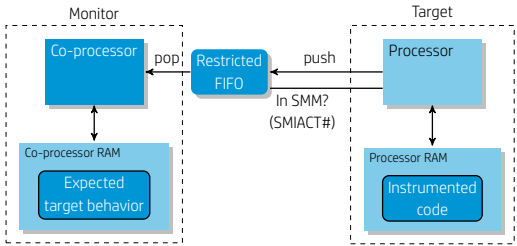
- Dedicated co-processor
- Private memory

We bridge the semantic gap

- Communication channel
- Instrumentation of the target code to send messages

We allow the definition of multiple correct behaviors

- Flexible, multiple possibilities
  - CFI
  - CPU registers integrity



Our experimental setup

Our prototype is implemented in a simulated and emulated environment

SMM code implementations used

- EDK2: foundation of many BIOSes (Apple, HP, Intel,...)
  → UEFI Variables SMI handlers
- coreboot: perform hardware initialization (used on some Chromebooks)
  → Hardware-specific SMI handlers

We want to emulate SMM environment and features

QEMU emulator for security evaluation

We want to simulate accurately the performance impact

gem5 simulator for performance evaluation

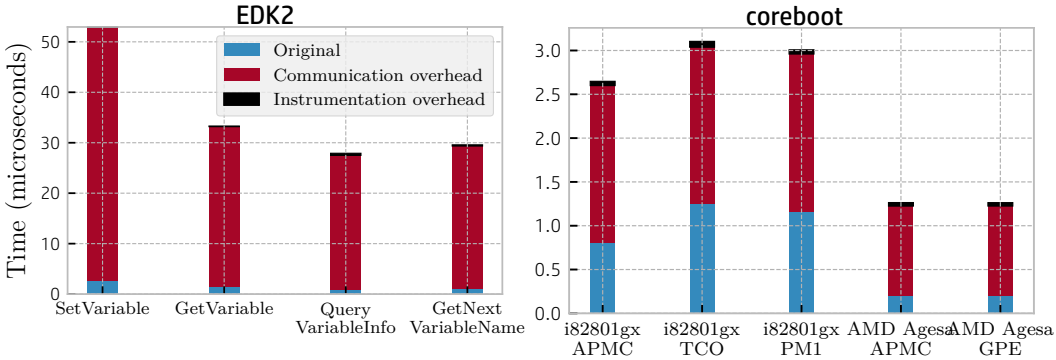
Security evaluation

We simulated attacks & vulnerabilities similar to those found in real-world BIOSes

Vulnerability	Attack Target	Security Advisories	Detected
Buffer overflow	Return address	CVE-2013-3582	Yes
Arbitrary write	Function pointer	CVE-2016-8103	Yes
Arbitrary write	SMBASE	LEN-4710	Yes
Insecure call	Function pointer	LEN-8324	Yes

Performance evaluation

Running time overhead for SMI handlers



- Under the 150 microseconds limit defined by Intel
- Most of the communication overhead is due to the shadow call stack

Related work

Snapshot-based approaches

✗ Transient attacks

Copilot [Petroni et al. 2004]

DeepWatch [Bulygin and Samyde 2008]

Event-driven approaches

✓ Detect transient attacks

Ki-Mon [Lee et al. 2013]

✗ Semantic gap

MGuard [Liu et al. 2013]

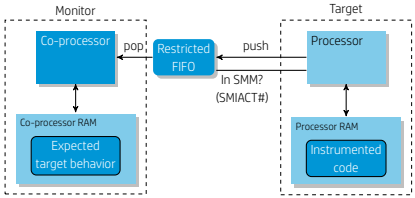
✗ Semantic gap

What did we do? What did we learn?

Our contributions

- Event-based approach to monitor firmware
- Prototype implementing our approach
- Evaluation of our prototype

Our approach



Results

- Detection of state-of-the-art attacks
- Acceptable performance (< 150 µs Intel threshold)

Future work

- Non-control data attacks
- Adaptation to other firmware

Thanks for your attention!

Questions?

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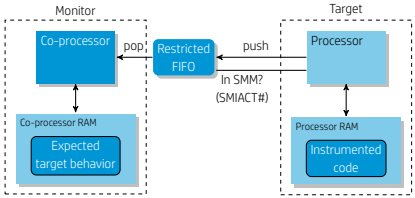

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Bazhaniuk, Oleksandr et al. (2015). “A new class of vulnerabilities in SMI handlers”. CanSecWest, Vancouver, Canada.

Bulygin, Yuriy, Oleksandr Bazhaniuk, et al. (2017). “BARing the System: New vulnerabilities in Coreboot & UEFI based systems”. REcon Brussels.

Bulygin, Yuriy and David Samyde (2008). “Chipset based approach to detect virtualization malware”. Black Hat USA.

Kallenberg, Corey et al. (2013). “Defeating Signed BIOS Enforcement”. EkoParty, Buenos Aires.

Lee, Hojoon et al. (2013). “KI-Mon: A Hardware-assisted Event-triggered Monitoring Platform for Mutable Kernel Object”. In: *Proceedings of the 22th USENIX Security Symposium*, pp. 511–526.

Liu, Ziyi et al. (2013). “CPU Transparent Protection of OS Kernel and Hypervisor Integrity with Programmable DRAM”. In: *Proceedings of the 40th Annual International Symposium on Computer Architecture*. ISCA ’13. Tel-Aviv, Israel: ACM, pp. 392–403.

References ii

Petroni Jr., Nick L. et al. (Aug. 2004). “Copilot - a Coprocessor-based Kernel Runtime Integrity Monitor”. In: *Proceedings of the 13th USENIX Security Symposium*, pp. 179–194.

Pujos, Bruno (May 2016). *SMM unchecked pointer vulnerability*. URL: `http://esec-lab.sogeti.com/posts/2016/05/30/smm-unchecked-pointer-vulnerability.html`.

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