FPGA-Based Image Acquisition System Designed for Wireless

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Abstract. Introduced micro-wireless transmission system image acquisition the overall structure, each part of the overall design ideas and works theory. Designed SBBC camera interface and data cache control module, analysis of the TCP / IP communication protocol standard structure and characteristics, and on this basis, the design of a non-standard short-range wireless communication protocol. System which controlled by the input and output module is based on FPGA, the system collected data alternately to the outer SDRAM, this realized the image data collection; Ethernet interface controller also designed in FPGA to achieve the image data transmit through wireless. The results show that: under normal conditions, the wireless communication module can be complete, accurate, stable wireless data transceiver functions.

Keywords: Digital image sensor, SBBC interface, FPGA, wireless transmission

1 Introduction

Along with the fast developing of computer, network transmission technology and communication technology, wireless remote video transmission has become a trend, this technology has gradually be applied in remote monitoring, aerial photo taken, conference call, etc. Video monitoring now generally use the following solutions[1,2]: use high imaging quality of image sensor camera, through the S-VIDEO terminals transmission data in real-time, this plan need a camera and acquisition device connectivity, and the monitoring center also need large storage space to store image and video clips, this scheme is high real-time, but big energy consumption and high cost, so it is suitable for public security and monitoring. While the wireless image acquisition system based on FPGA with its low power consumption and reconfigurable characteristics being perfect choice. In the condition of the wireless application protocol has been developed, the center of gravity of the research is to image sensor used by the hardware platform and streams of data processing, at present the main schemes are: ①DSP+FPGA, use FPGA to complete data storage and preprocessing work, using DSP chip high-speed processing power to compress and process the image, this plan suitable for need data parallel processing and more numerical JPEG data flow.

② FPGA+ video codec chips, use the parallel processing ability of FPGA transmit and processing of images and video data simultaneously, because FPGA is reconfigurable in hardware, this plan suitable for the experimental stage. ③CPU + FPGA, use as the central control and interface CPU control role, use the FPGA to complete image processing tasks. MicroBlaze32 a soft processor core of Xilinx company is the industry's fastest soft handling solutions, running in the 150 MHz clock, it can provide 125 D-MIPS , very suitable for design in view of the network, data communication, embedded of complex system, so that the plan three with the CPU inside FPGA to design the wireless image acquisition system[3] .

2 Design Thought

Wireless image acquisition system Based on FPGA is mainly collection site image signal, and the collected image data will be transmit to upper computer in real-time through Ethernet, at the same time can receive instruction data from upper computer, the whole system diagram shown as in figure 1. System mainly consists of four modules: image sensor module, image acquisition and control module, image storage and processing module, network data transmission module. In the process of operation, the FPGA will storage the CMOS sensor data to the expansion SRAM [4], every full of a frame processor read data from SRAM and FPGA kernel processor by MicroBlaze will sent the data to the upper machine through the Ethernet chips.

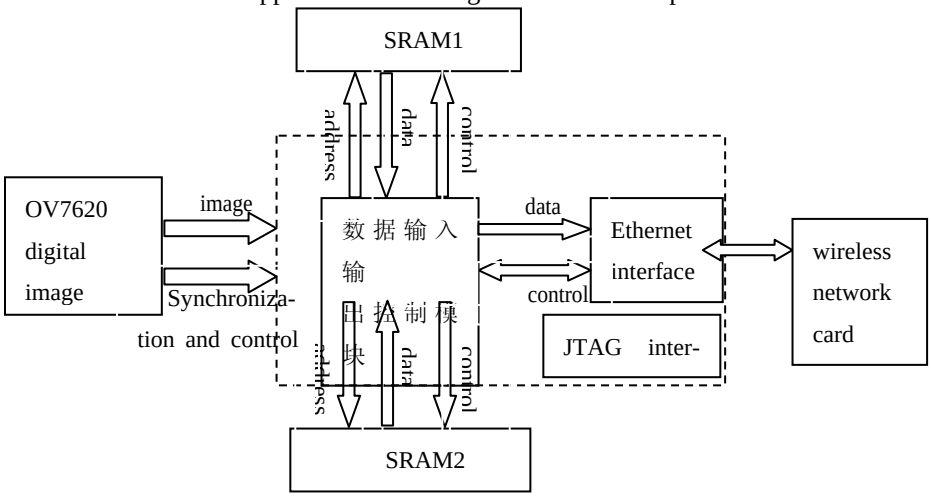

Fig.1. System diagram

3 Control and Processing Module Design Use FPGA

The system use FPGA made by xilinx company the chip models is XC3S1500, the input and output of the camera data control module was designed, SRAM reading and

writing control module and based on the soft nuclear Ethernet interface were designed, below will make a detailed description for each part .

3.1 Image Acquisition and Interface Design

In the system the Omni vision company OV7620 type CMOS image sensor [5] was adopted as image sensor, it support continuous and interlaces the two scanning mode, with 10 double channel A/D converter, output eight image data; the highest pixels is 664 x 492, frame rate is 30 FPS; data formats including YUV, YUV, RGB three types, can satisfy the requirement of general image acquisition system, can programming configuration internal registers through SCCB bus. Meet the power supply and working in the crystals can output digital streaming of video at the same time also provide pixel clock PCLK, line reference signal----HREF、vertical synchronized signal----VSYNC, can use the clock signal above to determine each frame output image starting bit and end bit, meet the requirements of the external circuit read image

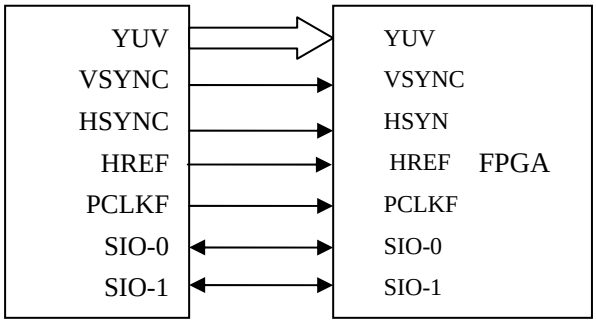

Fig.2. OV7620 and FPGA interface

SCCB bus timing is similar to the I2C bus timing，SIO-0 equivalent to SDA, SIO-1 equivalent to SCL. The system set OV7620 work in slave mode, its interface with FPGA connection as shown in figure 2. The camera work mode can be set through write corresponding data to different registers, in the process of writing register first send OV7620 ID address, and then write the purpose of sending data register addresses, and finally to write data sent by setting the corresponding register, can make the image sensor work in a different model.

3.2 Data Storage Module

The data storage use company of ISSI IS61LV25616AL type chip, it is the static RAM, system of each frame resolution for the 640*480 grayscale image need 2457600 bit, less than its storage capacity 4194304 bit, can meet the storage requirements. To meet the real time requirement, data storage using high-speed SRAM switch mode, called "table tennis" mode. The specific process as follows: the data of image data flow distribution to two SRAM through FPGA output and output control module. In the first period, the input data cache to SRAM1, in the second period through the input data flow choice unit storage the date to SRAM2, at the same time, to sent the first cycle of data cached in SRAM1 to subsequent module through the

output data choice unit, the third cycle the input data stream select units will storage data to SRAM1, at the same time, to sent data in SRAM2 last cycle through the output data choice unit to the follow-up module. So again, to realize the seamless data buffer, ensure the integrity of the image data.

3.3 Transmission

In the network transmission module, the chip BCM5221 made by BroadCom company was used in the physical, use the soft MicroBlaze32 nuclear as controller in the EDK development environment to generate the basic framework and related documents by generation wizard , the architecture of the soft nuclear as shown in figure 3.

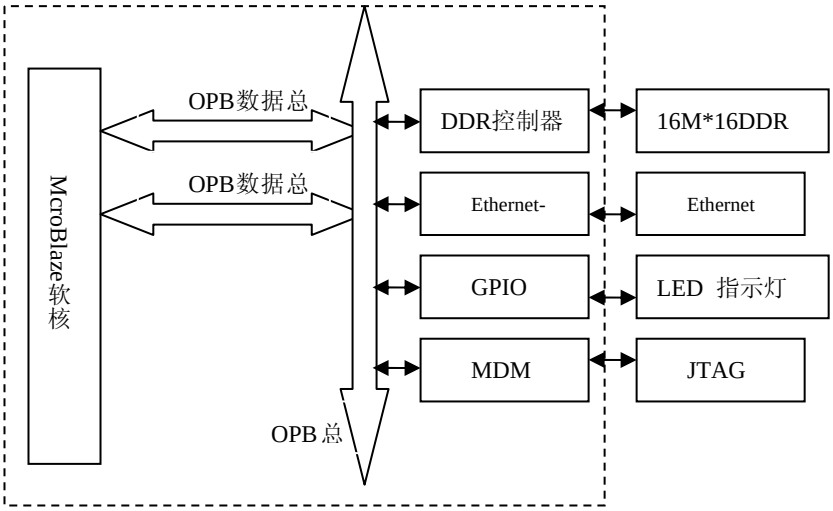

Fig.3. Soft nuclear basic framework

In the system, the DDR (double-data-rate) use the OPB DDR controller connect with OPB high-speed bus, and the Ethernet physical chip----BCM5221 connect with OPB bus through the Ethernet MAC, they are all OPB bus high-speed equipment; GPIO (General Purpose I/O) is the low speed terminal controller also can be connected in OPB bus, links such as LED and some terminals not high demand for the speed. MicroBlaze Debug modules MDM (MicroBlaze Debug Module) is responsible for download and test software.

The system adopts the TCP/IP protocol, divided into fluctuation two parts to realize [6, 7]. The physical layer realized by the hardware BCM5221 chip, the MAC layer realized by xilinx company Ethernet MAC IP nuclear ; The top of the transport layer by the software code realization, the LwIP agreement module, this module is one set for the embedded system is an open source TCP/IP protocol, the main purpose of LwIP is to keep the TCP/IP protocol in the main functions of the case to reduce the use of RAM, at present LwIP is widely used in all kinds of top-grade of embedded system. LwIP also support server mode and client mode, in the upper part of the agreement we adopt LwIP agreement module.

4 Conclusion

After research of the traditional image acquisition module deeply, based on disadvantages of transmission to the traditional image acquisition module, designed the image acquisition and wireless transmission module for portable embedded system. The system realized the original data collection and image storage, ensure the image data of wireless transmission continuously and completely, with small size, low power consumption, speed advantages.

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