Accurate Modeling of Fault Impact in Arithmetic Circuits
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1. Objective: Design of Robust Arithmetic Circuits

Study links between fault detection/tolerant solutions and

- types of operations ±, ×, ÷, √, sin, cos, log, ...
- computation algorithms and representations of numbers
- optimizations at architecture and circuit levels
- mathematical error due to faults and rounding modes

Applications: signal/image processing, embedded computing, protections for cryptographic devices, ...

2. Intensive Logical Fault Simulations: Emulation on FPGA

Possible locations for logical fault injection:

- manual on selected internal nets (for debug)
- random on internal nets
- random over circuit area (based on cells area)

3. Hardware Platform

4. Emulation Engine(s) in FPGA

5. Tools Flow

6. Example: Multiplier with Residue Code Detection

16 × 16-bit integer multiplier, moduli \( m \in \{3, 7, 15\} \), with

\[
(a \times b) \mod m = ((a \mod m) \times (b \mod m)) \mod m
\]

Comparaison to a CABA simulation in software (Vivado 2014.4):

- 6880 speedup for 1 emulation engine

Error distribution for exhaustive tests (\( 2^{32} \) inputs) and various single faults (1 color = 1 fault):

7. Future Works

References:

P. Guilloux & A. Tisserand, Compas 2016, French Conf. on Parallelism, Architecture and System