# IFIP Advances in Information and Communication Technology

461

#### Editor-in-Chief

Kai Rannenberg, Goethe University Frankfurt, Germany

#### **Editorial Board**

Foundation of Computer Science

Jacques Sakarovitch, Télécom ParisTech, France

Software: Theory and Practice

Michael Goedicke, University of Duisburg-Essen, Germany

Education

Arthur Tatnall, Victoria University, Melbourne, Australia

**Information Technology Applications** 

Erich J. Neuhold, University of Vienna, Austria

Communication Systems

Aiko Pras, University of Twente, Enschede, The Netherlands

System Modeling and Optimization

Fredi Tröltzsch, TU Berlin, Germany

**Information Systems** 

Jan Pries-Heje, Roskilde University, Denmark

ICT and Society

Diane Whitehouse, The Castlegate Consultancy, Malton, UK

Computer Systems Technology

Ricardo Reis, Federal University of Rio Grande do Sul, Porto Alegre, Brazil

Security and Privacy Protection in Information Processing Systems

Yuko Murayama, Iwate Prefectural University, Japan

Artificial Intelligence

Tharam Dillon, Curtin University, Bentley, Australia

**Human-Computer Interaction** 

Jan Gulliksen, KTH Royal Institute of Technology, Stockholm, Sweden

**Entertainment Computing** 

Matthias Rauterberg, Eindhoven University of Technology, The Netherlands

#### IFIP - The International Federation for Information Processing

IFIP was founded in 1960 under the auspices of UNESCO, following the First World Computer Congress held in Paris the previous year. An umbrella organization for societies working in information processing, IFIP's aim is two-fold: to support information processing within its member countries and to encourage technology transfer to developing nations. As its mission statement clearly states,

IFIP's mission is to be the leading, truly international, apolitical organization which encourages and assists in the development, exploitation and application of information technology for the benefit of all people.

IFIP is a non-profitmaking organization, run almost solely by 2500 volunteers. It operates through a number of technical committees, which organize events and publications. IFIP's events range from an international congress to local seminars, but the most important are:

- The IFIP World Computer Congress, held every second year;
- Open conferences;
- Working conferences.

The flagship event is the IFIP World Computer Congress, at which both invited and contributed papers are presented. Contributed papers are rigorously refereed and the rejection rate is high.

As with the Congress, participation in the open conferences is open to all and papers may be invited or submitted. Again, submitted papers are stringently refereed.

The working conferences are structured differently. They are usually run by a working group and attendance is small and by invitation only. Their purpose is to create an atmosphere conducive to innovation and development. Refereeing is also rigorous and papers are subjected to extensive group discussion.

Publications arising from IFIP events vary. The papers presented at the IFIP World Computer Congress and at open conferences are published as conference proceedings, while the results of the working conferences are often published as collections of selected and edited papers.

Any national society whose primary activity is about information processing may apply to become a full member of IFIP, although full membership is restricted to one society per country. Full members are entitled to vote at the annual General Assembly, National societies preferring a less committed involvement may apply for associate or corresponding membership. Associate members enjoy the same benefits as full members, but without voting rights. Corresponding members are not represented in IFIP bodies. Affiliated membership is open to non-national societies, and individual and honorary membership schemes are also offered.

More information about this series at http://www.springer.com/series/6102

Alex Orailoglu · H. Fatih Ugurdag Luís Miguel Silveira · Martin Margala Ricardo Reis (Eds.)

## VLSI-SoC: At the Crossroads of Emerging Trends

21st IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2013 Istanbul, Turkey, October 6–9, 2013 Revised and Extended Selected Papers



Editors Alex Orailoglu University of California at San Diego La Jolla, CA USA

H. Fatih Ugurdag Ozyegin University Istanbul Turkey

Luís Miguel Silveira University of Lisbon Lisbon Portugal Martin Margala University of Massachusetts Lowell, MA USA

Ricardo Reis Universidade Federal do Rio Grande do Sul Porto Alegre Brazil

ISSN 1868-4238 ISSN 1868-422X (electronic)
IFIP Advances in Information and Communication Technology
ISBN 978-3-319-23798-5 ISBN 978-3-319-23799-2 (eBook)
DOI 10.1007/978-3-319-23799-2

Library of Congress Control Number: 2015952217

Springer Cham Heidelberg New York Dordrecht London © IFIP International Federation for Information Processing 2015

This work is subject to copyright. All rights are reserved by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed.

The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

The publisher, the authors and the editors are safe to assume that the advice and information in this book are believed to be true and accurate at the date of publication. Neither the publisher nor the authors or the editors give a warranty, express or implied, with respect to the material contained herein or for any errors or omissions that may have been made.

Printed on acid-free paper

Springer International Publishing AG Switzerland is part of Springer Science+Business Media (www.springer.com)

#### **Preface**

This book contains extended and revised versions of the highest-quality papers that were presented during the 21<sup>st</sup> edition of the IFIP/IEEE WG10.5 International Conference on Very Large Scale Integration (VLSI-SoC), a global system-on-chip design and CAD conference. This edition of the conference was held at Novotel Hotel in Istanbul, Turkey (October 6–9, 2013). Previous conferences have taken place in Edinburgh, Trondheim, Vancouver, Munich, Grenoble, Tokyo, Gramado, Lisbon, Montpellier, Darmstadt, Perth, Nice, Atlanta, Rhodes, Florianopolis, Madrid, Hong Kong, and Santa Cruz.

The purpose of this conference, which was sponsored by IFIP TC 10 Working Group 10.5, the IEEE Council on Electronic Design Automation (CEDA), and the IEEE Circuits and Systems Society, and In-Cooperation of ACM SIGDA, was to provide a forum for the exchange of ideas and presentation of industrial and academic research results in the field of microelectronics design. The current trend toward increasing chip integration and technology process advancements have brought new challenges both at the physical and system design levels as well as in the test of these systems. The VLSI-SoC conference aims to address these exciting new issues.

The quality of submissions (244 papers from 48 countries, excluding PhD Forum and embedded tutorials) made the selection process a very difficult one. Finally, 49 were accepted as full papers (6 pages in the proceedings), 19 as short papers (4 pages), and 14 as extended abstracts (2 pages). Out of the 48 full papers presented at the conference, 11 papers were chosen by a selection committee to have an extended and revised version included in this book. An extended version of a previously unpublished high-quality paper from VLSI-SoC 2012 is also included. The selection process of these papers considered the evaluation scores during the review process as well as the review forms provided by members of the technical program committee and session chairs as a result of the presentations. The Technical Program Committee comprised 97 members.

The chapters of this book have authors from Algeria, France, Germany, Greece, Italy, Japan, Sweden, Switzerland, United Arab Emirates, and USA.

VLSI-SoC 2013 was the culmination of the work of many dedicated volunteers: paper authors, reviewers, session chairs, invited speakers, and various committee chairs and members, especially the local organizers. We thank them all for their contributions. We also thank Aydin Dirican, Cagatay Ozmen, and Nurettin Tan (University of Massachusets Lowell) for their critical help in the revision of the book chapters.

This book is intended for the VLSI community, mainly those who did not have the chance to attend the conference. We hope you will enjoy reading this book and that you will find it useful in your professional life and for the development of the VLSI community as a whole.

July 2015

Alex Orailoglu H. Fatih Ugurdag Luís Miguel Silveira Martin Margala Ricardo Reis

#### **Organization**

The IFIP/IEEE International Conference on Very Large Scale Integration-System-on-Chip (VLSI-SoC) 2013 took place during October 6–9, 2013, in Novotel, Istanbul, Turkey. VLSI-SoC 2013 was the 21<sup>st</sup> in a series of international conferences, sponsored by IFIP TC 10 Working Group 10.5 (VLSI), IEEE CEDA, and ACM SIGDA.

#### **General Chairs**

H. Fatih Ugurdag Ozyegin University, Turkey

Luís Miguel Silveira INESC ID/IST - University of Lisbon, Portugal

**Program Chairs** 

Alex Orailoglu UC San Diego, USA Luigi Carro UFRGS, Brazil

**Special Sessions Chair** 

Yankin Tanurhan Synopsys, USA

**Local Arrangement Chair** 

Nizamettin Aydin Yildiz Technical University, Turkey

**Publication Chairs** 

Martin Margala University of Massachusetts, Lowell, USA

Ricardo Reis UFRGS, Brazil

**Publicity Chair** 

Ricardo Reis UFRGS, Brazil

**Registration Chair** 

Sezer Goren Yeditepe University, Turkey

**Finance Chair** 

Sule Ozev Arizona State University, USA

#### PhD Forum Chair

Mahmut Kandemir Penn State University, USA

#### **VLSI-SoC Steering Committee**

Manfred Glesner TU Darmstadt, Germany Matthew Guthaus UC Santa Cruz, USA

Salvador Mir TIMA, France Ricardo Reis UFRGS, Brazil

Michel Robert University of Montpellier, France

Luís Miguel Silveira INESC ID/IST - University of Lisbon, Portugal

Chi-Ying Tsui HKUST, Hong Kong, SAR China

#### **Program Committee**

#### Track 1 - Analog and Mixed-signal IC Design

Günhan Dündar Boğaziçi University, Turkey (chair)

Jose M. de La Rosa CNM, Spain (chair)
Abhijit Chatterjee Gatech, USA
Dongsheng Ma UT Dallas, USA
Haralambos Stratigopoulos IMAG, France

Jerzy Dobrowski Linköping University, Sweden Piero Malcovati University of Pavia, Italy Pui-In Mac University of Macau, China

Sergio Bampi UFRGS, Brazil

#### Track 2 - Circuits for Applications

#### (DSP, Image processing, Communications, Medical)

Tobias Noll RWTH-Aachen, Germany (chair)

Urs Frey Riken, Japan (chair)

Andreas Demosthenous

Andrew Mason

George Jie Yuan

Goksenin Yaralıoğlu

University College London, UK

Michigan State University, USA

UST, Hong Kong – China

Özyeğin University, Turkey

Jun Ohta Nara Institute of Science and Technology, Japan

Vijaykrishnan Narayanan Pennsylvania State University, USA

#### Track 3 - Application Systems

#### (DSP, Image Processing, Communications, Medical)

Luc ClaesenUniversity of Hasselt, Belgium (chair)İlker HamzaoğluSabancı University, Turkey (chair)Berna OrsIstanbul Technical University, TurkeyChun-Jen TsaiNational Chiao Tung University, Taiwan

IX

Hassan Ghasemzadeh UCLA, USA Pai Chou UC Irvine, USA

Yun Pan Zhejiang University, China

#### Track 4 - VLSI Test, Diagnosis and Silicon Debug

Matteo Sonza Reorda Politecnico di Torino, Italy (chair) Zain Navabi University of Tehran, Iran (chair)

Erik Larsson Lund University, Sweden

Hans-Joachim Wunderlich University of Stuttgart, Germany

Fernanda Kastensmidt UFRGS, Brazil

Michiko Inoue Nara Institute of Science and Technology, Japan

Xiaoqing Wen Kyutech, Japan

#### Track 5 - Variability, Security, Reliability

Srinivas Devadas MIT, USA (chair) Özgür Sinanoğlu NYU, UAE (chair) Bruno Rouzeyre LIRMM, France

Maria Michael University of Cyprus, Cyprus

Mehdi Tahoori Karlsruhe Institute of Technology, Germany

Paolo Prinetto Politecnico di Torino, Italy

Ramesh Karri NYU, USA Swaroop Ghosh USF, USA

#### Track 6 - Devices, Circuits and Systems for Emerging Technologies

Wenjing Rao University of Illinois Chicago, USA (chair) Swarup Bhunia Case Western Reserve University, USA (chair)

Andras Moritz UMass Amherst, USA
Dmitry Strukov UC Santa Barbara, USA
Fabien Clermidy CEA LETI, France

Ian O'Connor Ecole Centrale de Lyon, France

Sorin Cotofana TU Delft, Netherlands

Valeriu Beiu United Arab Emirates University, UAE

#### Track 7 - Prototyping, Verification, and Validation

Masahiro Fujita University of Tokyo, Japan (chair)
Franco Fummi University of Verona, Italy (chair)
Alper Şen Boğaziçi University, Turkey
Andreas Veneris University of Toronto, Canada
Graziano Pravadelli University of Verona, Italy

Ian Harris UC Irvine, USA Laurence Pierre IMAG, France

#### Organization

X

#### Track 8 - Embedded Systems, HW-SW Codesign, Logic and High-Level Synthesis

Andreas Gerstlauer UT Austin, USA (chair)

Jason Xue City University of Hong Kong, Hong Kong – China

(chair)

Fadi Kurdahi UC Irvine, USA Frederic Rousseau IMAG, France

Jarmo Takala Tampere University of Technology, Finland Joerg Henkel Karlsruhe Institute of Technology, Germany

Petru Eles Linköping University, Sweden

Sri Parameswaran UNSW, Australia

#### Track 9 - Reconfigurable, Adaptive, FPGA

Koen Bertels TU Delft, Netherlands (chair)

Juergen Becker Karlsruhe Institute of Technology, Germany (chair)

Apostolos Dollas Technical University of Crete, Greece

Joao Cardoso University of Porto, Portugal

Michael Huebner Karlsruhe Institute of Technology, Germany

Pascal Benoit LIRMM, France
Philip Brisk UC Riverside, USA

Rainer Hartenstein Kaiserslautern University of Technology, Germany

#### Track 10 - SOC Design and Interconnect

Cristina Silvano Poltecnico di Milano, Italy (chair)

Jose Ayala Complutense University of Madrid, Spain (chair)
Jiang Xu Hong Kong University of Science & Technology,

China

Gilles Sassatelli LIRMM, France

Leandro Soares Indrusiak The University of York, UK Luca Carloni Columbia University, USA

Smail Niar LAMIH/University of Valenciennes, France

Xiaoxia Wu Qualcomm, USA

#### Track 11 - Processor Architecture, Embedded Processors, Multicores

Onur Mutlu CMU, USA (chair)

Stephan Wong
Ayse K. Coskun
Chengmo Yang
Gang Qu
Mirko Loghi
University of University

Soontae Kim KAIST, Korea

Tulika Mitra National University of Singapore, Singapore

#### Track 12 - Transistor Level Digital VLSI Circuits and Memory

Massimo Alioto University of Siena, Italy (chair)

Saibal Mukhopadhay
Alexander Fish
Bar-Ilan University, Israel
Ali Afzali-Kusha
University of Tehran, Iran
Alper Demir
Koç University, Turkey
Armin Tajalli
FPFL, Switzerland
Joachim Rodrigues
Lund University, Sweden

Yajun Ha National University of Singapore, Singapore

### Contents

Debugging Methods Through Identification of Appropriate Functions for Internal Gates	1
Kosuke Oshima, Takeshi Matsumoto, and Masahiro Fujita	
Gate Sizing Under Uncertainty	23
New Scan-Based Attack Using Only the Test Mode and an Input Corruption Countermeasure	48
Quantitative Optimization and Early Cost Estimation of Low-Power Hierarchical-Architecture SRAMs Based on Accurate Cost Models	69
Low-Power Low-Voltage $\Delta\Sigma$ Modulator Using Switched-Capacitor Passive Filters	94
Fine Grain Precision Scaling for Datapath Approximations in Digital Signal Processing Systems	119
A Complete Real-Time Feature Extraction and Matching System Based on Semantic Kernels Binarized	144
An FPGA-Based Real-Time System for 3D Stereo Matching, Combining Absolute Differences and Census with Aggregation and Belief Propagation Kyprianos Papadimitriou, Sotiris Thomas, and Apostolos Dollas	168
Minimizing Test Frequencies for Linear Analog Circuits: New Models and Efficient Solution Methods	188
Partition-Based Faults Diagnosis of a VLIW Processor	208

#### XIV Contents

Enhanced Compressed Look-up-Table Based Real-Time	
Rectification Hardware	227
Abdulkadir Akin, Luis Manuel Gaemperle, Halima Najibi,	
Alexandre Schmid, and Yusuf Leblebici	
A Flexible ASIC for Time-Domain Decision-Directed Channel Estimation	
in MIMO-OFDM Systems	249
Andreas Minwegen, Dominik Auras, and Gerd Ascheid	
Author Index	267
INMINI IIIMVA	201