Efficient Hybrid Continuous-Time/Discrete-Time $\sum \Delta$ Modulators for Broadband Wireless Telecom Systems

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Abstract. This work analyzes the use of hybrid continuous-time/discrete-time ΣΔ modulators for the implementation of analog-to-digital converters intended for wideband mobile applications. Two alternative multirate cascade ΣΔ architectures are discussed and analyzed, taking into account the impact of main circuit-level error mechanisms, namely: mismatch, finite dc gain and gain-bandwidth product. Both multirate ΣΔ modulators are compared with conventional single-rate continuous-time cascade ΣΔ modulators in terms of their sensitivity to non-ideal effects, considering different target specifications. Theoretical predictions match simulation results, showing that the lowest performance degradation is obtained by a new kind of multi-rate hybrid ΣΔ modulators, in which the continuous-time circuits operate at a higher rate than the discrete-time parts of the modulator.

Keywords: Analog-to-digital conversion, multirate sigma-delta modulation, hybrid continuous-time/discrete-time circuits, wireless telecom applications.

1 Introduction

The need of increasingly higher data rates in mobile telecom systems demands for power-efficient wideband Analog-to-Digital Converters (ADCs). Among other ADC techniques, Sigma-Delta Modulators (ΣΔMs) implemented with Continuous-Time (CT) circuits have demonstrated to be a suited solution in these applications. Compared with Discrete-Time (DT) ΣΔMs – usually implemented with SC circuits – CT-ΣΔMs achieve faster rates with less power consumption. However, they present a higher sensitivity than DT-ΣΔMs to some critical circuit non-idealities, mainly: clock jitter error and circuit element tolerances [1]. This has motivated the exploration of other alternatives like the so-called Hybrid CT/DT ΣΔMs (H-ΣΔMs) [2], in which the front-end part of the ΣΔM is implemented with CT circuits, thus benefiting from their faster operation, embedded anti-aliasing filtering and reduced power dissipation, while keeping a higher robustness against circuit errors than in pure CT-ΣΔMs [3].

The main drawback of H-ΣΔMs is that their sampling rate is indeed limited by the DT part of the system. This problem can be alleviated if the signal is *downsampled* across the modulator, so that the CT front-end operates at a higher clock rate than the

DT back-end, thus relaxing its dynamic requirements, and achieving the required specifications by properly combining the different OverSampling Ratios (OSRs) in a *multirate* operation [4]. However, a detailed analysis of their circuit non-ideal effects is required in order to systematize the circuit design and to optimize performance in terms of required signal bandwidth, effective resolution and power consumption.

This paper contributes to this topic and analyses the effect of main circuit errors on the performance of two different kinds of multirate cascade H-ΣΔMs (MR H-ΣΔMs). The first one, named UpSampling MR H-ΣΔM (US MR H-ΣΔM), increases the OSR in the back-end stages. The second one, denoted as DownSampling MR H-ΣΔM (DS MR H-ΣΔM), decreases the OSR in the back-end stages. Both MR H-ΣΔMs are compared with conventional Single-Rate cascade CT-ΣΔMs (SR CT-ΣΔMs). Theoretical calculations are given for all ΣΔMs, which are compared with time-domain simulations for different cases of signal bandwidths and effective resolutions.

2 Contribution to Value Creation

The analysis presented in this paper constitutes an essential tool for the systematic design of high-efficiency ΣΔ ADCs for the next generation of *software-defined-radio* (SDR) mobile systems integrated in nanometer CMOS technologies. The fulfillment of this global objective involves a number of technology innovations at different levels of the transceiver hierarchy – from system to device – in order to redefine the concept of wireless hand-held terminals, evolving from a pure hardware-based radio to a combination of both *hardware* and *software* [5].

In addition to allowing future mobile phones to easily accommodate new emerging standards via either software or *firmware* upgrade, the implementation of the SDR concept will make it possible the practical implementation of the so-called *cognitive radio* paradigm, that will incorporate *spectrum-sensing capabilities* to be dynamically adaptable on the fly, according to the information obtained from their interaction with the environment. The value creation of this research is backed by the European Technology Platform for Nanoelectronics (ENIAC) that, in its Strategic Research Agenda (SRA), envisions a set of markets with potential European leadership in the horizon of 2020, being communication one of the major markets [6].

3 ΣΔ Modulator Architectures Under Study

Fig. 1 shows the block diagram of the ΣΔMs under study, where $H(s)=1/s$ and $H(z)=z^{-1}/(1-z^{-1})$, denote the transfer functions of the CT and DT integrators, respectively. The same loop filter topology is used in all cases, consisting on a fourth-order cascade 2-stage architecture with embedded multi-bit quantization in both stages. However, three different topologies are considered attending to the sampling rate of each stage and its circuit nature, either CT or DT. Thus, Fig. 1(a) is a SR CT-ΣΔM, where both stages operate at the same sampling frequency, f_s. Fig. 1(b) is a US MR H-ΣΔM, where the back-end stage operates at a higher sampling frequency

than the front-end stage, i.e. $f_{s2} = r \cdot f_{s1}$, where $r > 1$ denotes the *upsampling ratio*. The opposite operation is carried out in Fig. 1(c), which corresponds to a DS MR H-ΣΔM, in which the front-end stage operates at the highest sampling rate, i.e. $f_{s1} = p \cdot f_{s2}$, with $p > 1$ being the *downsampling ratio*.

Assuming a linear model for the quantizers, it can be shown that the In-Band Noise (IBN) power at the output of the modulators in Fig. 1(a), (b) and (c) are respectively given by [1][4]:

$$\begin{aligned} \mathrm{IBN}_{\mathrm{SRCT}} &\cong \frac{\Delta^2 \pi^{2L}}{12 \cdot (2L+1) \mathrm{OSR}^{2L+1}} \\ \mathrm{IBN}_{\mathrm{USMR}} &\cong \frac{\Delta^2 \pi^{2L} r^{2L_1}}{12 \cdot (2L+1) \mathrm{OSR}_{2_{\mathrm{US}}}^{2L+1}} \\ \mathrm{IBN}_{\mathrm{DSMR}} &\cong \frac{\Delta^2 \pi^{2L} p^{2(L-L_1)+1}}{12 \cdot (2L+1) \mathrm{OSR}_{1_{\mathrm{DS}}}^{2L+1}} \end{aligned} \quad \textbf{(1)}$$

where Δ stands for the quantization step of the last quantizer; L_1=2 and L=4 are respectively the loop-filter order of the ΣΔM front-end stage and the entire modulators in Fig. 1; $\mathrm{OSR}_{\mathrm{SR}} \equiv f_s/(2B_w)$ is the OSR of the SR CT-ΣΔM [Fig. 1(a)], and $\mathrm{OSR}_{2_{\mathrm{US}}} \equiv f_{s2}/(2B_w)$ and $\mathrm{OSR}_{1_{\mathrm{US}}} \equiv f_{s1}/(2B_w)$ denote the value of the largest OSR in the US MR H-ΣΔM [Fig. 1(b)] and DS MR H-ΣΔM [Fig. 1(c)], respectively, with B_w being the signal bandwidth.

Note that the same ideal IBN can be achieved by all ΣΔMs in Fig. 1, by properly choosing the values of r, p, $\mathrm{OSR}_{\mathrm{SR}}$, $\mathrm{OSR}_{2_{\mathrm{US}}}$ and $\mathrm{OSR}_{1_{\mathrm{DS}}}$. As a case study, let us consider a maximum sampling frequency for the DS MR H-ΣΔM of $f_{s1} = 1\mathrm{GHz}$, and two different cases of B_w= 20, 40MHz, corresponding to $\mathrm{OSR}_{1_{\mathrm{DS}}} = 25$ and 12.5, respectively. This way, according to (1), the ideal value of $\mathrm{IBN}_{\mathrm{DSMR}}$ for p= 3,4,5,6 varies from −88.5dB to −46.4dB, which means that the effective resolution ranges from 7.4 bit to 14.4 bit. As an illustration, Fig. 2 shows the output spectra of the modulators in Fig. 1 for different cases of r and p, showing the variation of the notch frequency associated to the multirate operation.

4 Effect of Circuit Errors

The analysis presented above was carried out considering ideal ΣΔM building blocks. However, in practice, the performance of the modulators in Fig. 1 is degraded by circuit errors. This section analyses the IBN degradation caused by three of the most critical CT and DT non-ideal effects, namely: mismatch error, finite OTA dc gain and Gain-BandWidth (GBW) product. In order to perform this analysis, it will be assumed that the DT and CT integrators in Fig. 1 are implemented by Forward-Euler (FE) Switched-Capacitor (SC) integrators and Gm-C integrators, respectively.

4.1 Mismatch Error

Let us assume that the integrators in Fig. 1 have a gain error caused by technology process variations. In the case of SC FE integrators, this gain error – due to capacitor mismatch – is modeled as an random deviation of the integrator's weight, ε_{DT}, given by the ratio between the sampling capacitor and the integrator capacitor [7]. In the case of Gm-C realizations, integrator's weight error, ε_{CT}, is due to random variations of the time constant, i.e. the transconductance-capacitor product [1].

Considering the effect of ε_{DT} and $\varepsilon_{CT,}$ it can be shown that the IBN at the output of the ΣΔMs in Fig. 1 can be written as:

$$\begin{aligned}
\mathrm{IBN}_{\mathrm{SRCT}}^{mis} &\cong \frac{\Delta_1^2 \varepsilon_{\mathrm{CT1}}^2 \pi^{2L_1}}{12(2L_1+1)\mathrm{OSR}_{\mathrm{SR}}^{(2L_1+1)}} + \frac{\Delta_2^2 (1+\varepsilon_{\mathrm{CT2}})^2 \pi^{2L}}{12(2L_1+1)\mathrm{OSR}_{\mathrm{SR}}^{(2L+1)}} \\
\mathrm{IBN}_{\mathrm{USMR}}^{mis} &\cong \frac{\Delta_1^2 \varepsilon_{\mathrm{CT1}}^2 \pi^{2L_1} r^{(2L_1+1)}}{12(2L_1+1)\mathrm{OSR}_{2_{\mathrm{US}}}^{(2L_1+1)}} + \frac{\Delta_2^2 (1+\varepsilon_{\mathrm{DT}})^2 \pi^{2L} r^{(2L_1)}}{12(2L+1)\mathrm{OSR}_{2_{\mathrm{US}}}^{(2L+1)}} \\
\mathrm{IBN}_{\mathrm{DSMR}}^{mis} &\cong \frac{\Delta_2^2 (1+\varepsilon_{\mathrm{DT}})^2 \pi^{2L} p^{(2L_2+1)}}{12(2L+1)\mathrm{OSR}_{1_{\mathrm{DS}}}^{(2L+1)}} + \frac{\Delta_1^2 \pi^{2L_1}}{12(2L_1+1)\mathrm{OSR}_{1_{\mathrm{DS}}}^{(2L_1+1)}} \cdot \sum_{k=0}^{p-1} \left[\left| \alpha \varepsilon_{\mathrm{CT11}} + \frac{\beta}{2} \varepsilon_{\mathrm{CT12}} \right|^2 \right]
\end{aligned} \tag{2}$$

where $\Delta_{1,2}$ stands for the quantization step of the front-end and the back-end quantizers; ε_{CTij} denote the weight error of the *j*-th Gm-C integrator in the *i*-th stage $(i, j = 1, 2)$ and $\alpha = 2\exp(-j2\pi k/p) - \exp(-j4\pi k/p)$ and $\beta = \exp(-j2\pi k/p) + \exp(-j4\pi k/p)$.

4.2 Finite dc gain

Let us consider now that the integrators in Fig. 1 have a finite OTA dc gain. This effect can be modeled as a finite dc gain of the opamp in SC integrators [7] and a finite output resistance of the transconductor circuit in Gm-C integrators [1]. Thus, taking into account this effect on the integrators transfer functions, it can be demonstrated that the IBN at the output of the modulators in Fig. 1 is given by:

$$\begin{aligned}
\mathrm{IBN}_{\mathrm{SRCT}}^{gain} &\cong \frac{\Delta_1^2 \mu_1^2 \pi^{2L_1-2}}{12(2L_1-1)\mathrm{OSR}_{\mathrm{SR}}^{(2L_1-1)}} + \frac{\Delta_2^2 \pi^{2L}}{12(2L+1)\mathrm{OSR}_{\mathrm{SR}}^{(2L+1)}} + \frac{\Delta_2^2 \mu_2^2 \pi^{2L-2}}{12(2L-1)\mathrm{OSR}_{\mathrm{SR}}^{(2L-1)}} \\
\mathrm{IBN}_{\mathrm{USMR}}^{gain} &\cong \frac{\Delta_1^2 \mu_1^2 \pi^{2L_1-2} r^{2L_1-1}}{12(2L_1-1)\mathrm{OSR}_{2_{\mathrm{US}}}^{(2L_1-1)}} + \frac{\Delta_2^2 \pi^{2L} r^{2L_1}}{12(2L+1)\mathrm{OSR}_{2_{\mathrm{US}}}^{(2L+1)}} + \frac{\Delta_2^2 \mu_2^2 \pi^{2L-2} r^{2L_1}}{12(2L-1)\mathrm{OSR}_{2_{\mathrm{US}}}^{(2L-1)}} \\
\mathrm{IBN}_{\mathrm{DSMR}}^{gain} &\cong \frac{\Delta_1^2 \mu_1^2 \pi^{2L_1-2} p^{2L_1-1}}{12(2L_1-1)\mathrm{OSR}_{1_{\mathrm{DS}}}^{(2L_1-1)}} + \frac{\Delta_2^2 \pi^{2L} p^{2L_2+1}}{12(2L+1)\mathrm{OSR}_{1_{\mathrm{DS}}}^{(2L+1)}} + \frac{\Delta_2^2 \mu_2^2 \pi^{2L-2} p^{2L_2-1}}{12(2L-1)\mathrm{OSR}_{1_{\mathrm{DS}}}^{(2L-1)}}
\end{aligned} \tag{3}$$

where $\mu_i = 1/A_{\mathrm{DCi1}} + 1/A_{\mathrm{DCi2}}$ and $A_{\mathrm{DC}ij}$ is the dc gain of the *j*-th integrator in the *i*-th stage.

4.3 Gain-Band Width product

Following the same procedure as in previous sections, it can be found that the IBN degradation caused by the effect of the integrators' GBW has the same expressions as those shown in (2), but considering that in this case $\varepsilon_{CTij} = f_s / \mathrm{GBW}_{ij}$ and $\varepsilon_{DTij} = \exp(-\pi \mathrm{GBW}_{ij} / f_s)$, where GBW_{ij} stands for the GBW of the *j*-th integrator in the *i*-th stage.

5 Simulation Results

In order to verify the theoretical analysis described in previous sections and to compare the performance of the different approaches in Fig. 1, the ΣΔMs under study were simulated using SIMSIDES – a time-domain behavioral simulator for ΣΔMs [8]. To make a fair comparison, the same ideal conditions, $r = p$ [with $r = p = 1$ in Fig. 1(a)] were assumed and the values of the OSR for each modulator was computed from (1), so that the same ideal IBN is achieved in all cases. The same embedded quantizers were used in all ΣΔMs, considering 4-bit quantization in both stages. Two values of signal bandwidths were simulated, $B_w = 20, 40\mathrm{MHz}$ and a 1-MHz input tone with amplitude −7dB below quantization full-scale range was applied in all cases. For the sake of simplicity, only the effect of errors associated to the front-end (CT) integrators – which are common in all the ΣΔ architectures in Fig. 1 – will be taken into account in the simulations.

Fig. 3 shows the impact of finite dc gain error of the first Gm-C integrator for the ΣΔMs under study. Note that both theoretical predictions and simulation results are in good agreement, showing that the DS MR H-ΣΔM is the least sensitive to the impact of this error, while US MR H-ΣΔM presents the worst performance.

The impact of GBW is illustrated in Fig. 4, highlighting a good matching between theory and simulations, and showing the worst performance for the US MR H-ΣΔM, while similar degradation is roughly obtained for the DS MR H-ΣΔM and the SR CT-ΣΔM, the latter achieving a higher robustness against the impact of GBW in the first integrator.

Finally, Fig. 5 shows the effect of mismatch and circuit element tolerances. It can be noted how both theoretical calculations and simulations demonstrate that the DS MR H-ΣΔM achieves the largest robustness against circuit element tolerances, getting better as both *p* and B_w increases.

Conclusions

Different approaches for the implementation of multirate cascade hybrid continuous-time/discrete-time ΣΔ modulators have been discussed. One of them increases the clock rate across the cascade while the other uses a lower oversampling ratio in the back-end stage. Both multirate cascade topologies have been compared to conventional single-rate cascade continuous-time ΣΔ modulators. The effect of main circuit errors has been theoretically analyzed and verified by time-domain simulations, demonstrating that the downsampling multirate architecture exploits the capability of continuous-time circuits to operate at higher frequencies with less power consumption, while keeping a higher robustness against circuit errors. These characteristics make these new kinds of ΣΔ modulators very suited candidates for the implementation of analog-to-digital converters in the next generation of software-defined-radio based mobile terminals.

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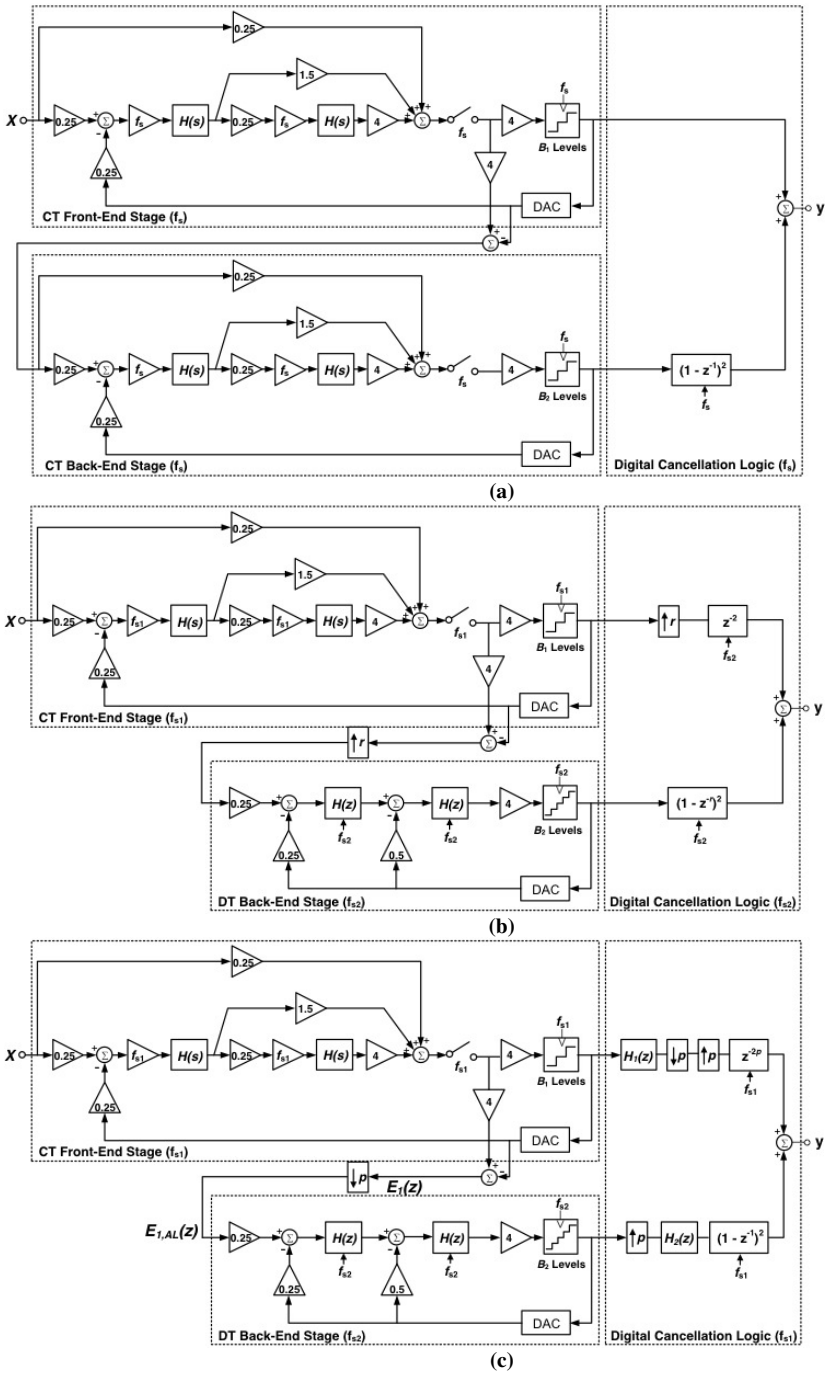
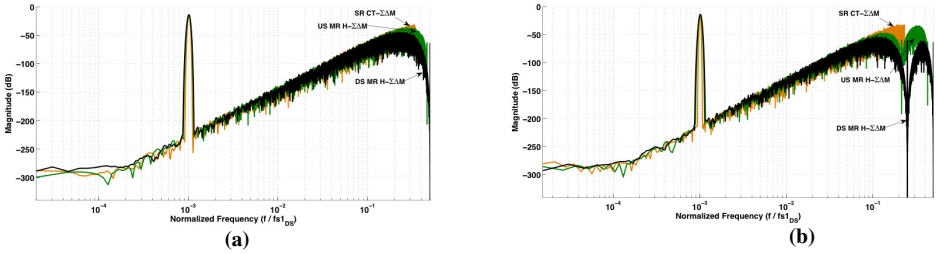
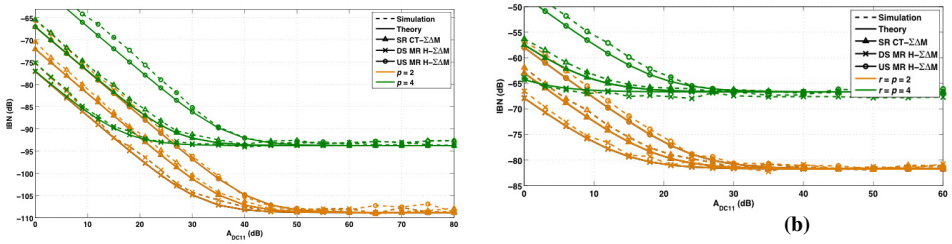


Fig. 1 Block diagrams of the ΣΔMs: **(a)** CT-ΣΔM, (b) US MR H-ΣΔM, (c) DS MR H-ΣΔM.



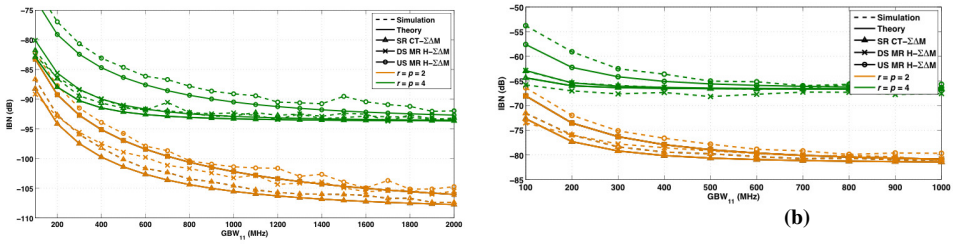
(a) **(b)**

Fig. 2 Output spectra of the ΣΔMs in Fig. 1 for: (a) r=p=2 and (b) r=p=4.



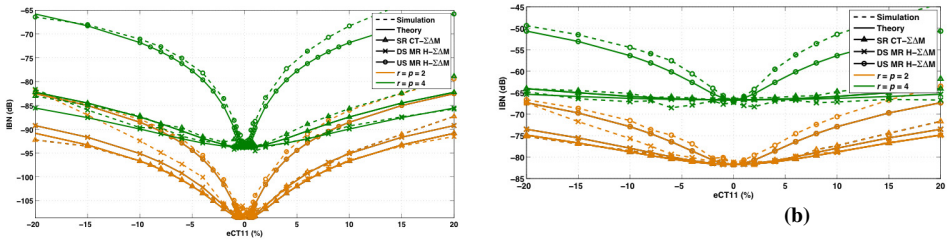
(a) **(b)**

Fig. 3 IBN vs. finite dc gain for: (a) B_W= 20MHz and (b) B_W= 40MHz.



(a) **(b)**

Fig. 4 IBN vs. GBW for: (a) B_W= 20MHz and (b) B_W= 40MHz.



(a) **(b)**

Fig. 5 IBN vs. mismatch error for: (a) B_W= 20MHz and (b) B_W= 40MHz.