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► **To cite this version:**

João Casaleiro, Luís B. Oliveira. A High-Level Model for Capacitive Coupled RC Oscillators. 3rd Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS), Feb 2012, Costa de Caparica, Portugal. pp.429-436, 10.1007/978-3-642-28255-3_47. hal-01365756

HAL Id: hal-01365756

<https://inria.hal.science/hal-01365756>

Submitted on 13 Sep 2016

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A High-Level Model for Capacitive Coupled RC Oscillators

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Abstract. In this paper a high-level model is proposed for quadrature oscillators that are based on two RC oscillators with capacitive coupling. The capacitive coupling technique has the advantages of being noiseless and not increasing the power requirements, which are important features for low power receivers. This coupling technique was already study for LC oscillators but not for RC oscillators. Simulations showed that the behavior of capacitive coupling in RC oscillators is different than for LC. In opposition to what was expected, in RC oscillators, the oscillation frequency increases almost linearly and proportional to the coupling capacitances. This behavior can be explained by the presented model. Simulations are presented to validate the model in respect to the oscillation frequency and to the output phases of the oscillator.

Keywords: Quadrature oscillators, RC oscillators, Capacitive coupling, High-level model.

1 Introduction

Quadrature oscillators are key blocks in the design of modern transceivers. In recent years, significant research efforts have been invested in the study of oscillators with accurate quadrature outputs, with particular emphasis on cross-coupled RC and LC oscillators [1],[2],[3].

Typically, coupled oscillators require two extra gain blocks with current sources. This increases the power dissipation, reduces the oscillation frequency [1], and prevents use of low supply voltages. Recently, capacitive coupling has been proposed for LC oscillators [4],[5] to obtain in-phase and quadrature outputs. This solution, in opposite to the traditional active coupling, does not add extra noise sources and does not increase the power consumption but has the disadvantage of lowering the oscillation frequency.

It is known that inductorless (RC) oscillators [1],[2] occupy less area than LC oscillators. Since they do not require technologies with many metal layers and a thick top layer for the design of high Q inductors, their fabrication cost is much lower.

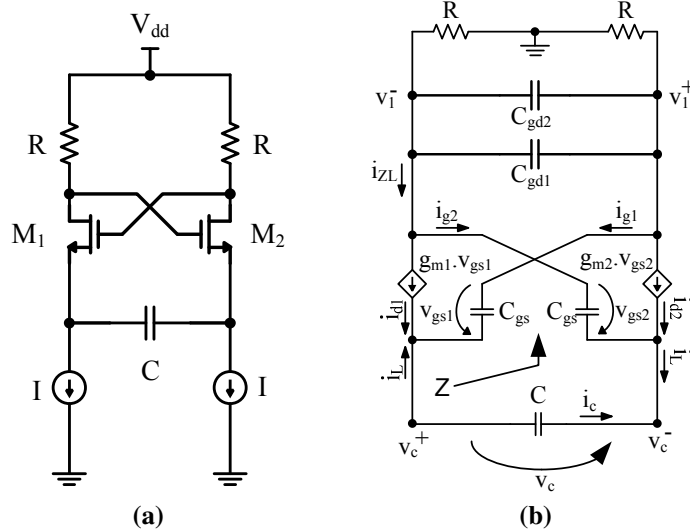


Fig. 1. a) Single RC oscillator. b) Small-signal circuit

In this paper we investigate quadrature RC oscillators with capacitive coupling and present a novel approach to explain the relation between the coupling factor and the oscillation frequency. Section 2 presents the main contribution of this work for technological innovation. In Section 3, we review the analysis of a single RC oscillator working in the near sinusoidal regime presenting the equations for the amplitude and frequency of the oscillator. In Section 4, the capacitive coupling and the oscillation frequency are discussed and the frequency locking between the two oscillators is explained. The high-level model based on the frequency locking is explained in Section 5. The simulation results are presented in Section 6 and in Section 7, some general conclusions are drawn.

2 Contribution to Value Creation

The main application of this work is to aid in the design of RC quadrature oscillators with capacitive coupling, focusing mainly on the low power and low area. With the proposed model the integrated circuit (IC) design time is decreased and the circuit area and power requirements are minimized, which reduce the overall cost of the IC leading to a strong contribution to the value creation.

3 Single Oscillator

The source-coupled oscillator, presented in Fig. 1a, working in near sinusoidal regime was extensively study in [6],[7].

To determine the oscillation frequency at nearly sinusoidal regime, one needs to determine the impedance, $Z=v_e/i_e$, seen from the transistors sources, using the small-signal equivalent circuit, without the timing capacitor C , as shown in Fig. 1b. Assuming that the circuit has no mismatch, the impedance, Z , is given by,

$$Z(s) \approx 2 \underbrace{\left(\frac{1}{g_m} - R\right)}_{\text{Real term}-R_e} + s 2 \underbrace{\frac{R}{g_m} (4C_{gd} + C_{gs})}_{\text{Imaginary term}-j\omega L_e} \quad (1)$$

Where g_m represents the transistor M_1 and M_2 transconductances, C_{gd} and C_{gs} are the gate to drain capacitances and gate to source capacitances respectively of both transistors M_1 and M_2 .

From (1) one can conclude that the circuit can be simplified to a RL circuit. And that the overall circuit is an RLC. In order to oscillate, the real part of (1), R_e , must be zero or negative, which is rather simple if the resistors value is higher than the inverse of M_1 and M_2 transconductances, *i.e.* $R > 1/g_m$. In this case, the oscillation frequency is given by

$$\omega = \frac{1}{\sqrt{2 \frac{R}{g_m} (4C_{gd} + C_{gs}) C}} \quad (2)$$

Where C is the timing capacitor of the oscillator.

To determine the steady-state amplitude is necessary to add the nonlinearities of the circuit, which will limit the amplitude of oscillation and introduce a neglectable shift on the oscillation frequency if timing capacitor C is much larger than the sum of gate to drain capacitances C_{gd} . The strongest nonlinearities of the circuit are introduced by the transconductances of transistor M_1 and M_2 , which suffer a drift from their nominal value for large signal swings. Thus, to determine the oscillator differential equation one must assume that the transconductance g_{m1} and g_{m2} are different, $g_{m1} \neq g_{m2}$. The oscillator characteristic equation can be reduced to the Van der Pol equation [5], using the notation $x=i_e/I$,

$$\frac{d^2x}{dt^2} - 2(\delta_0 - \delta_2 x^2) \frac{dx}{dt} + \omega_0^2 x = 0 \quad (3)$$

where

$$\delta_0 = \frac{Rg_{m0} - 1}{2R(4C_{gd} + C_{gs})} \quad (4)$$

and

$$\delta_2 = \frac{Rg_{m0}K}{2R(4C_{gd} + C_{gs})} \quad (5)$$

where K is a fitting parameter to compensate the equations simplification.

The solution for (3) is of the form,

$$x(t) = A \cdot \sin(\omega_0 t) \quad (6)$$

where A represents the amplitude of oscillation that is given by

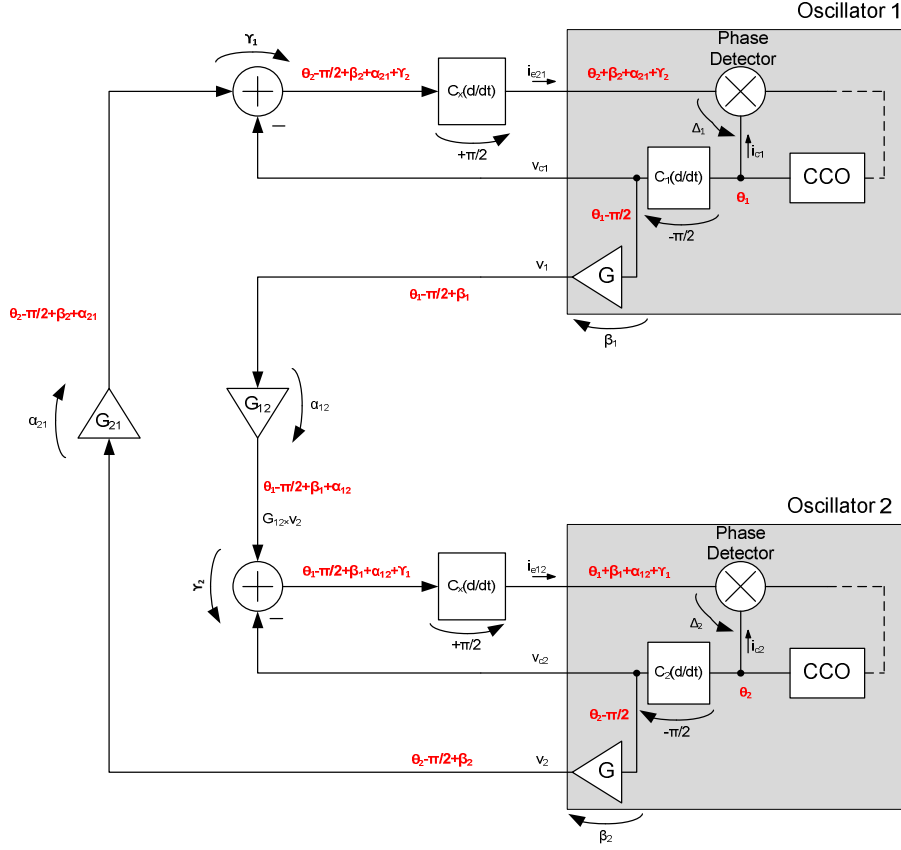


Fig. 3. The block diagram of the high-level model with the phase shift of each block

Where the oscillators are represented by a first-order phase lock loop (PLL) – gray box –, with the instantaneous frequency (8). The coupling is modeled by two gain blocks, G_{21} and G_{12} ; and the conversion from voltage to current – performed by the coupling capacitors C_X – are modeled by differential blocks with gain C_X .

Assuming a locked state, where the frequency of oscillation is equal for both oscillators, and assign generic phase shifts for each block, one can derive the following system of equations:

$$\begin{cases} \Delta_1 = (\theta_2 + \beta_2 + \alpha_{21} + \gamma_2) - \theta_1 \\ \Delta_2 = (\theta_1 + \beta_1 + \alpha_{12} + \gamma_1) - \theta_2 \end{cases} \quad (9)$$

where Δ represents the phase difference between currents i_e and i_c , θ is the oscillator absolute phase, β represents the phase shift between lower and upper parts of the oscillator, i.e. phase between v_c and v , α is the phase shift introduced by the coupling and γ the phase difference inserted by the amplitude difference in the coupling capacitor. All symbols are indexed accordingly to its oscillator number.

Assuming no mismatch $\Delta_1=\Delta_2$, $\beta_1=\beta_2$ and $Y_1=Y_2$, the phase difference between the oscillators are given by

$$(\theta_2 - \theta_1) = \frac{\alpha_{12} - \alpha_{21}}{2} \quad (10)$$

From (10) it is possible derive the values in Table I, which are in accordance with the conclusions of [8], that a system with N coupled differential oscillators produces outputs with a phase shift of π/N . To obtain quadrature outputs one of the couplings should be direct and other crossed.

Table 1. Oscillator phase output

Coupling Oscillator 1 to Oscillator2		Coupling Oscillator 2 to Oscillator1		Phase output	
G_{12}	α_{12}	G_{21}	α_{21}	$\theta_2 - \theta_1$	
1	0 (2π)	1	0 (0)	0 (π)	In-phase
-1	π	1	0	$\pi/2$	Quadrature
1	0	-1	π	$\pi/2$	Quadrature
-1	π (2π)	-1	π (0)	0 (π)	In-phase

If both couplings are either crossed or direct then outputs can be in-phase or in opposition of phase (dependent on the initial conditions).

The dependence of the frequency by the coupling capacitances C_X can be explained using (8). If one increased the value of C_X the current i_e also increase and as a result the frequency will be dependent on the term $\cos(\Delta)$. If the cosine value is positive – which is the case for $\theta_2 - \theta_1 = \pi/2$ – the frequency increases. If the cosine value is negative – which is the case for $\theta_2 - \theta_1 = 0$ – the frequency decreases.

6 Simulations and Results

The circuit in Fig. 2 was simulated using the Cadence Spectre and SpectreRF and UMC 130 nm CMOS technology library. The oscillator was designed for a nominal frequency, f_0 , around 1.9 GHz. Transistors M_1 , M_2 , M_3 and M_4 have $W=7.2 \mu\text{m}$, $L = 120 \text{ nm}$. The current sources I , implemented as single transistors with $W=7.2 \mu\text{m}$, $L = 360 \text{ nm}$ (not shown in the circuits). The resistors (Fig. 2) are also from the technology library; they have $W = 1 \mu\text{m}$ and $L = 1.6 \mu\text{m}$ which results in $R=185.4 \Omega$. The timing capacitance are implemented using two parallel capacitors with $W = 11 \mu\text{m}$ and $L = 22 \mu\text{m}$, resulting in a capacitance of 431.7 fF. The coupling capacitances C_X was changed from 0 fF up to 200fF. The supply voltage is 1.2 V, and the bias current is 550 μA .

Fig. 4 shows the results of the simulations – for several frequencies – of a single RC oscillator with a current source i_e in parallel with the timing capacitor. As can be seen the oscillator locks to the frequency of the external source – up to the limit

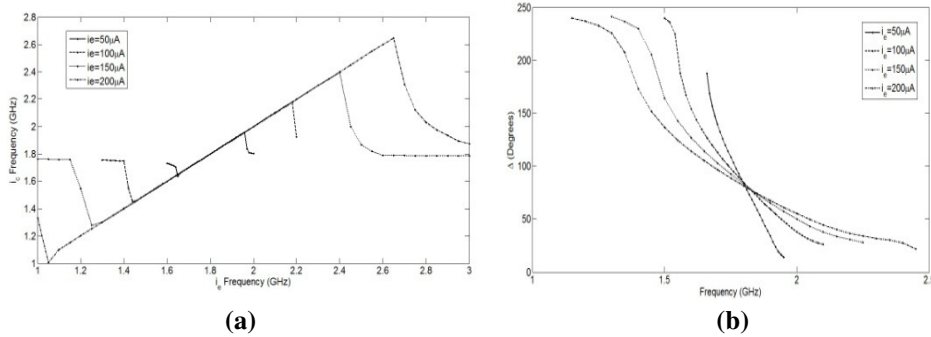


Fig. 4. a) Frequency of i_e and i_c ; b) The i_c and i_e phase difference

imposed by the i_e/i_c ratio – and the phase difference between both currents is presented in Fig. 4b. The oscillator returns to its nominal frequency f_0 when the external/forced frequency is above the locking range. This result clearly shows that the oscillator behaves like a phase lock loop.

Fig. 5 shows the simulation results of two coupled RC oscillators (circuit of Fig. 2). The value of the coupling capacitances was changed from 0 to 200 fF. Fig. 5b shows the frequency increase almost linear in relation to the C_X value. Fig. 5a shows that a coupling capacitance above 10 fF locks the two oscillators to each other and generate four phases with $\pi/2$ phase difference.

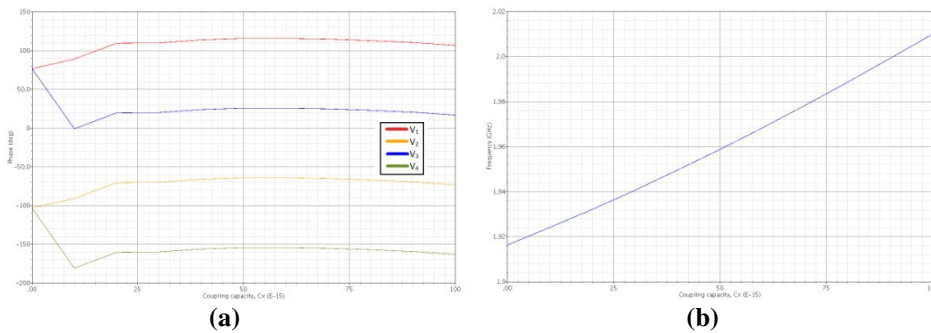


Fig. 5. Phase difference between i_e and i_c as a function of the i_e frequency

7 Conclusions

This work presented a high-level model for RC quadrature oscillators capacitive coupled and demonstrated by simulations that the RC oscillator behaves like a PLL. The objective of the model is to better explain the three possible modes of oscillation – in-phase, quadrature and phase opposition – and the frequency relation to the coupling factor for all modes.

Simulations showed that the in-phase and phase opposition modes are strongly dependent of the circuit initial conditions. Essential because for non-crossed and

double crossed connections both modes are stable. In these two modes the frequency always decrease when the coupling factor grow. For the quadrature mode the frequency increases proportional to the coupling factor.

The locking range of each oscillator is directly proportional to the ratio of the coupling currents and the timing capacitor current.

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