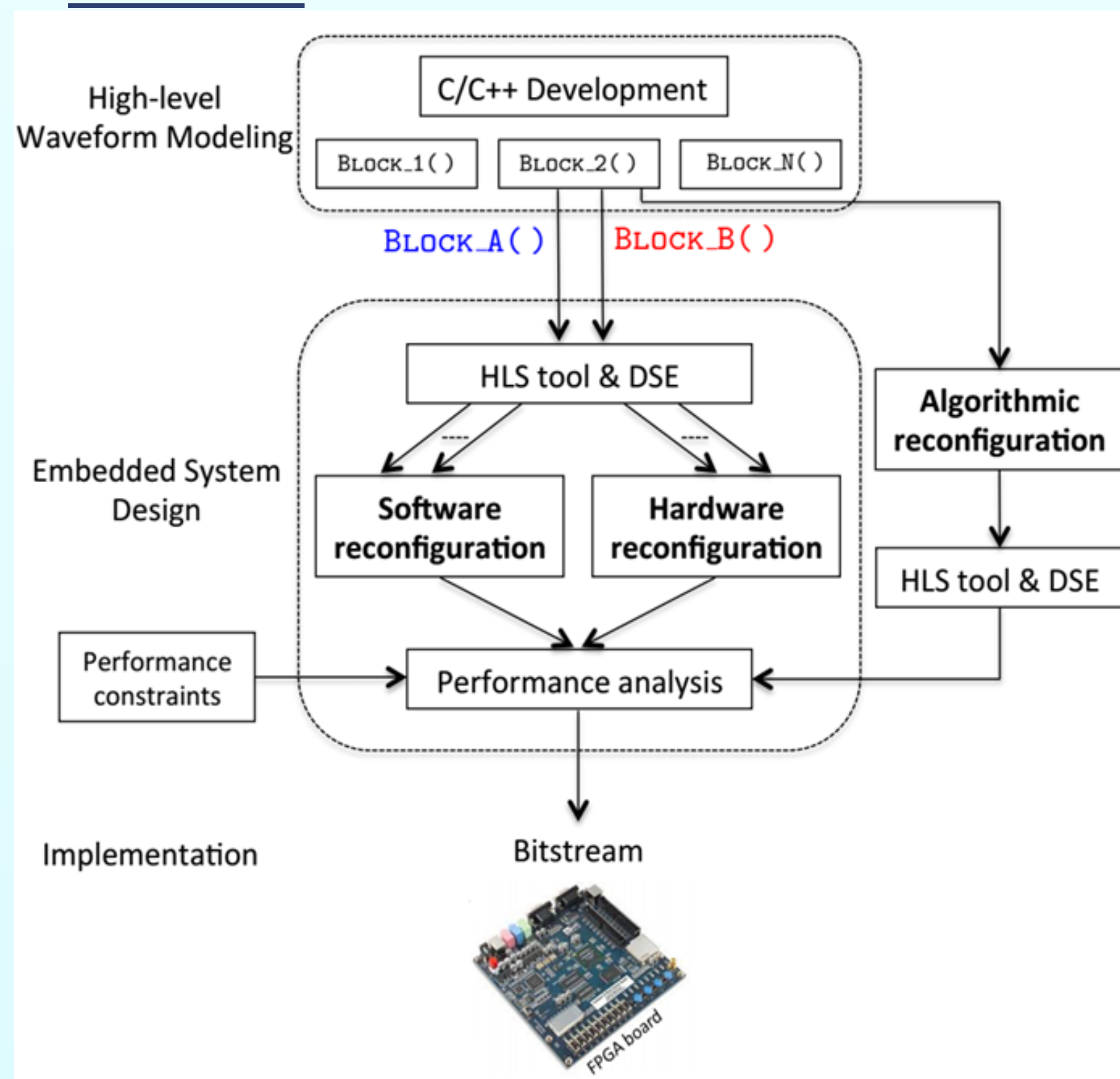


## FPGA-based implementation of a flexible FFT dedicated to LTE standard

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### Abstract

The Field Programmable Gate Array (FPGA) technology is expected to play a key role in the development of Software Defined Radio (SDR) platforms. To this aim, leveraging the nascent High-Level Synthesis (HLS) tools, a design flow from high-level specifications to Register-Transfer Level (RTL) description can be thought to generate processing blocks that can be reconfigured at run-time. Based on such a flow, this demo describes the architectural exploration of a Fast Fourier Transform (FFT) for Long Term Evolution (LTE) standard. Synthesis results show the tradeoff between reconfiguration time and area that can be achieved with such an approach.



Generation of multi-mode processing block

### Design flow for Software Defined Reconfiguration

**Algorithm 1** Automatic generation of a multi-mode processing block

```
function MULTI_MODE_BLOCK(inputs, outputs, control)
  switch control do
    case A
      BLOCK_A(inputs, outputs)
    case B
      BLOCK_B(inputs, outputs)
  end function
```

Processing block	BLOCK_FFT128()	BLOCK_FFT2048()	Two_Mode_BLOCK()
BRAM	6	12	12
DSP	17	65	82
LUT	1017	2522	3459
FF	862	2443	3241
Latency	5362	72410	5491/72411

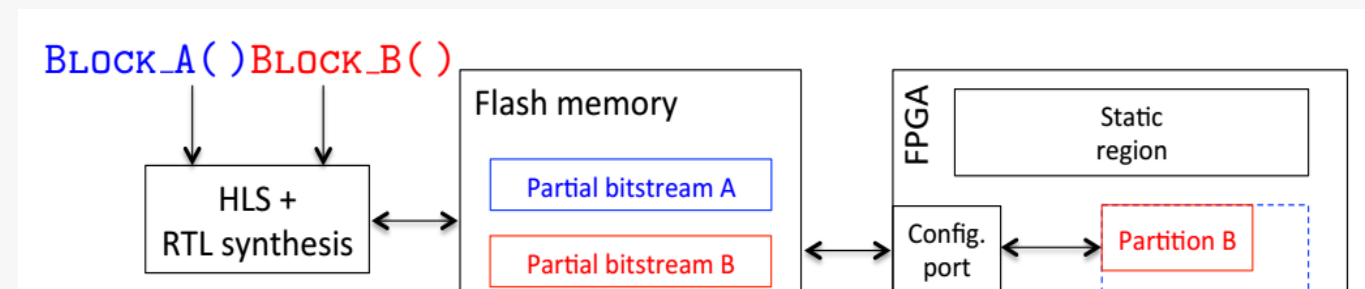
Latency: computation time in clock cycle

Software reconfiguration with two FFT modes(128/2048)

Pros	Cons
Simplicity, Rapid prototyping, Short reconfiguration time	High resources (Sharing hard to achieve)

### Software reconfiguration

	Processing block: Resources needed		Partition: Resources used		
	FFT 128	FFT 4048	FFT 128	FFT 4048	FFT 128/4048
BRAM	6	12	6	17	17
DSP	17	65	24	68	68
LUT	1017	2522	1440	4080	4080
FF	862	2443	2880	8160	8160
Bitstream size	n/a	n/a	138672 Bytes	410016 Bytes	2 x 410016 Bytes
Reconf. time	n/a	n/a	10.98 ms	32.9 ms	32.9 ms
Latency	5362	72410	5362	72410	5362/72410



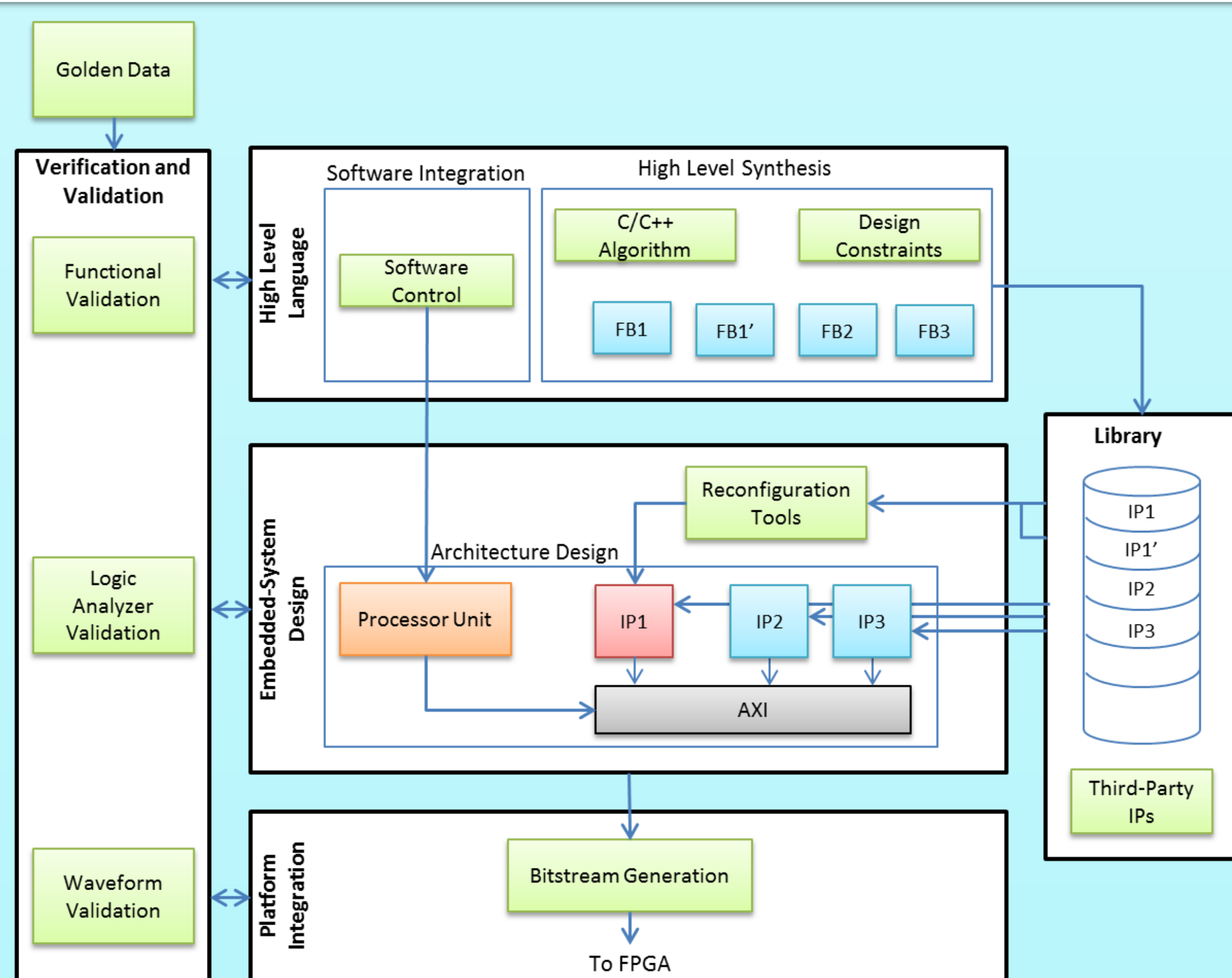
Pros	Cons
Low number of resources	Reconfiguration time depending on partial bitstream size. Memory cost

### Hardware reconfiguration

Pros	Cons
Low number of resources, Short reconfiguration time	Coding may be complex

### Algorithmic reconfiguration

- Algorithmic optimizations to share the resources between modes
- Hand-coding of a dedicated processing block being intrinsically flexible
- Control signals to switch between modes



The design flow for Software Defined Reconfiguration

### Building a flexible FFT for LTE standard

- FFT with six different lengths for OFDM

- 128, 256, 512, 1024, 1536, 2048

- Power-of-two point FFT:

- Algorithmic reconfiguration
- Radix-2 Decimation-In-Time is used

- Flexible FFT for LTE

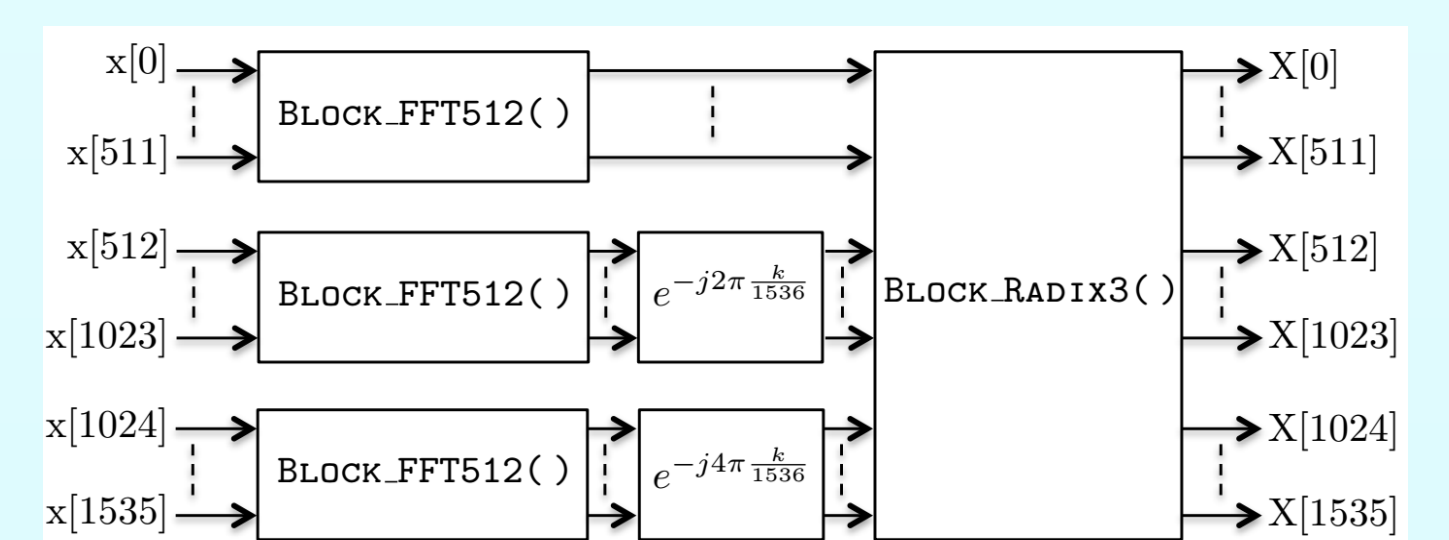
- Hardware reconfiguration

between Power-of-two point and 1536-point FFTs

**Algorithm 2** Algorithmic reconfiguration for the power-of-two point FFT

```
function BLOCK_FFTpow2(inputs, outputs, control)
  FFT_size_max = 2048
  FFT_stages_max = 11
  FFT_size = FFT_size_max >> control
  FFT_stages = FFT_stages_max - control
  Bit.reverse()
  for i = 0 to FFT_stages do
    Calculate_index()
    for j = 0 to FFT_size/2 do
      Computing_twiddles()
      for k = 0 to FFT_size/2 do
        Radix_2(inputs, outputs)
      end function
```

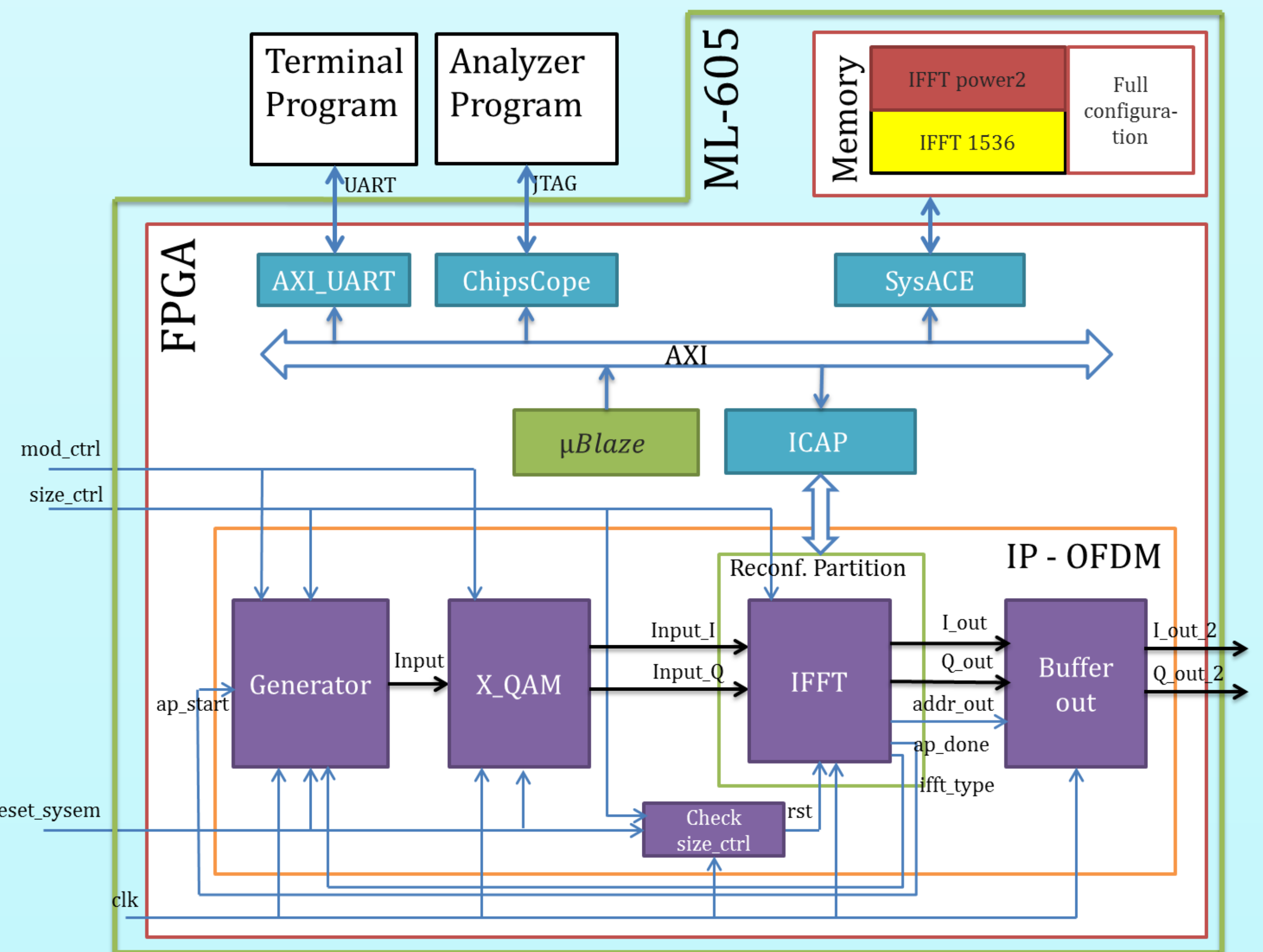
### FFT power-of-two point



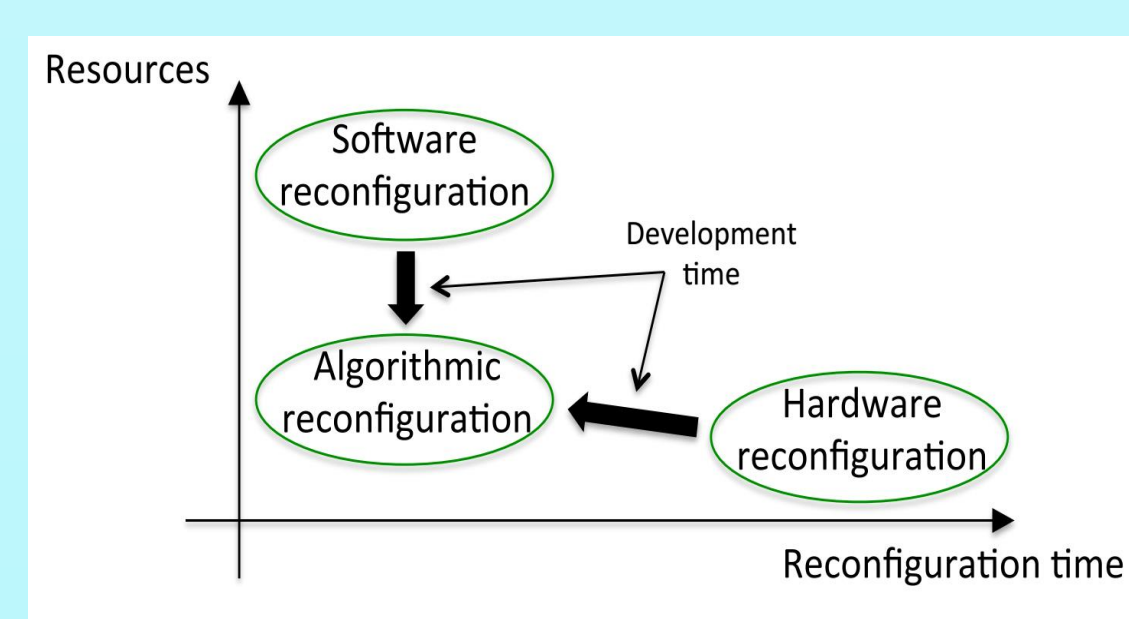
### FFT 1536-point

	Processing block	Software reconfiguration	Hardware reconfiguration
	BLOCK_FFTpow2()	BLOCK_FFT1536()	MULTI_MODE_BLOCK_LTE()
BRAM	12	14	26
DSP	65	40	103
LUT	2553	3054	5256
FF	2497	2010	4299
Bitstream size	n/a	n/a	n/a
Reconf. time	n/a	n/a	10 ns
Latency	3555 / 7604 / 16172 34284 / 72412	52198	3555 / 7604 / 16172 34284 / 72412 / 52198

### Results of a flexible FFT



The design on ML605 board



Tradeoff between resources and reconfiguration time & the board

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