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Process-level Power Estimation in Multi-core Architectures

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Process-level Power Estimation in Multi-core Architectures *

Maxime Colmant, Romain Rouvoy, Lionel Seinturier

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Motivation

Problem

- Hard to identify the largest power consumers
- Power meters are not fine-grained enough
- Limited number of processor-agnostic solutions
- Limited number of power-aware interfaces

Vision

- Software-defined power meters
- Support for all CPU features
- Provide critical indicators

Metrics

Hardware (HW) Performance Counters

- Representative and accurate metrics
- Mostly available on modern processors

Criteria selection

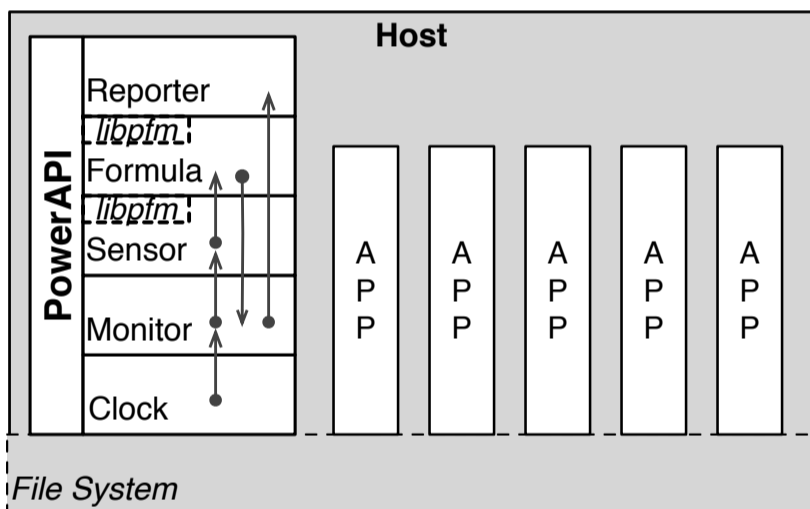
- Counter availability per CPU
- Monitoring overhead
- Best fit under several workloads

Selected HW Performance Counters

- CPU_CLK_UNHALTED:THREAD_P (uc)
- CPU_CLK_UNHALTED:REF_P

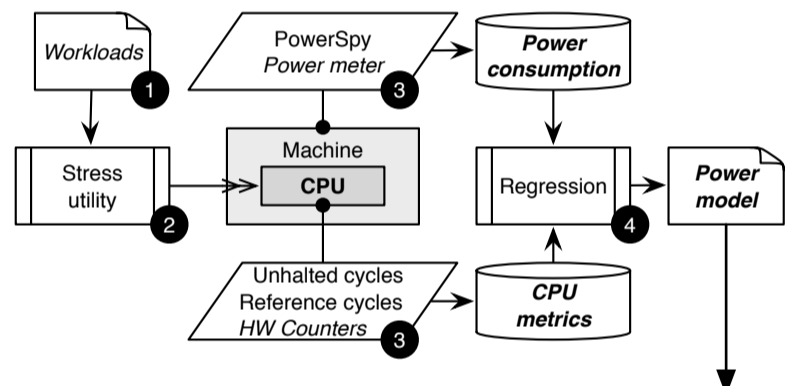
PowerAPI

Implementation



Available online:
<http://powerapi.org>

Learn the CPU power model

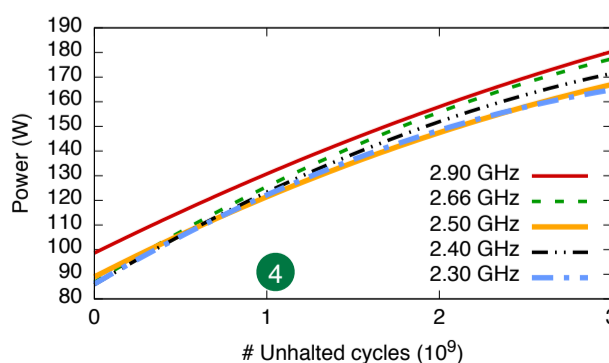
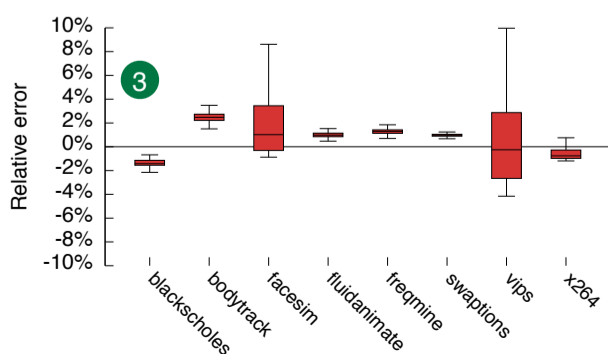
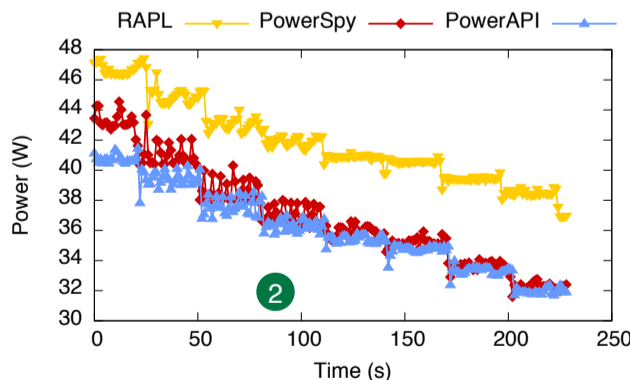
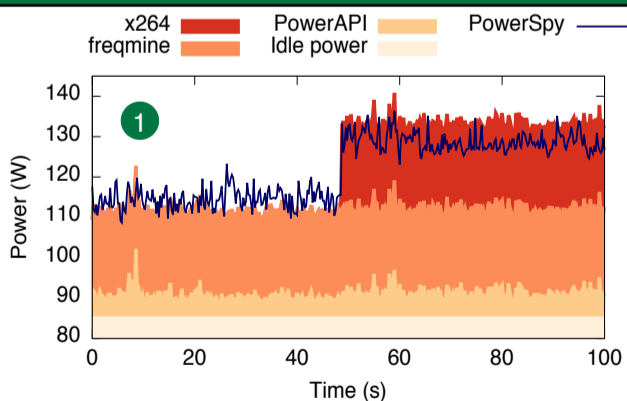


Power Model

$$P_{host}(f) = P_{idle}(f) + \sum_{pid \in PIDs} P_{cpu}(f, uc_{pid}^1 \dots uc_{pid}^N)$$

$$P_{cpu}(f, uc_{pid}^1 \dots uc_{pid}^N) = \sum_{n=1}^N P_f(uc_{pid}^n)$$

Validation



- 1 Process-level power consumption of PowerAPI, x264, and freqmine on a Xeon W3520 processor
- 2 Decreasing load of stress on a i3 2120 processor, compared to RAPL
- 3 Relative error distribution of the PARSEC benchmarks on a Xeon W3520 processor
- 4 Power models for the highest frequencies on a Xeon W3520 processor