



HAL
open science

Hardware and Arithmetic for Hyperelliptic Curves Cryptography

Gabriel Gallin, Arnaud Tisserand, Nicolas Veyrat-Charvillon

► **To cite this version:**

Gabriel Gallin, Arnaud Tisserand, Nicolas Veyrat-Charvillon. Hardware and Arithmetic for Hyperelliptic Curves Cryptography. RAIM: 7ème Rencontre Arithmétique de l'Informatique Mathématique, Apr 2015, Rennes, France. , 2015. hal-01134020

HAL Id: hal-01134020

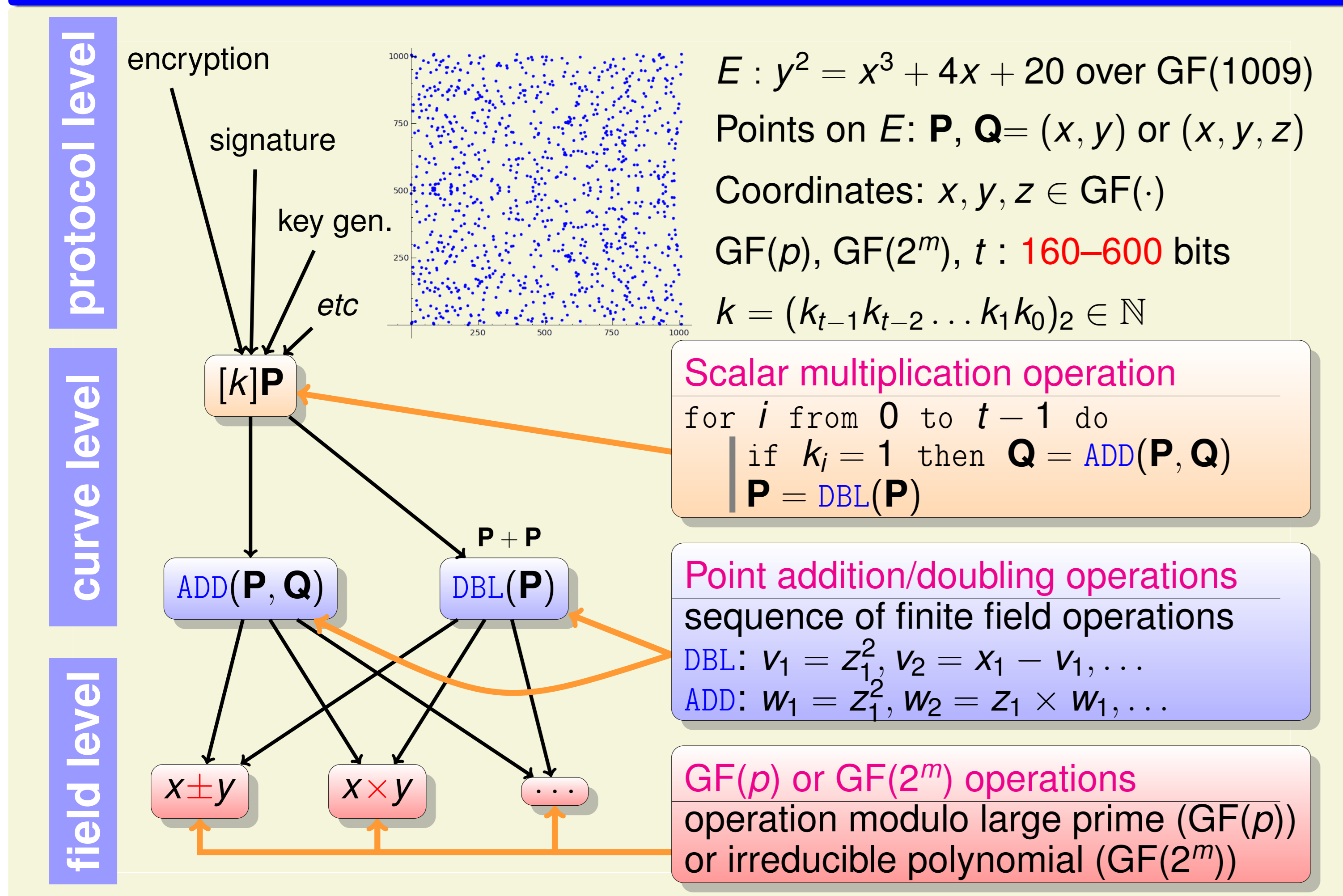
<https://inria.hal.science/hal-01134020>

Submitted on 29 Mar 2015

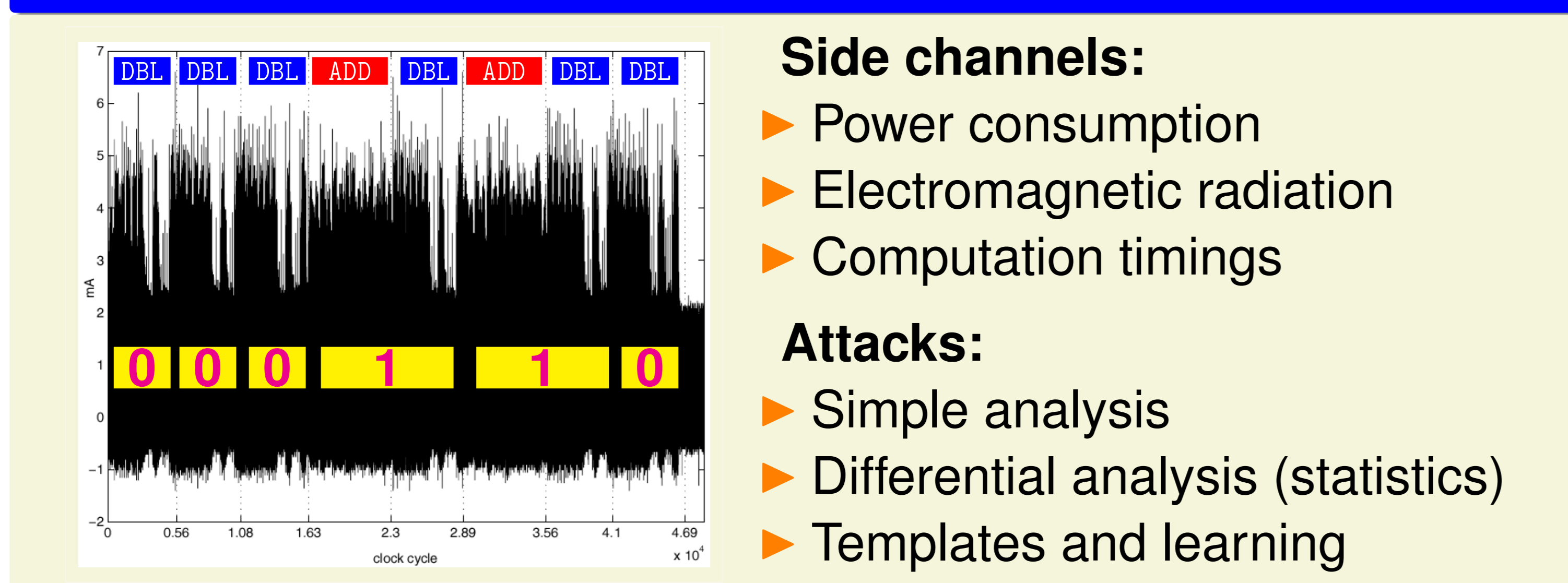
HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

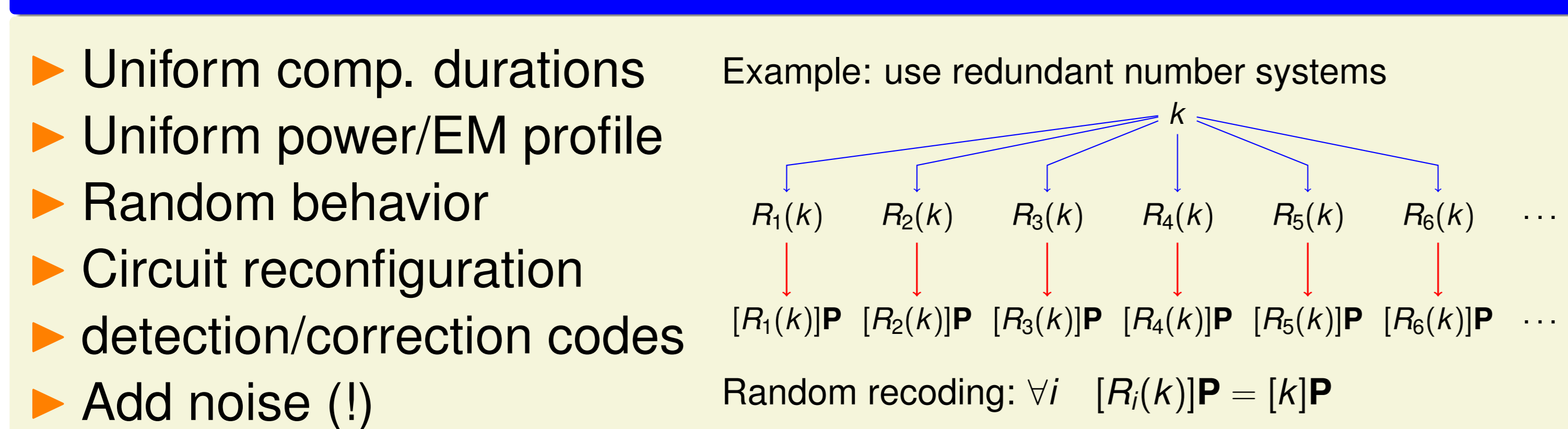
1. Elliptic Curve Cryptography (ECC)



2. Side Channel Attacks (SCAs)



3. Protections & Counter-Measures Against SCAs



4. From ECC to HECC

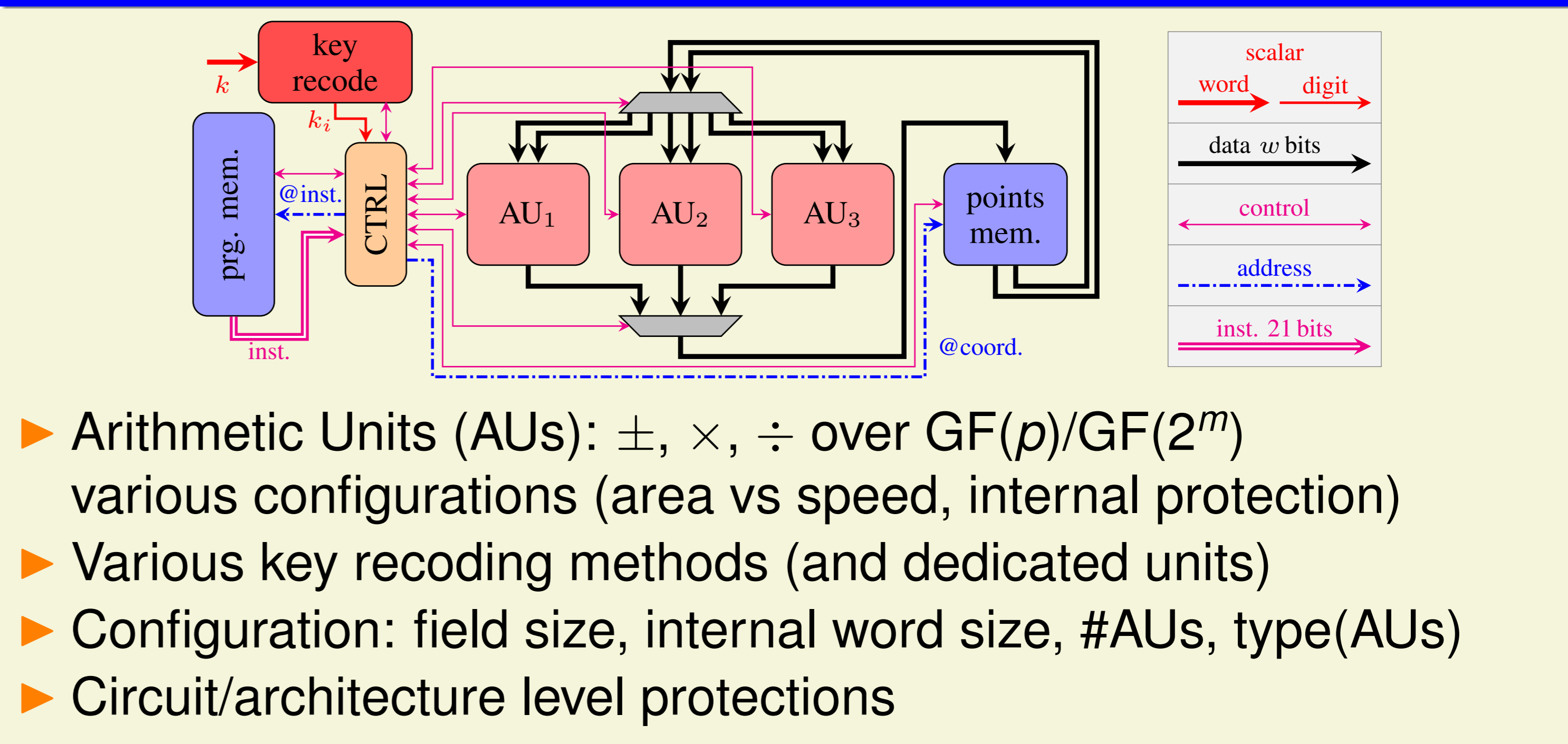
	field size	ADD	DBL
ECC	ℓ bits	Cost: 12M + 2S	Cost: 6M + 5S
HECC	$\frac{\ell}{2}$ bits	Cost: 47M + 4S	Cost: 38M + 6S

Examples of computation expressions for projective coordinates

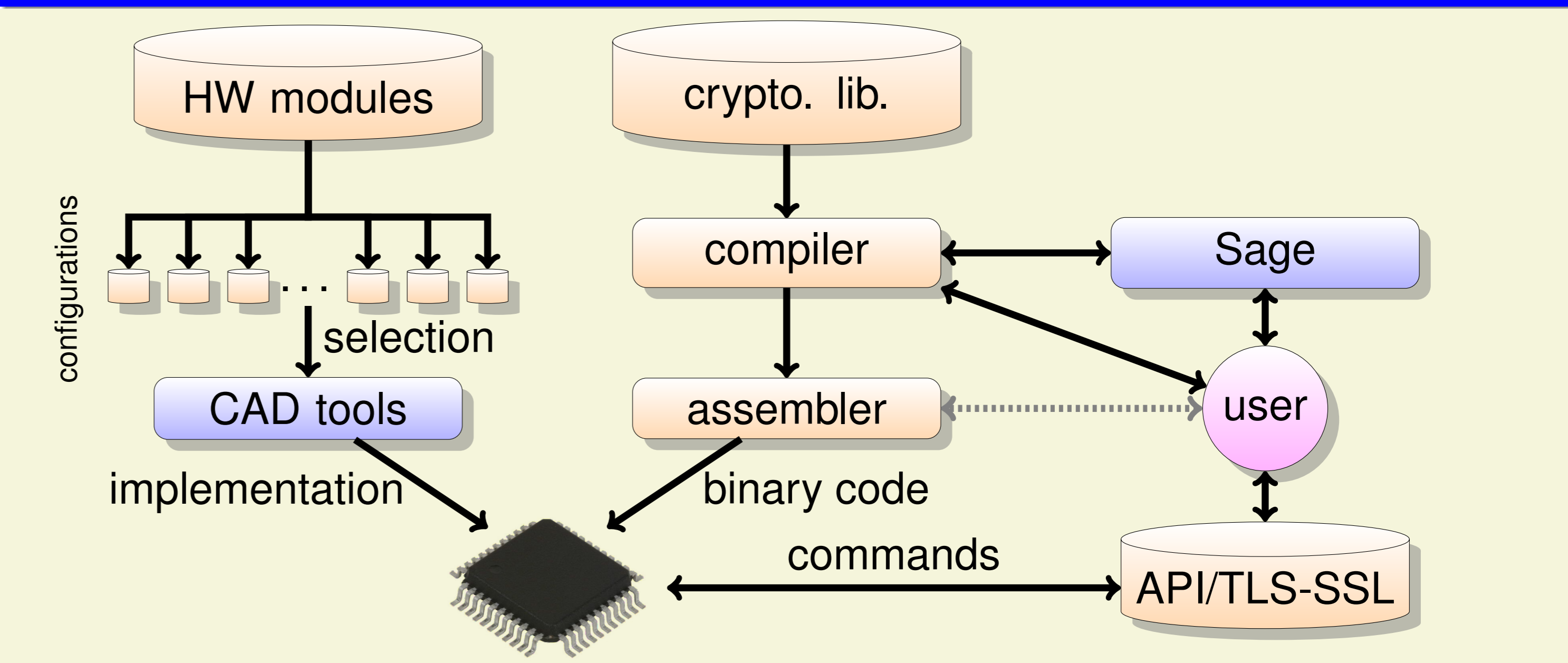
5. HAH Project Objectives

- Efficient algorithms and representations for HECC
- HECC protections against SCAs (passive and active)
- Fast, low-power and secure hardware implementations (open source hardware code and programming tools)
- Intensive security evaluation using our SCA setup

6. Developed Crypto-Processor(s) from PAVOIS ANR Project



7. Programming Tools for Our Crypto-Processor(s)



8. Implementation Results on FPGA

XC6SLX75 FPGA, GF(p), 256-bit ECC or 128-bit HECC, internal word size $w = 32$ bits

Recoding units:

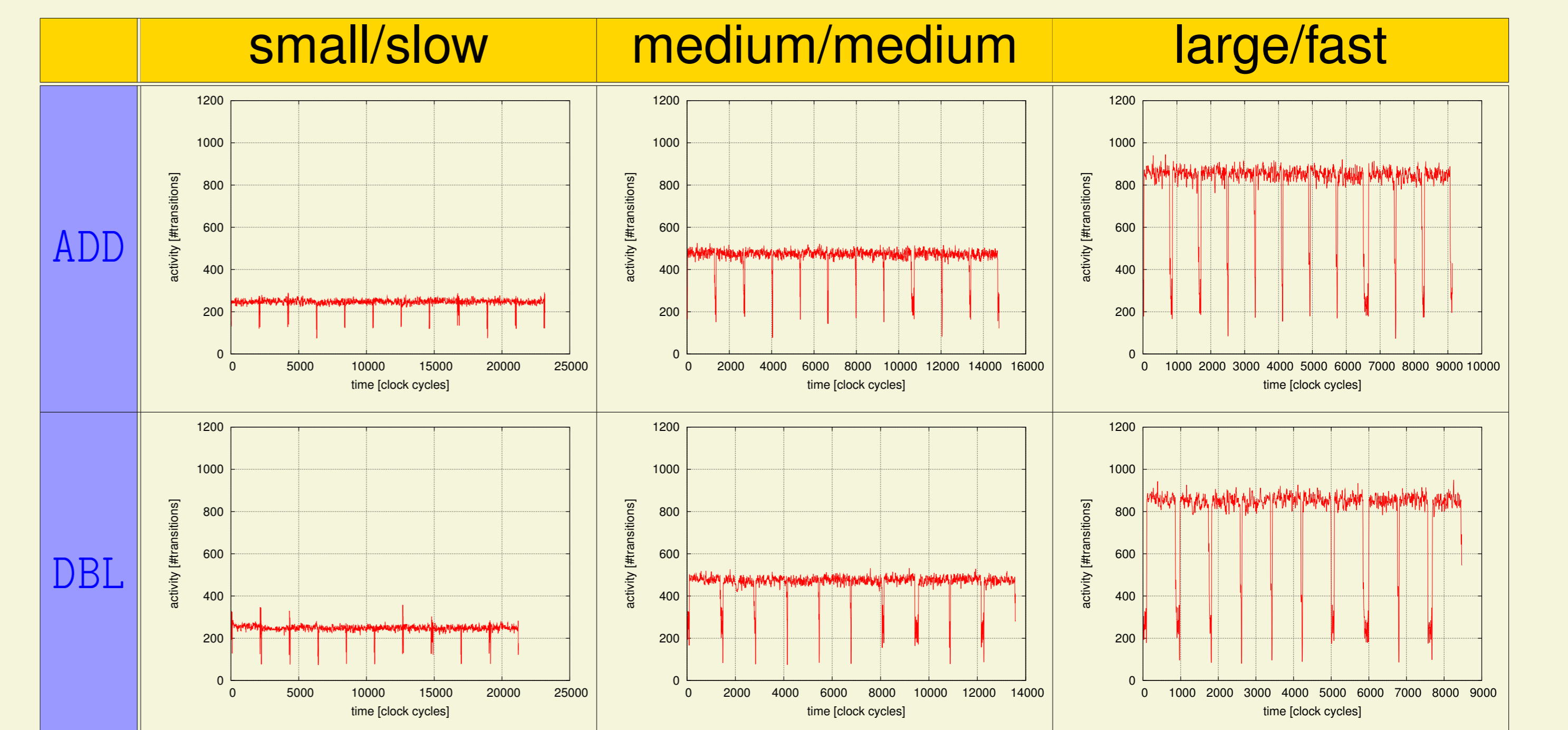
Recoding	BIN	NAF-2	NAF-3	NAF-4
area slices (FF/LUT)	565 (1321/1461)	570 (1340/1479)	571 (1344/1495)	503 (1348/1489)
freq. (MHz)	225	228	237	217

Area/speed trade-offs for ECC and HECC configurations:

	#mult.	BRAM	mult. 1 col.		mult. 2 col.		mult. 4 col.	
ECC	1	2	503 (1348/1489)	217	626 (1450/1643)	230	694 (1649/1891)	211
	2	2	689 (1744/1894)	219	754 (1948/2208)	234	931 (2345/2712)	220
	3	2	809 (2146/2245)	205	942 (2449/2704)	222	1105 (3046/3436)	222
HECC	1	2	522 (1344/1405)	228	520 (1434/1535)	217		
	2	2	634 (1746/1786)	226	689 (1926/2055)	220	area	freq.
	4	2	852 (2552/2531)	201	917 (2912/3045)	195	slices (FF/LUT)	MHz
	8	2	1347 (4145/3882)	204	1601 (4865/4928)	209		

9. Algorithms and Architecture Impacts on SCAs

Activity traces from CABA¹ simulations (after filtering) for several configurations of the field multiplier (area/speed)



¹ Cycle Accurate Bit Accurate (i.e. simulations close to real power measurements)