Hardware and Arithmetic for Hyperelliptic Curves Cryptography

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1. Elliptic Curve Cryptography (ECC)

- **Encryption**
- **Signature**
- **Key gen.**
- **etc.**

**Equation:**

\[ y^2 = x^3 + 4x + 20 \text{ over } GF(1009) \]

Points on **E**:

\[ P, Q = (x, y) \text{ or } (x, y, z) \]

Coordinates: \( x, y, z \in GF(p) \)

**GF(p), GF(2^m)**: \( t \approx 160-600 \text{ bits} \)

\[ k = (k_0, \ldots, k_{21}) \in \mathbb{N} \]

- **Scalar multiplication operation**
  
  \[ \text{for } i \text{ from } 0 \text{ to } t - 1 \text{ do} \]
  
  \[ i \text{ if } k_i = 1 \text{ then } Q = \text{ADD}(P, Q) \]

- **Point addition/doubling operations**
  
  \[ P = \text{ADD}(P, P) \]

- **Operation modulo large prime** (**GF(p)**) or irreducible polynomial (**GF(2^m)**)

2. Side Channel Attacks (SCAs)

- **Side channels:**
  - Power consumption
  - Electromagnetic radiation
  - Computation timings

- **Attacks:**
  - Simple analysis
  - Differential analysis (statistics)
  - Templates and learning

3. Protections & Counter-Measures Against SCAs

- Uniform comp. durations
- Uniform power/EM profile
- Random behavior
- Circuit reconfiguration
- Detection/correction codes
- Add noise (!)

Example: use redundant number systems

\[ R_i(x) = R_i(x) \cdot [R_i(x)]_P = [k]_P \]

Random recoding: \( \forall i \) [R_i(x)]_P = [k]_P

4. From ECC to HECC

- **Field size**
  - ADD
  - DBL

**ECC**

\( \ell \text{ bits} \)

Cost: \( 12M + 2S \)

**HECC**

\( \ell/2 \text{ bits} \)

Cost: \( 47M + 4S \)

Cost: \( 39M + 6S \)

Examples of computation expressions for projective coordinates

5. HAH Project Objectives

- Efficient algorithms and representations for HECC
- HECC protections against SCAs (passive and active)
- Fast, low-power and secure hardware implementations (open source hardware code and programming tools)
- Intensive security evaluation using our SCA setup

6. Developed Crypto-Processor(s) from PAVOIS ANR Project

- Arithmetic Units (AUs): \( +, \times, \div \text{ over } GF(p)/GF(2^m) \)
- Various key recoding methods (and dedicated units)
- Configuration: field size, internal word size, #AUs, type(AUs)
- Circuit/architecture level protections

7. Programming Tools For Our Crypto-Processor(s)

- HW modules
- Crypto. lib.
- CAD tools
- Assembler
- Implementations
- Binary code
- Commands
- User
- Sage

8. Implementation Results on FPGA

XC6SLX75 FPGA, **GF(p)**, 256-bit ECC or 128-bit HECC, internal word size \( w = 32 \) bits

**Recoding units:**

<table>
<thead>
<tr>
<th>Recoding</th>
<th>BIN</th>
<th>NAF-2</th>
<th>NAF-3</th>
<th>NAF-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>area slices (FF/LUT)</td>
<td>freq. (MHz)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>505 (134/149)</td>
<td>225</td>
<td>228</td>
<td>227</td>
<td>217</td>
</tr>
</tbody>
</table>

**Area/speed trade-offs for ECC and HECC configurations:**

<table>
<thead>
<tr>
<th>#mul.</th>
<th>BRAM</th>
<th>mult. 1 col.</th>
<th>mult. 2 col.</th>
<th>mult. 4 col.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECC</td>
<td>1</td>
<td>505 (134/149)</td>
<td>227</td>
<td>228</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>505 (134/149)</td>
<td>227</td>
<td>228</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>505 (134/149)</td>
<td>227</td>
<td>228</td>
</tr>
<tr>
<td>HECC</td>
<td>1</td>
<td>505 (134/149)</td>
<td>227</td>
<td>228</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>505 (134/149)</td>
<td>227</td>
<td>228</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>505 (134/149)</td>
<td>227</td>
<td>228</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>505 (134/149)</td>
<td>227</td>
<td>228</td>
</tr>
</tbody>
</table>

9. Algorithms and Architecture Impacts on SCAs

Activity traces from CABA\(^1\) simulations (after filtering) for several configurations of the field multiplier (area/speed)

<table>
<thead>
<tr>
<th><strong>ADD</strong></th>
<th><strong>DBL</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>small/slow</td>
<td>medium/medium</td>
</tr>
</tbody>
</table>

\(^1\) Cycle Accurate Bit Accurate (i.e. simulations close to real power measurements)

http://h-a-h.inria.fr/