



Hardware and Arithmetic for Hyperelliptic Curves Cryptography

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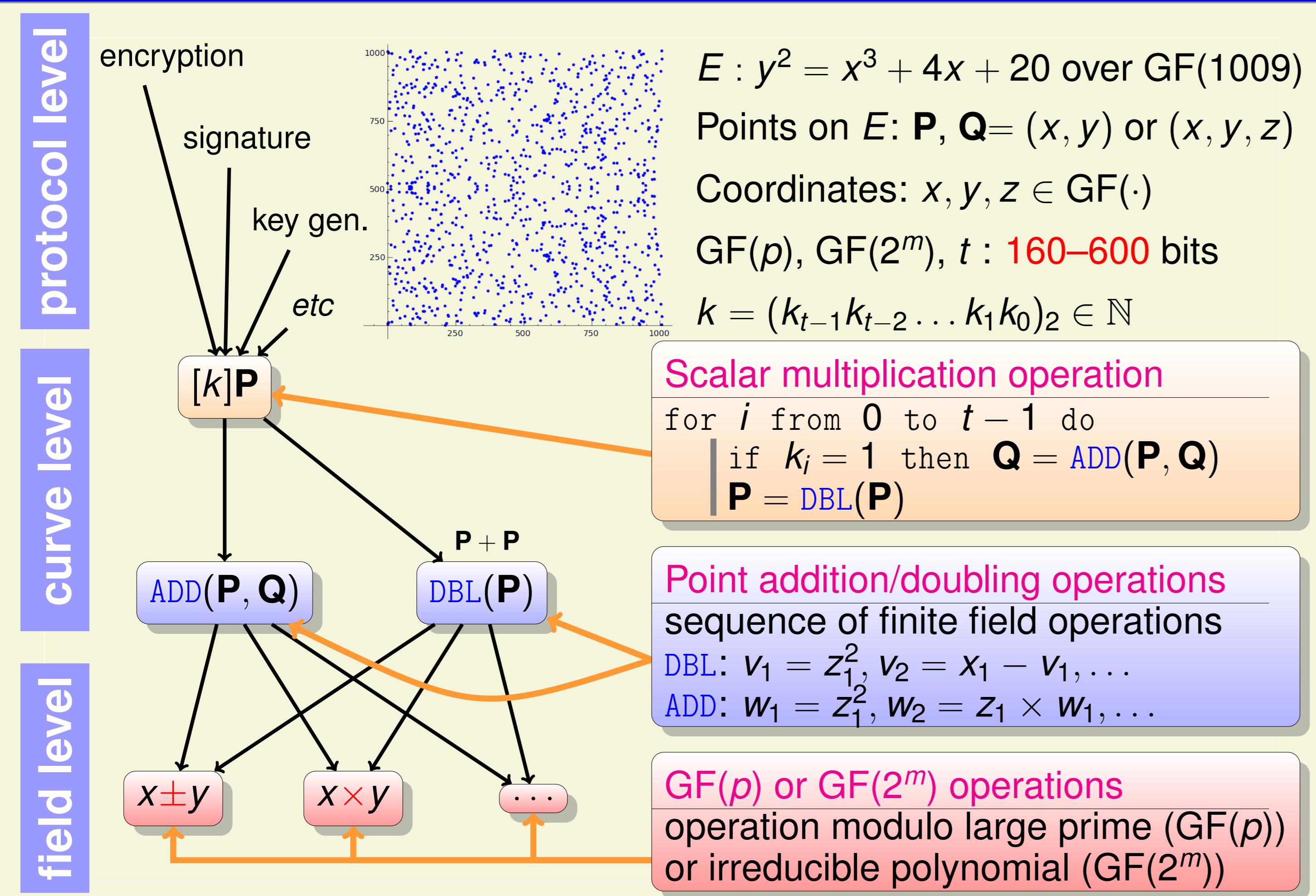
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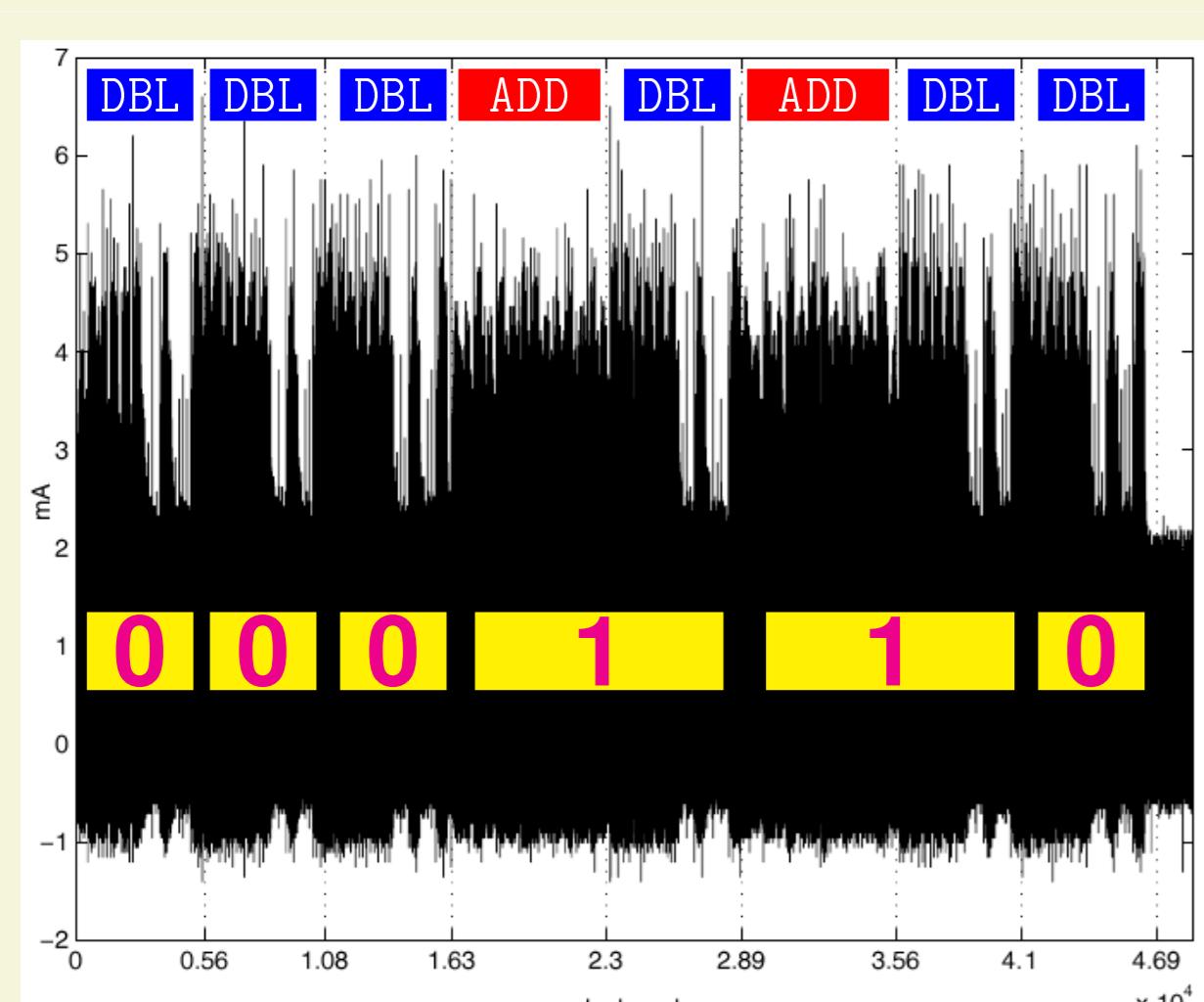
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1. Elliptic Curve Cryptography (ECC)



2. Side Channel Attacks (SCAs)



Side channels:

- Power consumption
- Electromagnetic radiation
- Computation timings

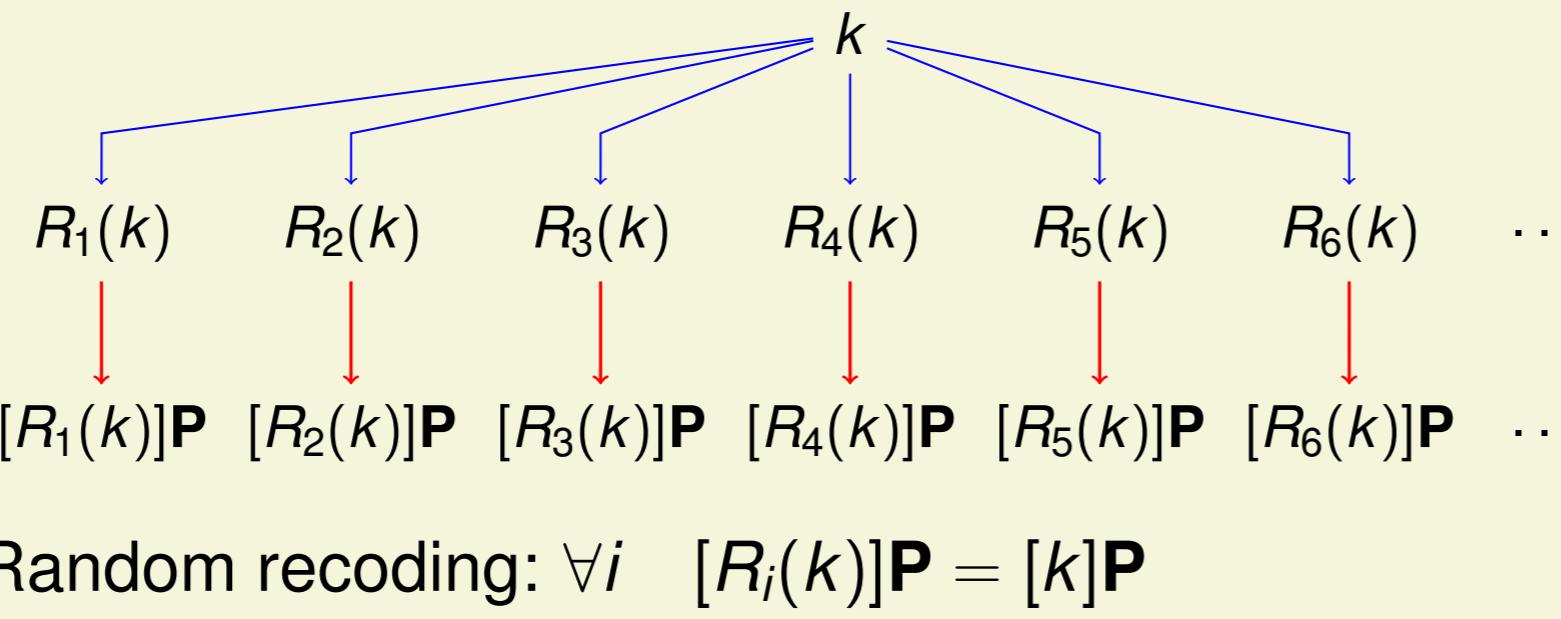
Attacks:

- Simple analysis
- Differential analysis (statistics)
- Templates and learning

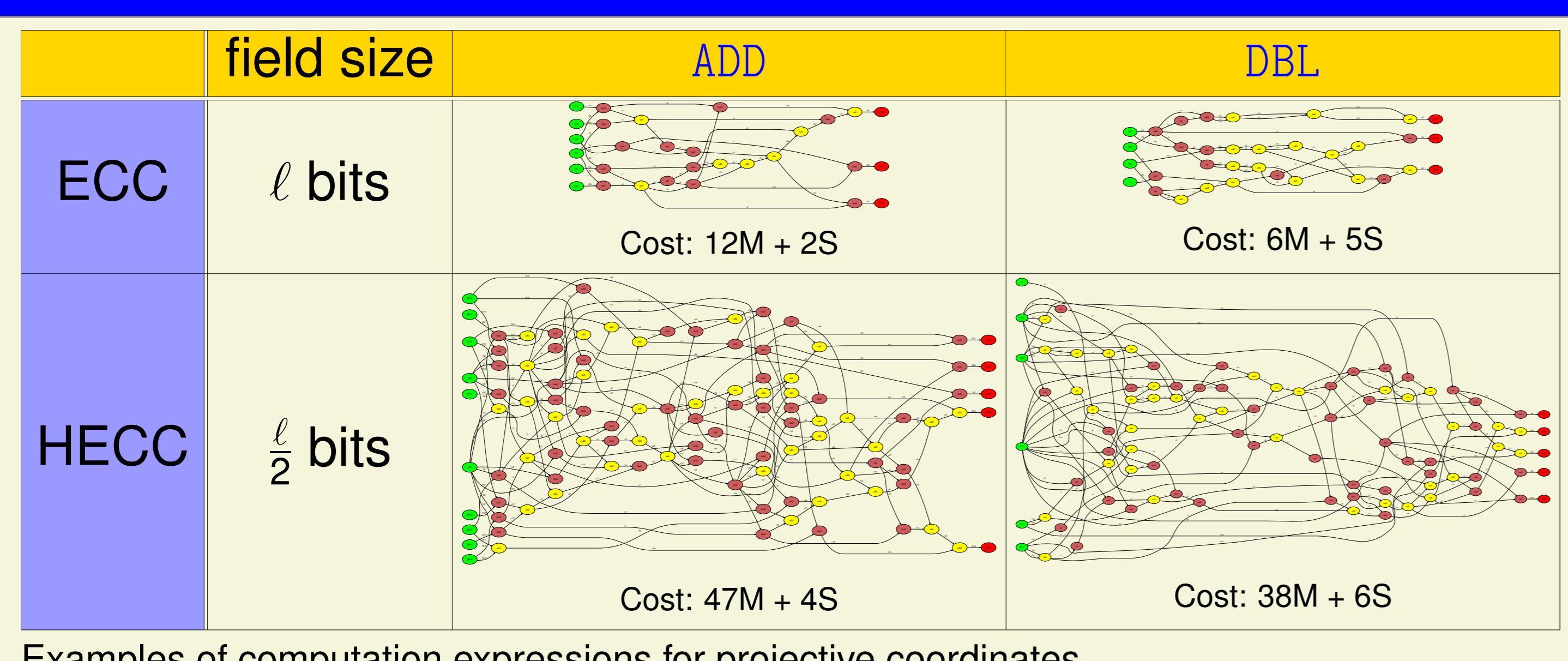
3. Protections & Counter-Measures Against SCAs

- Uniform comp. durations
- Uniform power/EM profile
- Random behavior
- Circuit reconfiguration
- detection/correction codes
- Add noise (!)

Example: use redundant number systems



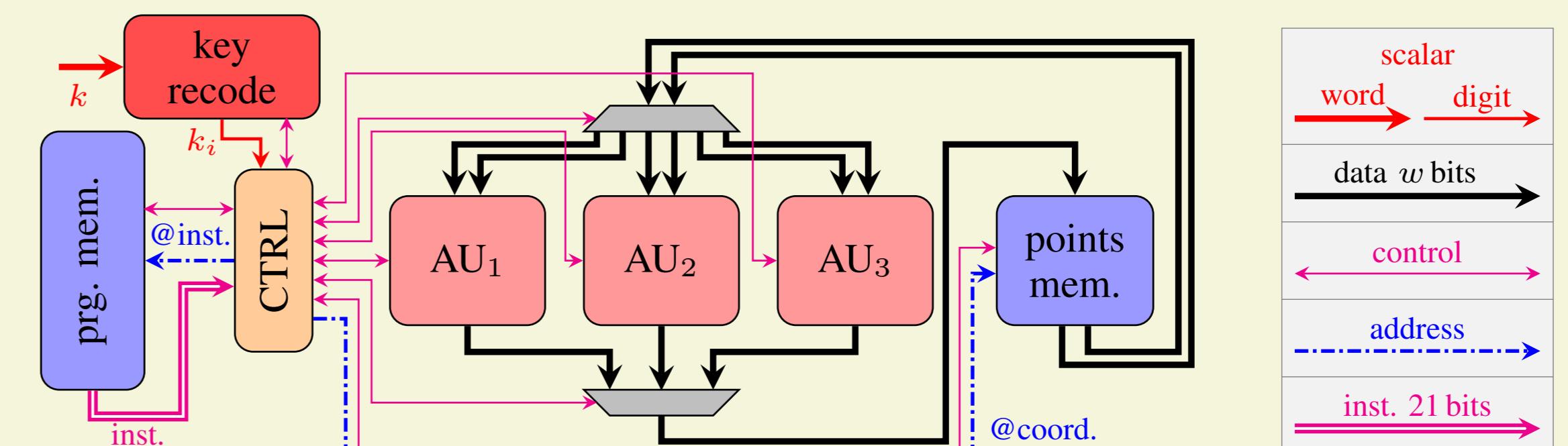
4. From ECC to HECC



5. HAH Project Objectives

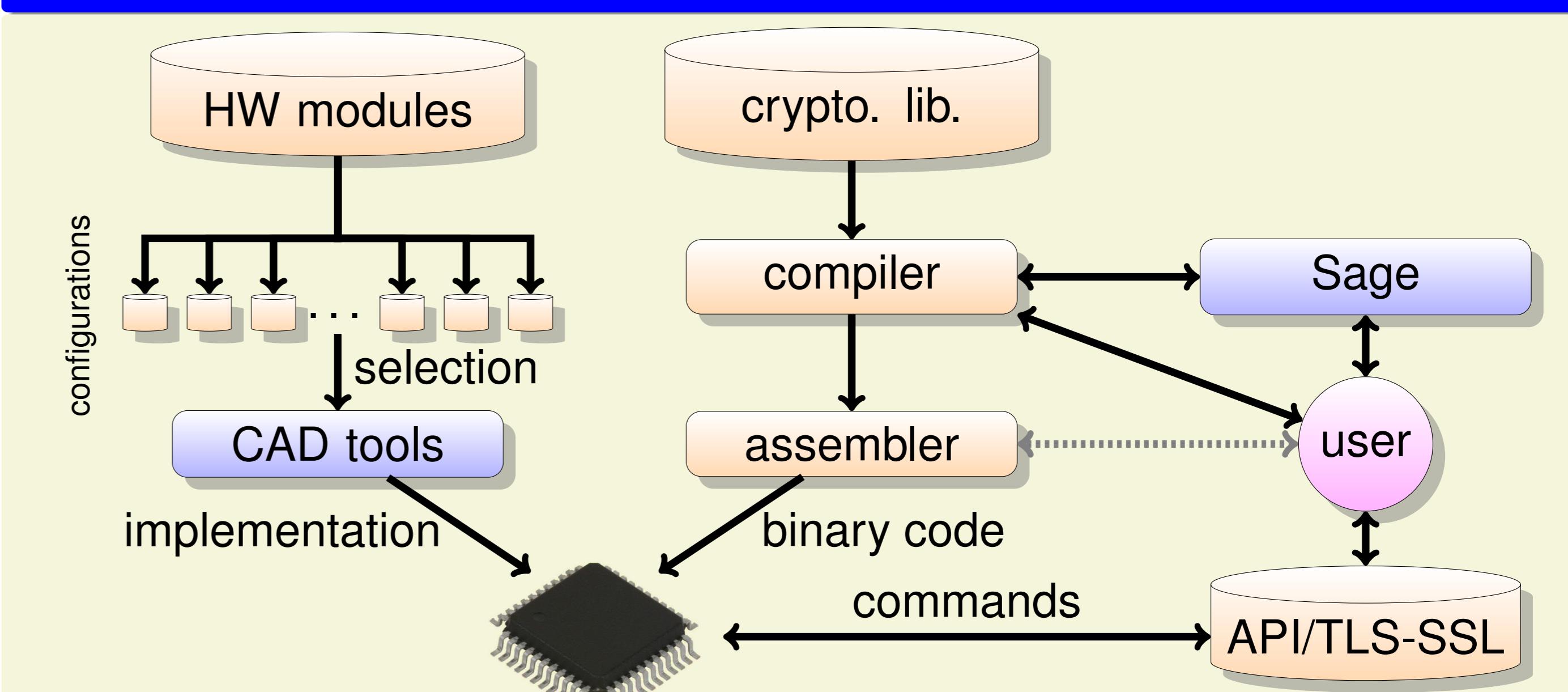
- Efficient algorithms and representations for HECC
- HECC protections against SCAs (passive and active)
- Fast, low-power and secure hardware implementations (open source hardware code and programming tools)
- Intensive security evaluation using our SCA setup

6. Developed Crypto-Processor(s) from PAVOIS ANR Project



- Arithmetic Units (AUs): \pm, \times, \div over $GF(p)/GF(2^m)$ various configurations (area vs speed, internal protection)
- Various key recoding methods (and dedicated units)
- Configuration: field size, internal word size, #AUs, type(AUs)
- Circuit/architecture level protections

7. Programming Tools for Our Crypto-Processor(s)



8. Implementation Results on FPGA

XC6SLX75 FPGA, $GF(p)$, 256-bit ECC or 128-bit HECC, internal word size $w = 32$ bits

Recoding units:

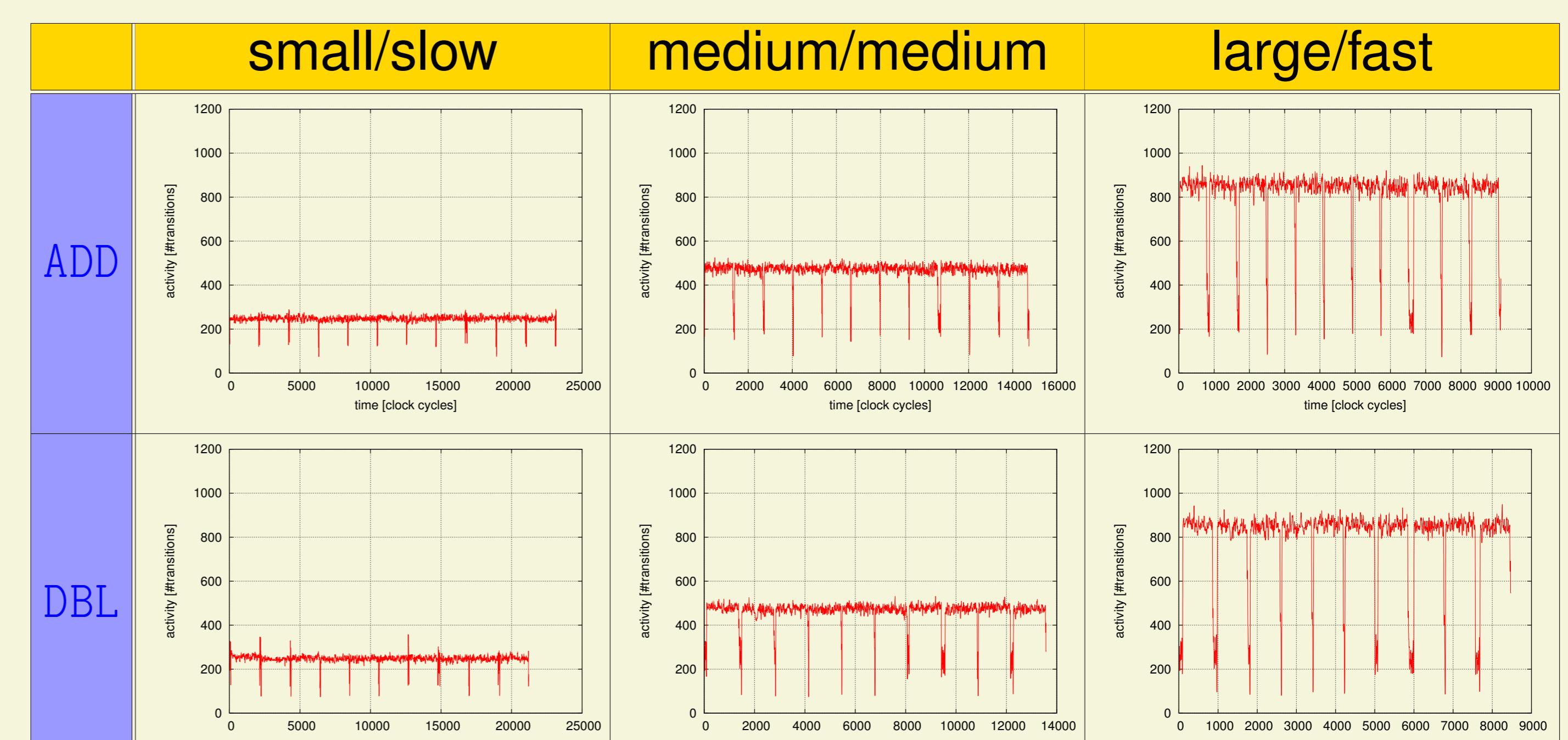
Recoding	BIN	NAF-2	NAF-3	NAF-4
area slices (FF/LUT)	565 (1321/1461)	570 (1340/1479)	571 (1344/1495)	503 (1348/1489)
freq. (MHz)	225	228	237	217

Area/speed trade-offs for ECC and HECC configurations:

	#mult. BRAM	mult. 1 col.	mult. 2 col.	mult. 4 col.
ECC	1	503 (1348/1489)	217	626 (1450/1643)
	2	689 (1744/1894)	219	754 (1948/2208)
	3	809 (2146/2245)	205	942 (2449/2704)
HECC	1	522 (1344/1405)	228	520 (1434/1535)
	2	634 (1746/1786)	226	689 (1926/2055)
	4	852 (2552/2531)	201	917 (2912/3045)
	8	1347 (4145/3882)	204	1601 (4865/4928)
		area slices (FF/LUT)	freq. MHz	

9. Algorithms and Architecture Impacts on SCAs

Activity traces from CABA¹ simulations (after filtering) for several configurations of the field multiplier (area/speed)



¹ Cycle Accurate Bit Accurate (i.e. simulations close to real power measurements)