Hardware and Arithmetic for Hyperelliptic Curves Cryptography
Gabriel Gallin, Arnaud Tisserand, Nicolas Veyrat-Charvillon

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1. Elliptic Curve Cryptography (ECC)

- **E**: $y^2 = x^3 + 4x + 20$ over $GF(1009)$
- Points on $E$: $P = (x, y)$ or $(x, y, z)$
- Coordinates: $x, y, z$ in $GF(1009)$
- $GF(p)$, $GF(2^m)$, $m = 160–600$ bits
- $K = (k_0, k_1, \ldots k_{21}) \in \mathbb{Z}$

**Scalar multiplication operation**

$P[i]$ from $U$ to $P$ is defined by $Q = AID(P, Q)$

**Point addition/doubling operations**

- Sequence of field operations: $z_i = z_1, \ldots, w_i = w_{i+1}$
- $GF(p)$ or $GF(2^m)$ operations
- Operation modulo large prime ($GF(p)$) or irreducible polynomial ($GF(2^m)$)

2. Side Channel Attacks (SCAs)

**Side channels:**
- Power consumption
- Electromagnetic radiation
- Computation timings

**Attacks:**
- Simple analysis
- Differential analysis (statistics)
- Templates and learning

3. Protections & Counter-Measures Against SCAs

- Uniform comp. durations
- Uniform power/EM profile
- Random behavior
- Circuit reconfiguration
- Detection/correction codes
- Add noise (!)

4. From ECC to HECC

**Field size**

- $ECC$: $\ell$ bits
- Cost: $12M + 2S$
- $HECC$: $\ell$ bits
- Cost: $24M + 4S$

5. HAH Project Objectives

- Efficient algorithms and representations for HECC
- HECC protections against SCAs (passive and active)
- Fast, low-power and secure hardware implementations (open source hardware code and programming tools)
- Intensive security evaluation using our SCA setup

6. Developed Crypto-Processor(s) from PAVOIS ANR Project

- Arithmetic Units (AUs): $\pm, \times, \div$ over $GF(p)/GF(2^m)$
- Various key recoding methods (and dedicated units)
- Configuration: field size, internal word size, #AUs, type(AUs)
- Circuit/architecture level protections

7. Programming Tools for Our Crypto-Processor(s)

- HW modules
- Crypto. lib.
- Assembly
- CAD tools
- Compiler
- Assembler
- Binary code
- User
- API/TLS-SSL

8. Implementation Results on FPGA

**XC6SLX75 FPGA**, $GF(p)$, 256-bit ECC or 128-bit HECC, internal word size $\omega = 32$ bits

**Recoding units:**

<table>
<thead>
<tr>
<th>Recoding</th>
<th>BIN</th>
<th>NAF-2</th>
<th>NAF-3</th>
<th>NAF-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>area slices (FF/LUT)</td>
<td>255 (132/146)</td>
<td>257 (134/147)</td>
<td>271 (134/145)</td>
<td>303 (134/149)</td>
</tr>
<tr>
<td>freq. (MHz)</td>
<td>225</td>
<td>228</td>
<td>237</td>
<td>217</td>
</tr>
</tbody>
</table>

**Area/speed trade-offs for ECC and HECC configurations:**

| $\ell$ | $\omega$ | $R[|K|]P - |K|P$ | $R[|K|]P$ | $R[|K|]P$ |
|-------|---------|----------------|----------|----------|
| ECC | 1 | 2 | 3 | 4 | 5 |
| HECC | 1 | 2 | 3 | 4 | 5 |
| freq. (MHz) | 225 | 228 | 237 | 217 |

**Examples of computation expressions for projective coordinates**

- $R[|K|]P - |K|P$
- $R[|K|]P$
- $R[|K|]P$

9. Algorithms and Architecture Impacts on SCAs

**Activity traces from CABA simulations** (after filtering) for several configurations of the field multiplier (area/speed)

<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>ECC</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>HECC</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
</tbody>
</table>

**Example configurations:**

- small/slow
- medium/medium
- large/fast

**Notes:**

- $^1$ Cycle Accurate Bit Accurate (i.e., simulations close to real power measurements)

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**References:**

- Gabriel Gallin, Arnaud Tisserand & Nicolas Veyrat-Charvillon
- Hardware and Arithmetic for Hyperelliptic Curves Cryptography
- HAH Project, IRISA–IRMAR