Orcc's Compa-Backend demonstration

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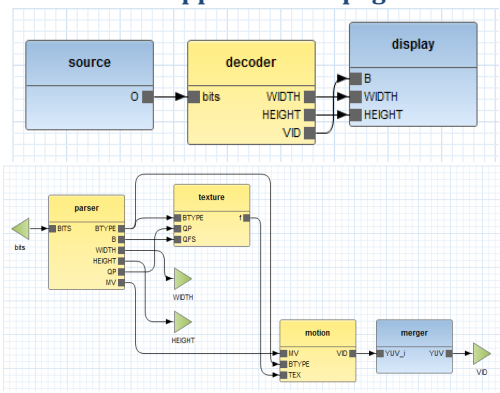
Abstract

This work presents the implementation of an MPEG-4 part 2 video decoder, from its high-level description to the system implementation, using the Orcc's Compa-Backend. The high-level description consists of a data flow model (a network of actors) and the functional description in language CAL for each actor.
The target HW architecture is a shared-memory multiprocessor embedded system.

Introduction

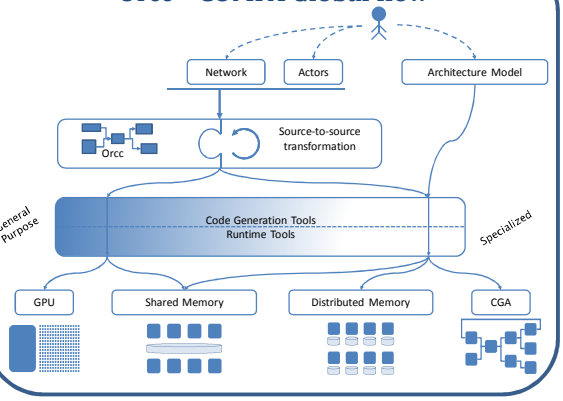
More complex communication and video standards and more powerful and heterogeneous multi-core hardware architectures, make the design of modern electronic systems an arduous process. New tools such as the Open RVC-CAL Compiler (ORCC) emerge to help overcome the challenges of the new designs.
Our goal in this work is to validate a new extension to the Orcc framework for multiprocessors embedded systems.

Use case application: Mpeg4 Part 2



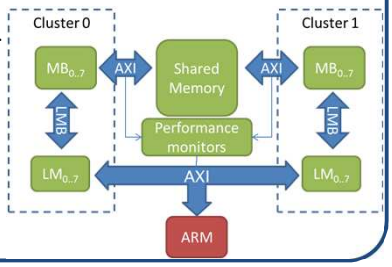
15 actors + Source & Display; 32 token channels

Orcc – COMPA Global flow

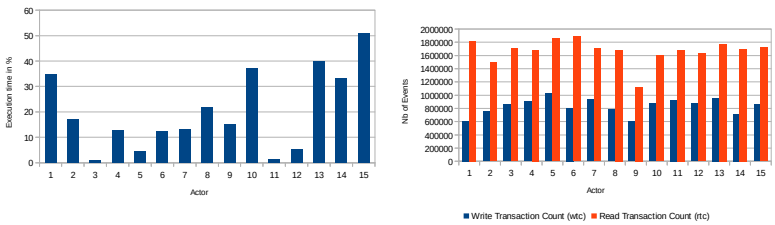


Target HW architecture

- Implemented on the Xilinx's ZC706 board.
- Up to 16 Microblazes as slave processors.
- 1 ARM as the master processor.
- Shared memory for inter-slaves data exchanges.
- Master access to local memories for control communications.



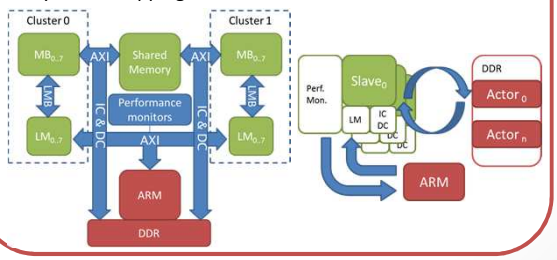
Output metrics



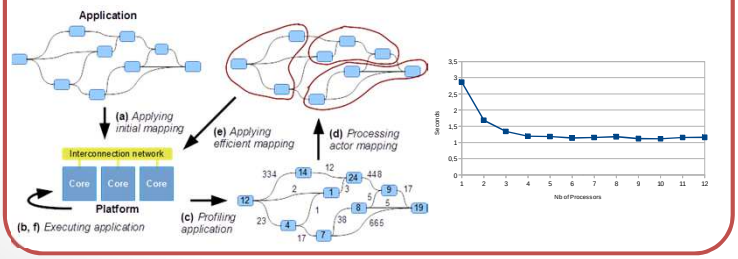
Conclusions & Perspectives

Validated work :
✓ Version with application in local memories.

Work in progress :
❑ Version with application in external memory.
❑ Dynamic mapping based on metrics.



Other mappings using a load balancing strategy



Related work

- *Communication-model based Embedded Mapping of Dataflow Actors on Heterogeneous MPSoC. DASIP-14 Session #6* (next Friday)
- http://www.compa-project.org/
- http://orcc.sourceforge.net/