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CLOCK JITTER EFFECT ON SWITCHED-CAPACITOR FILTER DESIGN

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This paper proposes the study of clock jitter effect on high-Q switched-capacitor filter behavior. A command circuit made up by a ring voltage controlled oscillator (VCO) with XOR gates is used to generate the command signals. According to the correlation of these signals the jitter effect on the signal constellation has been studied. A good agreement between measured and simulation results has been achieved which validate our design methodology.

Keywords: Jitter; phase noise; switched-capacitor filter.

1. Introduction

In modern radio-communication systems, passive filters such as surface acoustic wave (SAW) are widely used. These filters present high quality factors. However, they are off-chip, have high insertion losses, and are not easily tunable over a broad range of frequencies; furthermore, their manufacturing costs are prohibitive. Among the integrated filters, the switched-capacitor filters have been widely used for the design of stable, accurate and high-Q filters for operating frequencies in the megahertz range [1–4]. These filters offer interesting advantages in particular a very high selectivity associated with the possibility of adjustment of the center frequency by a clock signal. This characteristic is more significant for integrated circuits applications, for which the tuning of the center frequency by a clock signal permits either to compensate the dispersions due to the technology used, or to filter various channels with the same filter. Nevertheless, the performances of these filters are strongly related to the possibility to generate stable clock signals. For high frequency applications, time jitter becomes more important and can significantly degrade the performances of the filter [5]. Consequently, a special attention should be given to

study the effects of time jitter in order to predict the possible degradations on the behavior of these filters.

2. Circuit Description

Figure 1 shows the switched-capacitor filter topology. The switches consist of NMOS transistors sequentially controlled in ON/OFF states. These transistors present a Ron resistance of 30 Ω and a drain-source capacitance of 0.06 pF, to give an optimal dynamic range [6]. The input NMOS transistor, biased in the triode regime, is here introduced to implement the filter tuning.

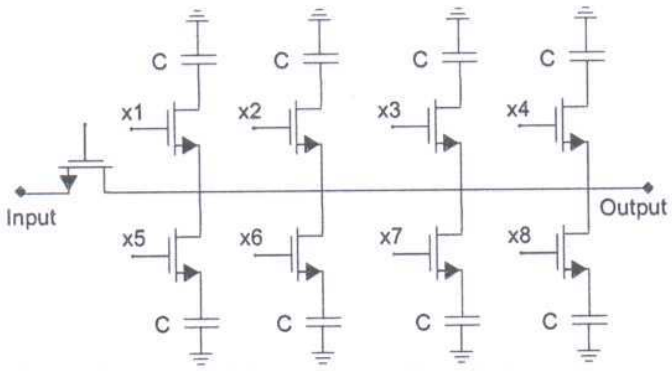

Fig. 1. Architecture of the switched-capacitor filter.

A significant limitation of this filter is related to the design of the command circuit of the switches which commonly uses low frequency shift registers. Recently a solution based on a ring voltage controlled oscillator associated with 'XOR' gates (Fig. 2) has been proposed [6]. This solution provides the possibility of tuning within a broad frequency band, sweeping different channels with high Q-factors.

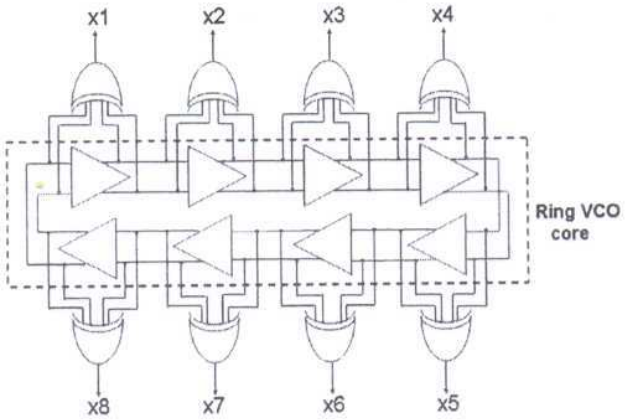

Fig. 2. Architecture of the command circuit consisting of ring VCO with 'XOR' gates.

However, if ring VCOs provide an easy integration on-chip, they are characterized by a significant unwanted phase noise compared to LC tank ones. Indeed, this undesired phase noise produces a time jitter which introduces a random variation of the instantaneous frequency. This can directly affect the command signals and consequently degrade the filter performance.

3. Jitter Effect on Filter Behavior

The description details with trade-offs design of the proposed command circuit have been presented in [6]. Actually, during the ring VCO design, a special attention was given to its temporal waveform signals [7] in order to limit the jitter and hence the spectral power of phase noise at roughly -101.46 dBc/Hz at 1-MHz offset frequency from the carrier frequency. With this phase noise value, it is possible to calculate the jitter of the ring VCO. It appears evident that this jitter must be lower than the command impulse duration which is equal to 250 ps, with 900 MHz center frequency and eight cells.

Since the phase noise at 1-MHz offset from the carrier frequency is in the $1/f^2$ region, the jitter is generated by the conversion of a white Gaussian cyclostationary process. Thus, the cycle-to-cycle jitter σ_{CTC} is defined by the following expression [7]:

$$\sigma_{CTC} = \sqrt{\frac{1}{F}} \cdot \frac{\Delta F}{F} \cdot 10^{-L\{\Delta F\}/20} \tag{1}$$

where, F, ΔF and $L\{\Delta F\}$ are respectively the oscillation frequency, offset frequency from the carrier and noise power spectral density. Then, the calculated cycle-to-cycle jitter is equal to 0.3 ps. Such a value is insignificant compared to the impulse duration: 250 ps, with 900 MHz center frequency.

To predict the possible degradations which can be generated by the filter, a special attention was given to study the jitter effect when its input signal is changed to a digitally modulating signal of type π/4–DQPSK (Differential Quadriphase Shift Keying) digital modulation. According to the correlation of these signals the effect on the signal constellation and consequently the EVM (Error Vector Magnitude) is quite different.

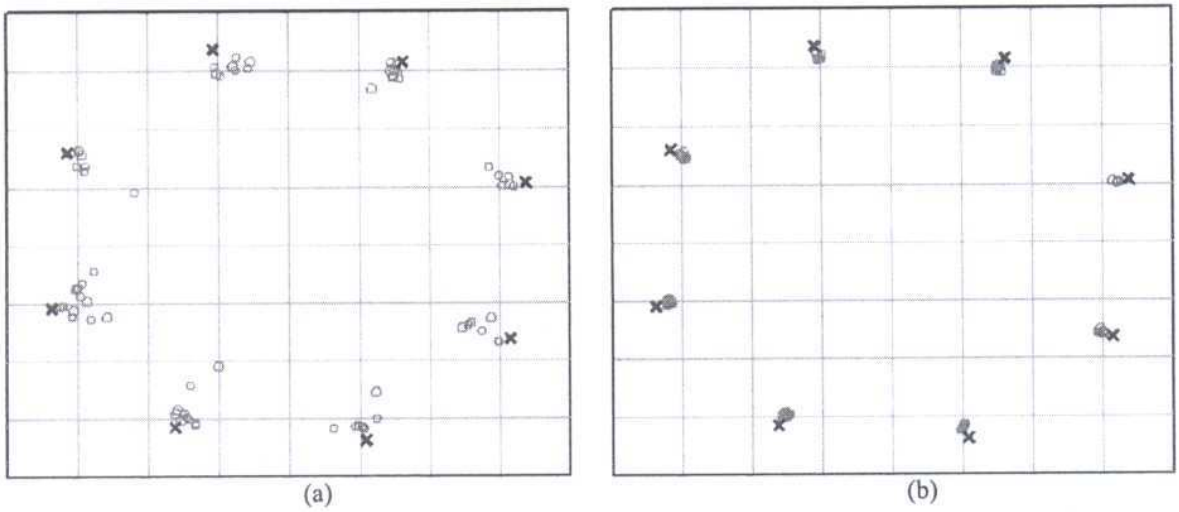

Fig. 3. Constellation diagrams of input and output circuit with, (a) uncorrelated command signals, and (b) correlated command signals.

Figure 3 shows the constellations obtained with 900 MHz center frequency, using a π/4–DQPSK digital modulation with a symbol rate equal to 24.3 KHz, by applying the same obtained phase noise value on command signals. Figure 3(a) shows the obtained output constellation compared to the ideal π/4–DQPSK constellation. In this case, the command signals are uncorrelated by using independent switching command sources. Thus, they can overlap; this phenomenon produces a weakness of the filtering function which results in a significant degradation of the filter output constellation. This can be

observed in the Fig. 3(a) which shows considerable shifts in the position of constellation points. However, when the command signals are generated by one single source by using the previous architecture (ring VCO), described above, the produced jitter is applied in a correlated manner on command signals without significant degradation of the output signal constellation (Fig. 3(b)). Since the simulation has been performed with identical average delays for all ring VCO cells, a fixed displacement of points can be observed in the result constellation of Fig. 3(b).

Expressed in percentage (%), the EVM is a parameter which makes it possible to quantify the effect of the additive noise on the deformation of the transmitted signal constellation.

Table 1. Normalized EVM Values.

EVM (RMS) correlated noise	EVM (RMS) uncorrelated noise
1.314%	9.526%

Table 1 shows that the RMS value of the EVM does not exceed 2% if the command signals are correlated. While this value is close to 10% in the case of uncorrelated command impulses. From this result, it appears important to have only one source that provides all commands signals, which justifies our choice of this ring VCO to command the filter.

4. Experimental Results

To validate the proposed approach, a test chip composed by a switched-capacitor filter and its command circuit (ring VCO with XOR gates) was fabricated using standard 0.35 μm CMOS process. Measurements based on constellation and EVM have been made.

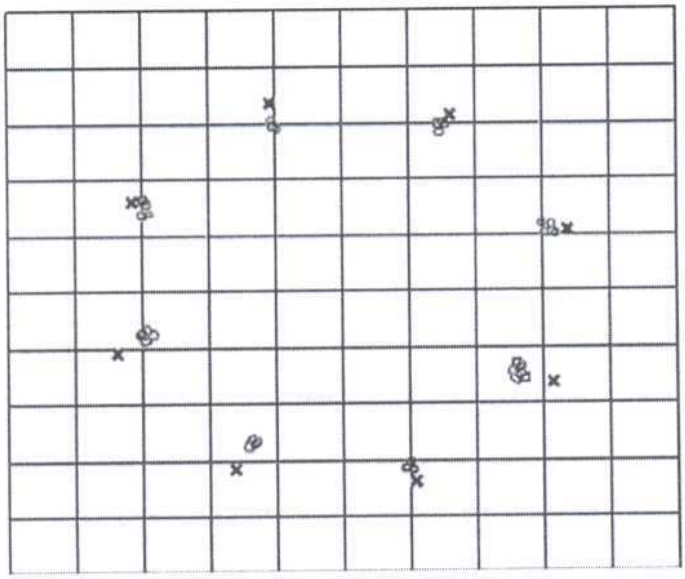

Fig. 4. Measured constellation at output filter.

Figure 4 shows the constellation obtained with 900 MHz center frequency using a π/4–DQPSK modulation. A slight displacement in the position points can be shown in the

measured constellation diagram compared to simulation (Fig. 3(b)). This may be due to mismatch in the VCO delay cells and the XOR gates, since the simulation in Fig. 3(b). has been performed with identical average delays for all cells. The RMS value of the EVM is equal to 2.192 % which is slightly higher than the simulation results (1.314%).

5. Conclusion

The jitter effect on high-Q switched-capacitor filter has been studied. The degradations produced by this jitter have been demonstrated firstly by simulation, and after with measurements by using a $\pi/4$–DQPSK digital modulation. A good agreement between measured and simulation results has been achieved which validate our choice to use the ring VCO to command the filter. This study shows the importance to take into account the jitter effect in the design of switched-capacitor circuits.

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