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Correct and Efficient Work-Stealing for Weak Memory Models

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Abstract
Chase and Lev’s concurrent deque is a key data structure in shared-memory parallel programming and plays an essential role in work-stealing schedulers. We provide the first correctness proof of an optimized implementation of Chase and Lev’s deque on top of the POWER and ARM architectures; these provide very relaxed memory models, which we exploit to improve performance but considerably complicate the reasoning. We also study an optimized x86 and a portable C11 implementation, conducting systematic experiments to evaluate the impact of memory barrier optimizations. Our results demonstrate the benefits of hand tuning the deque code when running on top of relaxed memory models.

Categories and Subject Descriptors D.1.3 [Programming Techniques]: Concurrent Programming; E.1 [Data Structures]: Lists, stacks, and queues

Keywords: lock-free algorithm, work-stealing, relaxed memory model, proof

1. Introduction
Multicore POWER and ARM architectures are standard targets for server, consumer electronics, and embedded control applications. The difficulties of parallel programming are exacerbated by the relaxed memory model implemented by these architectures, which allow the processors to perform a wide range of optimizations, including thread-local reordering and non-atomic store propagation.

The safety-critical nature of many embedded applications call for solid foundations for parallel programming. This paper shows that a high degree of confidence can be achieved for highly optimized, real-world, concurrent algorithms, running on top of weak memory models. A good test-case is provided by the runtime scheduler of a task library. We thus focus on the Chase and Lev’s concurrent doubly-ended queue (deque) [3], the cornerstone of most work-stealing schedulers. Until now, no rigorous correctness proof has been provided for implementations of this algorithm running on top of a relaxed memory model. Furthermore, while work-stealing is widely used on the x86 architecture (an evaluation under a restrictive hypothesis of idempotence of the workload can be found in [10]), few experiments target weaker memory models.

Our first contribution is a correctness proof of this fundamental concurrent data structure running on top of a relaxed memory model. We provide a hand-tuned implementation of the Chase and Lev’s deque for the ARM architectures, and prove its correctness against the memory semantics defined in [12] and [7]. Our second contribution is a systematic study of the performance of several implementations of Chase–Lev on relaxed hardware. In detail, we compare our optimized ARM implementation against a standard implementation for the x86 architecture and two portable variants expressed in C11; a reference sequentially consistent translation of the algorithm, and an aggressively optimized version making full use of the release–acquire and relaxed semantics offered by C11 low-level atomics. These implementations of the Chase–Lev deque are evaluated in the context of a work-stealing scheduler. We consider diverse worker/thief configurations, including a synthetic benchmark with two different workloads and standard task-parallel kernels. Our experiments demonstrate the impact of the memory barrier optimization on the throughput of our work-stealing runtime. We also comment on how the ARM correctness proof can be tailored to these alternative implementations. As a side effect, we highlight that our optimized ARM implementation cannot be expressed using C11 low-level atomics, which invariably end up inserting one redundant synchronization instruction.

2. Chase–Lev deque
User-space runtime schedulers offer an excellent playground for studying low-level high-performance code. We focus on randomized work-stealing: it was originally designed as the scheduler of the Cilk language for shared-memory multiprocessors [4], but thanks to its merits [2] it has been adopted in a number of parallel libraries and parallel programming environments, including the Intel TBB and compiler suite. Work-stealing variants have also been proposed for distributed clusters [5] and heterogeneous platforms [1]. The scheduling strategy is intuitive:
• Each processor uses a dynamic array as a deque holding tasks ready to be scheduled.
• Each processor manages its own deque as a stack. It may only push and pop tasks from the bottom of its own deque.
• Other processors may not push or pop from that deque; instead, they steal tasks from the top when their own deque is empty. In most implementations, the stolen deque is selected at random.
• Initially, one processor starts with the “root” task of the parallel program in its deque, and all other dequees are empty.

The state-of-the-art algorithm for the work-stealing deque is Chase and Lev’s lock-free deque [3]. It uses an array with automatic, asynchronous growth. Assuming sequentially consistent memory, it involves only one atomic compare-and-swap (CAS) per steal, no CAS on push, and no CAS on take except when the deque has exactly only one element left.

We implemented and tested four versions of the concurrent deque algorithm, with different barrier configurations: (1) a sequentially consistent version, written with C11 seq. cst atomics, following the original description in [3]; (2) an optimized version, which takes full advantage of the C11 relaxed memory model, reported in Figure 1; (3) a native version for ARMv7, reported in Figure 2,
In the code of Figure 1 the atomic_ and memory_order_ prefixes have been elided for clarity. The ARMv7 pseudo-code of Figure 2 uses the keywords R and W to denote reads and writes to shared variables, and atomic indicates a block that will be executed atomically, implemented via LL/SC instructions. The x86 version is based on prior work [10] and only requires a single mfence memory barrier in take, in place of the call to thread_fence in the C11 code.

2.1 Notions of correctness

The expected behavior of the work-stealing deque is intuitive: tasks pushed into the deque are then either taken in reverse order by the same thread, or stolen by another thread. We say that an implementation pushed into the deque are then either taken in reverse order by the same thread, or stolen by another thread. We say that an implementation is valid if it satisfies four criteria, formalized and proven correct for our ARMv7 optimized code in Section 4:

1. tasks are taken in reverse order;
2. only tasks pushed are taken or stolen (well-defined reads);
3. a task pushed into a deque cannot be taken or stolen more than once (uniqueness);
4. given a finite number of push operations, all pushed values will eventually be either taken or stolen exactly once, if enough take and steal operations are attempted (existence).

These criteria hold because of the following assumptions and properties of the Chase–Lev algorithm:

- For any given deque, push and pop operations execute on a single thread. Concurrency can only occur between one execution of push or take in the owner thread, and one or more executions of steal in different threads.
- Newly pushed tasks are made visible to take and steal by the increment to bottom in push. As we shall see in Section 4, our ARMv7 implementation enforces this by placing a sync barrier before the update of bottom, guaranteeing that the pushed element cannot be stolen before bottom is updated.
- Taken tasks are reserved first by updating bottom; again, in our ARMv7 code, the sync barrier placed after the update to bottom will ensure that it will not be concurrently stolen.
- Stolen tasks are reserved by updating top. The only situation where steal and take contend for the same task is when the deque has a single element left; this particular conflict is resolved through the CAS instructions in both take and steal. This scenario allowed Chase and Lev to make the CAS in take conditional upon the size of the deque being 1. The correctness of this optimization on a relaxed memory model depends on the presence of the two full barriers in take and steal, to ensure that at least one of the participants will have a consistent view of the size of the deque. Having just one take or steal seeing a consistent view of the size of the deque is enough: if it is take, that will force a CAS to be performed; if it is steal, the index reservation will ensure an empty return value.
- Finally, stolen tasks are protected from being concurrently stolen multiple times by the monotonic CAS update to top in steal. This CAS orders steal operations and makes them mutually exclusive. At the same time, steal operations that abort due to a failed CAS do not change the state of the deque.

2.2 Comparison of the C11 and ARM implementations

Our C11 implementation in Figure 1 is optimal in the sense that no C11 synchronization can be removed without breaking the algorithm. However, if low-level atomics are compiled using the mapping of McKenney and Silvera [9] on ARMv7/POWER or the mapping of Tehrekev [14] on x86, the generated code contains more barriers than the hand-optimized native versions on both x86 and ARMv7. We show in Section 5 that this happens because of the need for sec-ext atomics to simulate ARMv7/POWER cumulative semantics. Concretely, on ARMv7, an extra dmb instruction is inserted before each CAS operation [11], compared to the native version where a relaxed CAS—coherent and atomic only—is sufficient. On x86, an mfence instruction is added between the two reads in steal. The fully sequentially consistent C11 implementation inserts many more redundant barriers [11].

3. The memory model of ARMv7

The memory model of the ARMv7 architecture is based closely on the POWER architecture, allowing a wide range of relaxed behaviors to be observable to the programmer:

1. The hardware threads can each perform reads and writes out-of-order, or even speculatively. Basically any local reordering is allowed unless there is a data/control dependence or synchronization instruction preventing it.
2. The memory system does not guarantee that a write becomes visible to all other hardware threads at the same time point. Writes performed by one thread are propagated to (and become visible from) any other thread in an arbitrary order, unless synchronization instructions are used.
3. A dmb barrier instruction guarantees that all the writes which have been observed by the thread issuing the barrier instruction are propagated to all the other threads before the thread can continue. Observed writes include all writes previously issued by the thread itself, as well as any write propagated to it from another thread prior to the barrier. This semantics of barrier instructions is referred to as cumulative.

We build on the axiomatic formalization of POWER and ARMv7 memory model by Mador-Haim et al. [7], which has been proved equivalent to the operational semantics of Sarkar et al. [12]. A gentle introduction can be found in [8].

Axiomatic execution witnesses capture abstract memory events associated with memory-related instructions and internal transitions of the model. Unlike in stronger models such as x86, each memory access is represented at run-time by two distinct events: an issuing event—called sat for reads and int for writes—even followed by a commit event when the speculative state of the instruction is resolved. Once a write instruction is committed, events that propagate it to other threads can be observed—propagation to thread A is denoted pp_A. All the relations part of an execution witness are listed in Table 1.

The core of the axiomatic model builds on the evord relation, modeling the happens-before order between events. This satisfies the fundamental property:

\[ \text{evord} \to after \to before \to commit \to mem \to local \]

and must be acyclic for an execution to be consistent.

We assume that the atomic sections, used to represent CAS-like behaviors, are executed atomically and obey a total order. We model them either as a single instance of a read instruction (failed CAS) or an atomic read–write pair of instruction instances (successful CAS). The atomicity of these accesses is captured by the patomic relation. We do not assume any other property on these atomic sections (e.g., cumulativity). In practice, atomic sections can be implemented with LL/SC instructions.

We use several notation shortcuts. We refer to the deque global variables top, bottom, and array as t, b, and a. Elements of the buffer are written \( x_i \), where \( i \) is the virtual index in natural numbers.
The proof builds on a precise analysis of all the possible execution witnesses of arbitrary invocations of the algorithm. We recall that an execution witness, as defined by the ARMv7 axiomatic model, is a graph capturing all memory events occurring during an execution (vertices), as well as the relations that link them (edges). Individual lemmas strive to narrow down the set of possible execution witnesses, based on properties of the algorithm and the architecture. To that end, we pinpoint specific subgraphs of an execution witness (hereafter, execution graphs) that cannot occur together in the same consistent execution witness. We then show that all incorrect executions, such as those containing two instances of steal reading the same value added by a single instance of push, cannot have consistent execution witnesses and, as such, cannot happen.

The proof is structured as follows. In 4.1 we provide basic technical definitions and properties of the memory model, which are used throughout the proof. In 4.2 we describe all the possible execution graphs for each of the three operations (push, take and steal), following the control flow of the ARMv7 code in Figure 2. In 4.3 we show how the succession of dynamic arrays built by resizing can be abstracted as a single sequence of unique abstract values independent of resize operations, with strong coherence and consistency properties. Corollary 2 establishes Criterion 2 (well-defined reads). In 4.4 we build on the previous abstraction to prove Theorem 1, pertaining to the uniqueness of elements taken and stolen, which corresponds to Criterion 3 (uniqueness). Finally, in 4.5, we rely on all previous results to prove Theorem 2 establishing Criterion 4 (existence): the existence of matching take or steal operations for every pushed element, under the appropriate hypotheses.

4.1 Preliminary properties

Before delving into the details of the proof itself, we introduce some support definitions and related properties.
read of value α from location l ( ... stands for any value)
write of value α to location l ( ... stands for any value)
memory barrier (usually implied by \textit{sync})

\textit{sync}

\textit{sat}(X)

\textit{init}(X)

\textit{com}(X)

\textit{pp}_A(X)

\textit{po}

\textit{p-o-atom}

\textit{po-loc}

\textit{po-sync}

\textit{after}

\textit{before}

\textit{comm}

\textit{local}

\textit{sword}

\textit{event happens-before order} (usually typeset as \(\rightarrow\))

\textit{atomic operation in program order}

\textit{write-to-read propagation}

\textit{program order}

\textit{intuitively}

\textit{Lemma 1.}

on ARMv7, \textit{xmc} corresponds to a \texttt{dmb} instruction while \textit{Ctr} corresponds to a dependent conditional branch followed by an \texttt{ish} instruction.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|}
\hline
\textbf{Table 1. Summary of relations used in the ARMv7 axiomatic model} & \\
\hline
For convenience, we define the \textit{po-loc} relation, which relates local (same-thread) accesses to the same memory location; \textit{po-sync} implies an instruction-level communication edge \(\rightarrow\), \(\rightarrow\) or \(\rightarrow\). In particular, \textit{po-sync} implies \(\rightarrow\) between two writes. & \\
\hline
\textit{Lemma 1. The following properties involving \textit{po-sync} apply:} & \\
\hline
\textit{R}_x \textit{po-sync} \textit{R}_y \iff \textit{sat}(\textit{R}_x) \rightarrow \textit{sat}(\textit{R}_y) \iff \textit{com}(\textit{R}_x) \rightarrow \textit{com}(\textit{R}_y) & \\
\hline
\textit{Proof. In the case the of an address or control dependence, the result is an immediate consequence of the definition of \textit{intra-instruction} and \textit{local} orders. It remains to be shown that the result holds for \textit{po-sync} -- a dependent conditional branch instruction, \textit{ctrl}, followed by an \textit{isync} barrier. Suppose \textit{R}_x \textit{po-sync} \textit{R}_y. Then we have: \textit{sat}(\textit{R}_x) \rightarrow \textit{com}(\textit{R}_x) \rightarrow \textit{com}(\textit{sync}) \rightarrow \textit{com}(\textit{R}_y) & \\
\hline
\textit{We define the relation \textit{pp-sync} between instruction instances, }\textit{A} \textit{wx}_x, \textit{pp-sync} \textit{B} \textit{wy}_x \textit{... as follows:} & \\
\hline
\begin{align*}
\textit{ww}_{x} & \rightarrow \textit{R}_y, \quad \text{if } A \sim B \\
\textit{pp}_A(\textit{wx}_x) & \rightarrow \textit{sat}(\textit{R}_y), \quad \text{if } A \not\sim B
\end{align*}
\hline
\end{tabular}
\caption{Summary of relations used in the ARMv7 axiomatic model}
\end{table}

\textit{Lemma 2. The following properties involve \textit{pp-sync} and \textit{po-sync}:

(i) } \textit{A} \textit{wx}_x, \textit{pp-sync} \textit{B} \textit{wy}_x, \quad \textit{R}_x, \textit{po-sync} \textit{B}' \textit{R}_x, \quad \Rightarrow \quad \textit{A} \textit{wx}_x, \textit{pp-sync} \textit{B}' \textit{R}_x, \\
\quad \textit{R}_x
\hline
\textit{Lemma 3. The following properties involving \textit{pp-sync} apply:

(i) } \textit{A} \textit{wx}_x, \textit{pp-sync} \textit{B} \textit{wy}_x, \quad \textit{R}_x, \textit{po-sync} \textit{B}' \textit{R}_x, \quad \Rightarrow \quad \textit{A} \textit{wx}_x, \textit{pp-sync} \textit{B}' \textit{R}_x, \\
\quad \textit{R}_x
\hline
\textit{Proof. We prove each case separately:

(i) If the write and the reads happen in the same thread, then all instruction instances belong to that thread, and \textit{program order} prevails. Otherwise, either } \textit{A} \textit{wx}_x, \textit{po-sync} \textit{B}' \textit{R}_x, \textit{... and the result is immediate, or } \textit{A} \textit{wx}_x, \textit{pp-sync} \textit{B}' \textit{R}_x, \textit{... implies the following:} \\
\textit{com}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{R}_x), \textit{by definition of \textit{loc-sync}}. \quad \Rightarrow \quad \textit{pp}_B(\textit{A} \textit{wx}_x) \rightarrow \textit{sat}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{R}_x) \rightarrow \textit{com}(\textit{R}_y), \textit{pp}_B(\textit{A} \textit{wx}_x)
\hline
\textit{Proof. We prove each case separately:

(i) If the write and the reads happen in the same thread, then all instruction instances belong to that thread, and \textit{program order} prevails. Otherwise, either } \textit{A} \textit{wx}_x, \textit{po-sync} \textit{B}' \textit{R}_x, \textit{... and the result is immediate, or } \textit{A} \textit{wx}_x, \textit{pp-sync} \textit{B}' \textit{R}_x, \textit{... implies the following:} \\
\textit{com}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{R}_x), \textit{by definition of \textit{loc-sync}}. \quad \Rightarrow \quad \textit{pp}_B(\textit{A} \textit{wx}_x) \rightarrow \textit{sat}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{R}_x) \rightarrow \textit{com}(\textit{R}_y), \textit{pp}_B(\textit{A} \textit{wx}_x)
\hline
\textit{Proof of Lemma 2:

(i) If the write and the reads happen in the same thread, then all instruction instances belong to that thread, and \textit{program order} prevails. Otherwise, either } \textit{A} \textit{wx}_x, \textit{po-sync} \textit{B}' \textit{R}_x, \textit{... and the result is immediate, or } \textit{A} \textit{wx}_x, \textit{pp-sync} \textit{B}' \textit{R}_x, \textit{... implies the following:} \\
\textit{com}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{R}_x), \textit{by definition of \textit{loc-sync}}. \quad \Rightarrow \quad \textit{pp}_B(\textit{A} \textit{wx}_x) \rightarrow \textit{sat}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{R}_x) \rightarrow \textit{com}(\textit{R}_y), \textit{pp}_B(\textit{A} \textit{wx}_x)
\hline
\textit{Proof of Lemma 3:

(i) If the write and the reads happen in the same thread, then all instruction instances belong to that thread, and \textit{program order} prevails. Otherwise, either } \textit{A} \textit{wx}_x, \textit{po-sync} \textit{B}' \textit{R}_x, \textit{... and the result is immediate, or } \textit{A} \textit{wx}_x, \textit{pp-sync} \textit{B}' \textit{R}_x, \textit{... implies the following:} \\
\textit{com}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{R}_x), \textit{by definition of \textit{loc-sync}}. \quad \Rightarrow \quad \textit{pp}_B(\textit{A} \textit{wx}_x) \rightarrow \textit{sat}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{B}' \textit{R}_y) \rightarrow \textit{com}(\textit{R}_x) \rightarrow \textit{com}(\textit{R}_y), \textit{pp}_B(\textit{A} \textit{wx}_x)
\hline
\end{table}

\textit{1 Note that } \textit{pp-sync} \textit{does not imply an \textit{event happens-before order} on the events making up the related instruction instances.}
4.2 Execution paths

We consider the three operations of the work-stealing algorithm: take, push and steal. Each of them exhibits different execution paths depending on control flow. Data and address dependences are implicit in the notations and are omitted for brevity. Control dependences are implied by the guard conditions in each case and are also omitted, but we explicit the constraints on the b and t variables carrying the control dependence. Greek letters $\beta$, $\tau$, $\xi$ denote the memory values of b, t, and some $x_i$, respectively. Reads and writes are annotated with the corresponding line from Figure 2.

For take and steal, we say that an instance of the operation is successful if it returns one element; otherwise (including if it returns empty) it is considered failed.

4.2.1 Take

Two failure cases return no element (empty), and two success cases return one element from the deque. All four paths start with:

(a) \( R_b, \beta \xrightarrow{\tau} (b) Ra, x, W_b, \beta - 1 \xrightarrow{\tau} (d) Rt, \tau \)

Specific continuations for each path are listed.

Return empty without CAS, $\beta - \tau \leq 0$: …

Return empty with (failed) CAS, $\beta - \tau = 1$, $\tau \neq \tau'$:

Return one without CAS, $\beta - \tau > 1$:

Return one with (successful) CAS, $\beta - \tau = 1$:

4.2.2 Push

There are two paths: a straight case, and a resizing case which grows the underlying circular buf.

Straight, $\beta - \tau = \text{size}(x) - 1$:

Resizing, $\beta - \tau \geq \text{size}(x) - 1$:

where $z'$ refers to the new array

Resize:

where $\text{resize} = R_x, \xi \xrightarrow{P_0} W_x', \xi \xrightarrow{P_0} \ldots \xrightarrow{P_0} R_x'_{\beta-1}, \xi - 1 \xrightarrow{P_0} W_x'_{\beta-1}, \xi - 1 \xrightarrow{P_0} W_x, \ldots$

4.2.3 Steal

There are three paths: two failure cases and one success case. Failure returns no element and success returns a stolen element.

Return empty without CAS, $\beta - \tau \leq 0$:

Return empty with (failed) CAS, $\beta - \tau > 0$:

Return one with (successful) CAS, $\beta - \tau > 0$:

4.3 Significant reads and writes

We define the sequence $\langle \beta_n \rangle$ of values taken by the variable $b$ over the course of the program, according to the write coherence relation. Initially $\beta_0 = 0$. Since all $push$ and $take$ operations occur in a single thread, and $steal$ operations never alter the value of $b$, the elements of $\langle \beta_n \rangle$ correspond to writes to $b$ in program order within the $push$ and $take$ operations. Similarly, we define the sequence $\langle \tau_n \rangle$ of values taken by the variable $t$. We assume $\tau_0 = 0$.

Furthermore, since all writes to $t$ are from CAS instructions, which are sequentially ordered, and all such CAS instructions increment $t$ by one, $\langle \tau_n \rangle$ is monotonically increasing, and s.t. $\tau_n = m$.

For each index $i$, we define the sequence $\langle \xi^i_n \rangle_{n \in \mathbb{N}}$ of successively given to the element at index $i$ in the deque by the last write $W_{x_i}$, of a push operation, regardless of the address $&x$ of the underlying array. Only the last such write is called significant as it induces a new value in an $\langle \xi^i \rangle$ sequence, while writes due to resizing do not. For all $i$, $\xi^i_1$, the value before the first significant write to $x_i$ location, is undefined: $\xi^i_1 = \bot$. Similarly, a read is significant if it occurs in a successful instance of $take$ or $steal$.

4.4.1.1 Lemma

For all $i$, $\langle \xi^i \rangle$ is globally coherent.

Proof. Given two significant writes $W_{x_i}$ and $W_{x_j}$ at index i (regardless of the address of the underlying array). If $W_{x_i}$ and $W_{x_j}$ both write to the same memory location, then they are ordered by write coherence. If they do not, then there must be a resize operation after the first write and before the second (all writes happen in the same thread). Because of the cumulative barrier after a resize operation, threads that see the second value must have seen the first beforehand. Hence, there is a global coherence order on the writes, which corresponds to the order of push operations.

We define the relation $\text{read from}$ as follows: for some memory locations $m_0, \ldots, m_n$ and some value $v$, $W_{m_0}, v \xrightarrow{p} W_{m_n}, v$ if $W_{m_0}, v \xrightarrow{p} W_{m_n}, v$ or there exists a sequence of copies carrying the value of the write to the read: $W_{m_0}, v \xrightarrow{R_{m_0}}, v \xrightarrow{R_{m_1}}, \ldots \xrightarrow{R_{m_n}}, v \xrightarrow{R_{m_n}}, v$.

For conciseness, we hereafter omit the variable name from reads and writes whenever the variable can be inferred from the value: e.g., $W_{b_3}$ stands for $Wb, b_0$. Let $W_{\xi^i_1}$ denote the first significant write at index $i$, and $\xi_n^i$ a significant read s.t. $W_{\xi^i_1} \xrightarrow{R_n} W_{\xi^i_1}$.

5.5.1 Lemma

Given a write $W_{x_i}$ and a read $R_{x_j}$, $i \neq j$ \implies $W_{x_i} \xrightarrow{R_n} W_{x_j}$.

Proof. If the addresses of the underlying arrays differ, then the memory locations read and written are distinct and there can be no $read from$ relation.

Otherwise, since old arrays are never reused, the addresses are the same and $i \equiv j \mod \text{size}(x)$ $R_{x_j}$ belongs to a successful instance of $take$, with (resizing), or steal. Let $X$ be that instance.

Let $P$ be the instance of push to which $W_{x_i}$ belongs. In $P$, we have the following execution graph:

where $\tau_P \leq \tau_0$ and $\tau_0 - \tau_P < \text{size}(x) - 1$

Let us assume $i \neq j \land W_{x_i} \xrightarrow{R_n} R_{x_j}$, and show it is indeed impossible.

Assume $X$ is a successful instance of $take$ or $push$. Since $X$ and $P$ belong to the same thread, $P$ must occur before $X$ in program order (the order of loads and stores to the same location is preserved: $P; W_{x_i} \xrightarrow{R_n} X; R_{x_j}$).

If $j < i$, then $j \leq i - \text{size}(x)$. However, the following must hold in $P$:

hence $j < i - \text{size}(x) + 1 \leq \beta_0 - \text{size}(x) + 1 < \tau_P$

Furthermore, if $X$ is a take operation, $R_{x_j}$ reads the last element of the deque, and $j = X - 1 \geq \tau_X$; if $X$ is a $push$ operation, $R_{x_j}$ results from a copy operation of the resizing code, hence $j \geq \tau_X$. Since $X$ occurs after $P$ in program order and $t$ is monotonically increasing, $P; R_{x_j} \xrightarrow{R_n} X; R_{x_j}$ and $\tau_P + \tau < \tau_X \leq j$. Impossible.

If $i < j$, then, since $j \geq \beta_0$, $b$ must increase from $\beta_0 + 1$ to $j + 1$ between the write in $P$ and the read in $X$. Hence, there must be an instance $P'$ of $push$ between $P$ and $X$ (in program order) that increments $b$ to $j + 1$. Indeed, the only writes that increase the value of $b$ occur in $push$ and $take$, and the effect of $take$ as a whole never increases the value of $b$ since it first
Given a significant write

\[ W_i X. \]

Corollary 1.

Hence, from Lemma 2 (ii), \( W_i X. \) is an instance of \( W_i X. \).

\[ W_i X. \]

It follows from Lemma 2 (ii) that \( \xi \) refers to the same memory location or they do not.

Lemma 6. Given a significant write \( W_i X. \) and a significant read \( R_i X. \):

\[ (i) W_i X. R_i X. \Rightarrow u \leq v 

(ii) 0 < u \leq v \Rightarrow W_i X. R_i X. \]

Proof. We prove each point separately:

(i) Suppose \( u < v \). We define \( W_i X. \) as follows,

(ii) Suppose \( u = v \). We define \( W_i X. \) as follows,

If \( v = 0 \), \( \xi \) is an undefined value; let \( W_i X. \) be the initialization of \( x_i \). The sequence of \( W_i X. \) comes before \( W_i X. \) in program order.

Otherwise, \( 0 < v < u \). Let \( W_i X. \) be the significant write s.t. \( W_i X. \) refers to \( x_i \). In other words, there exists a sequence of copies carrying the value of \( x_i \) to \( x_i \). That sequence ends with a write \( W_i X. \) and the semantics of reszing, \( W_i X. \) and \( W_i X. \) must come before \( W_i X. \) in program order.

We have two cases: either \( W_i X. \) and \( x_i \) refer to the same memory location or they do not.

Assume that they refer to the same memory location \( x_i \). Then it must be that \( W_i X. \) and \( W_i X. \).

Hence, from Lemma 2 (ii), \( W_i X. \) and \( W_i X. \). Impossible.

Conversely, assume that they do not refer to the same memory location.

Then there must be a resize operation between \( W_i X. \) and \( W_i X. \).

\[ W_i X. \]

From Lemma 3 (ii), \( W_i X. \) and \( W_i X. \).

And from Lemma 2 (ii), \( W_i X. \) and \( W_i X. \).

Then there must be a resize operation between \( W_i X. \) and \( W_i X. \).

Hence, from Lemma 3 (ii), \( W_i X. \) and \( W_i X. \).

\[ W_i X. \]

Corollary 2 (Well-defined significant reads). Given a significant read \( R_i X. \), \( \xi \) for some \( v > 0 \).

Proof. Let \( X \) be the significant instance of \( take \) or \( steal \) s.t. \( R_i X. \).

Suppose \( \xi \neq \xi \), then \( \xi \) can only be an undefined value from the uninitialized array, prior to copying. Indeed, if \( \xi \) is not affected by copying, then it must be one of the new slots allocated by the resizing, hence its initial value is \( \xi \).

Let \( R \) be the push operation that allocates the array. There always exists a \( \xi \), such that:

\[ W_i X. \]

It follows from Lemmas 2 (iii), 3 (i) and 2 (ii) that \( W_i X. \).

Impossible.

Hence, \( \xi \neq \xi \).

We have \( R_i x_i \neq R_i x_i \). Since all resize operations allocate new arrays, \( x_i \neq x_i \), which contradicts our premises. Otherwise, \( x_i \neq x_i \) refer to the same memory location \( x_i \), then it comes be-

It follows from Lemma 2 (i), \( W_i X. \).

Hence, from Lemma 2 (ii), \( W_i X. \).

Corollary 1. Given a significant write \( W_i X. \) and a significant read \( R_i X. \):

\[ i \neq j \Rightarrow W_i X. \]

Proof. If \( i \neq j \), we know that \( W_i X. \) and \( W_j X. \). Furthermore, all copies, which happen during a resize operation, copy from and to the same index. Since there are less copies than the size of the expanded array, there can be no two copies writing to the same memory location in the new array. Hence, there can be no sequence of copies from \( W_i X. \) to \( W_j X. \).

Lemma 6. Given a significant write \( W_i X. \) and a significant read \( R_i X. \):

\[ (i) W_i X. R_i X. \Rightarrow u \leq v 

(ii) 0 < u \leq v \Rightarrow W_i X. R_i X. \]

Proof. We prove each point separately:

(i) Suppose \( u < v \). We define \( W_i X. \) as follows,

(ii) Suppose \( u = v \). We define \( W_i X. \) as follows,

\[ W_i X. \]

Theorem 1 (Work-stealing: uniqueness of significant reads). Given a worker thread executing a sequence of \( push \) and \( take \) operations, and finite number iterator of \( steal \) threads each executing steal operations, all against a same deque. If \( X \) and \( Y \) are two distinct successful instances of steal or take,

\[ \forall R_i X. \in X, \forall R_i X. \in Y, i \neq i \land v \neq v \]

Lemma 7. Given \( S_1 \) and \( S_2 \) distinct successful instances of steal,

\[ \forall R_i X. \in S_1, \forall R_i X. \in S_2, i \neq i \]

Proof. All writes to \( t \) atomically increment it (by atomically CAS). Hence two successful steal operations cannot write (thus read) the same value of \( t \). Reads from \( x \) in a steal operation access the index given by the value of the \( t \) variable. Hence \( R_i t \), \( i \in S_1 \) and \( R_i t \), \( i \in S_2 \) imply \( i \neq i \).
Lemma 8. Given $T$ a successful instance of take and $P$ an instance of push. If $P$ comes after $T$ in program order, then:
\[
\forall \xi_i^p \in T, \forall \omega_i^w \in P, i \neq j \vee v \neq u
\]
Proof. Assume $i = j \wedge v = u$. We have $\xi_i^p \mapsto \omega_i^w$, therefore $W_i^\xi \mapsto W_i^\omega$. From Lemma 6 (ii), it follows that $u > v$. We have a contradiction.

Lemma 9. Given $T_1$ and $T_2$ distinct successful instances of take, $\forall \xi_i^p \in T_1, \forall \omega_i^w \in T_2, i \neq i' \vee v \neq v'$
Proof. We have the following execution graphs:
\[
T_1: R_b \mapsto R_a \mapsto W_b, \beta_i - 1 \mapsto R_t \mapsto R_{\beta_i - 1} \mapsto \cdots
\]
\[
T_2: R_b \mapsto R_a \mapsto W_b, \beta_i - 1 \mapsto R_t \mapsto R_{\beta_i - 1} \mapsto \cdots
\]
And $\beta_i - 1 = i$ and $\beta_i = i'$. Since all instances of take occur in the worker thread, we have either: $T_1: W_b, R_{\beta_i - 1} \rightarrow T_2: R_{\beta_i'}$ or $T_2: W_b, R_{\beta_i'} \rightarrow T_1: R_{\beta_i}$. Let us assume the first case as well as $\xi_i^p \mapsto \omega_i^w$. Impossible, the other case being symmetrical.

Lemma 10. Given $T$ a successful instance of take and $S$ a successful instance of steal, $\forall \xi_i^p \in T, \forall \omega_i^w \in S, i \neq i' \vee v \neq v'$
Proof. We have the following execution graphs:
\[
T: R_b \mapsto R_a \mapsto W_b, \beta_i - 1 \mapsto R_t \mapsto R_{\beta_i - 1} \mapsto \cdots
\]
\[
S: R_p \mapsto R_a \mapsto W_p, \beta_i - 1 \mapsto R_t \mapsto R_{\beta_i - 1} \mapsto \cdots
\]
with $\beta_i - 1 = i$ and $\nu_i = i'$. Let us assume $i = i' \vee v = v'$. Then $\nu_i = i' = i = \beta_i - 1$. For $S$ to succeed, we must have $\beta_i' \leq \beta_i$. Also, for $T$ to succeed, we must have $\beta_i < \beta_i'$. Two cases:
- If $\beta_i = \nu_i + 1$, then a successful CAS occurs in $T$. Moreover, $\beta_i = \nu_i + 1$ implies $\nu_i = \beta_i = \nu_i + 1$, hence $\nu_i = \nu_i + 1$. Impossible since $t$ is monotonically increasing and $S$ also contain a successful CAS with the same value of $t$.
- If $\beta_i > \nu_i + 1$, then no CAS occurs in $T$ and $\nu_i' > \nu_i$. Since $t$ monotonically increases, there must be not less than two writes $B.W \mapsto A.W \mapsto B.W$. Therefore, $\xi_i^p \mapsto \omega_i^w$.

4.5 Existence of significant reads

Theorem 2. Work-stealing: existence of significant reads. Consider a worker thread executing a sequence of push and take operations, and a finite number of thief threads each executing steal operations, all against a same deque. If the number of push is finite, then all threads reach a stationary state where $b = t$ in a finite number of transitions, and the following holds globally:
\[
\forall \xi_i^p, v > 0 \Rightarrow \exists \omega_i^w \text{ in some thread before the stationary point}
\]

Proof. We have two cases:
- Assume $X$ is an instance of take. $X$ follows $P_T$ in program order: $P_T, R_{T+m} \mapsto P_T, R_{T+m} \mapsto P_T, R_{T+m}$ by uniprocessor constraints.
- Assume $X$ is an instance of steal. Since $X$ is successful, $X$ contains a successful instance of a CAS instruction, hence the two reads from $t$ must yield the same value. Due to the barrier between $X.R_{\beta_i}$ and the barrier following $X.R_{\beta_i}$, we have:
\[
W_{T+m} \mapsto P_T, R_{T+m} \mapsto W_{T+m} \mapsto W_{T+m} \mapsto X.R_{\beta_i} \mapsto R_{T+m}
\]
From Lemma 3 (ii), we have $W_{T+m} \mapsto R_{T+m} \mapsto X.R_{\beta_i} \mapsto \cdots$. It then follows from Lemma 3 (i) that $W_{T+m} \mapsto R_{T+m} \mapsto X.R_{\beta_i}$. Total order on CAS instructions and Lemma 2 (ii) guarantee that $V_k < m.F, W_{T+m} \mapsto W_{T+m} \mapsto R_{T+m} \mapsto R_{T+m}$. Therefore, $m \geq m.F$.

4.6 Corollary 3. The combined number of successful stealing instances of take and steal is less than or equal to $\beta_{N_{\beta_T}} - T_{m_F}$.

Proof. Let $X$ be a successful stealing instance of take and steal, and $R_{b_{\beta_T}} \in X$ and $R_{T+m} \in X$. We know that $n \geq n_{m_T}$ (by definition) and $m \geq m_{m_T}$ (from Lemma 11). Hence $\tau_{m_T} \leq \tau_{m_{m_T}}$. Furthermore, a take operation always contains one decrementing write to $b$ by one, which may be followed by one incrementing write to $b$ by one. Hence $n \geq n_{m_T}$ implies $\beta_n \leq \beta_{m_T}$.

Therefore, $X$ can only read at an index $i$, s.t. $\tau_{m_{m_T}} \leq i < \beta_{m_T}$, where $\tau_{m_{m_T}}$ tells there can be no more than $\beta_{m_T} - \tau_{m_{m_T}}$ such $X$.}

Lemma 13. There is a finite number of successful (traveling or non-traveling) instances of take or steal.

Proof. It follows from Corollary 3 that there is a finite number of successful stealing instances of take or steal. Furthermore, there must be a finite number of non-traveling take operations, which come before $P_T$ in program order.

Lastly, there is a finite number of push operations, thus $\beta_n$ has a maximum, $\beta_{\text{max}}$. Since two successful steal operations must read different values of $t < \tau$ less than some value of $b$, there can be no more than $\beta_{\text{max}}$ successful instances of steal.

Hence the finite number of successful instances of take or steal.

Lemma 14. In each thread, there exists $X$ a failed instance of take or steal $\forall \beta_n \in X \neq X.R_{\tau_{m_T}}$.

Proof. Assume $X$ is a failed instance of take or steal $\forall \beta_n \in X \neq X.R_{\tau_{m_T}}$. From Lemma 6 (ii), it follows that $u > v$. We have a contradiction.
thread makes no more than \(1 + m_F + \beta_{n_F} - \tau_{n_F}\) attempts at take or steal that result in a failed CAS instruction.\(^2\)

**Proof.** It follows from Lemma 13 that there is a finite number of successful instances, hence a finite number per thread. Thus, there must exist a failed instance of take or steal.

A failure can occur either because the deque is empty (\(\beta_{n_F} \leq \tau_{n_F}\)) or because of a failed CAS instruction. Suppose there is no \(X\) where \(\beta_{n_F} \leq \tau_{n_F}\); then all failures must be due to a failed CAS instruction. A failed CAS occurs if the two values of \(t\) read during the instance \(X\) differ. Let \(Y_1\) and \(Y_2\) be two such failed instances executing in a same thread; let us assume that \(Y_2\) follows \(Y_1\) in program order, \(n_1 \neq n_1′\) and \(n_2 = n_2′\):

\[
Y_1, R_{n_1} \overset{\text{po-lc}}{\rightarrow} R_{n_1′} \overset{\text{po-lc}}{\rightarrow} Y_2, R_{n_2} \overset{\text{po-lc}}{\rightarrow} R_{n_2′}
\]

There exists a write \(W_{n_1} \overset{\text{rf}}{\rightarrow} Y_1, R_{n_1′} \overset{\text{po-lc}}{\rightarrow} Y_2, R_{n_2} \overset{\text{rf}}{\rightarrow} R_{n_2′}\). Due to Lemma 2 (i), we have \(\text{We} \Rightarrow Y_2, R_{n_2} \Rightarrow\), and, as in the proof of Lemma 11, we deduce that \(n_1′ \leq n_2\).

Since \(n_1 \neq n_1′\) and \(n_2 = n_2′\) and \(t\) is monotonic, it must be that \(n_1 \leq n_1′ \leq n_2 < n_2′\). Hence successive CAS-failing instances in a same thread read increasing values of \(t\). It follows from Corollary 3 that \(t\) takes no more than \(1 + m_F + \beta_{n_F} - \tau_{n_F}\) different values.

Therefore, there can be no more than \(1 + m_F + \beta_{n_F} - \tau_{n_F}\) CAS-failing instances of take or steal per thread. Since there is also a finite number of successful such instances, any further take or steal operations must return empty, and the thread reaches its stationary point.

**Corollary 4.** The combined number of successful (trailing or not) instances of take and steal is equal to the number of push.

**Proof.** A successful instance of take either decreases the value of \(b\) by one or increases the value of \(t\) by one; a successful instance of steal increases the value of \(t\) by one. An instance of push increases the value of \(b\) by one.

It follows from the previous lemma that the worker thread reaches a stationary point where \(b = t\). Clearly, this cannot occur before all push operations and all successful instances of take have occurred.

Since \(b = t\) at the stationary point and all increases to \(b\) precede the sum of increases to \(t\) and decreases to \(b\) (the combined number of successful instances of take and steal) must be at least equal to the number of increases to \(b\) (the number of push operations). It is exactly equal, as otherwise there would be more significant reads than significant writes, which is impossible according to Theorem 1.

One may finally prove Theorem 2. On the one hand, Corollary 4 tells that the number of significant reads (from a successful instance of take or steal) is equal to the number of significant writes (from an instance of push). On the other hand, Theorem 1 states that significant reads uniquely map to significant writes. By injectivity, there exists a unique significant read for each significant write.

### 5. On the C11 implementation

The sequentially consistent implementation is a direct translation of the original algorithm using C11 `seq_cst` atomic variables for all shared accesses. It is obtained from the code in Figure 1 by replacing all memory order constants with `seq_cst`; doing so makes fences unnecessary, hence they should be removed.

The optimized C11 implementation improves upon the previous version by replacing sequential consistency with release-acquire pairs where appropriate. It establishes happens-before relations between reads and writes, as required by the proof. Unfortunately, without relying on `seq_cst`, using only `release`, `acquire` and `consume` operations, we were unable to reproduce the required memory ordering constraints needed on the POWER and ARMv7 architectures while adhering to C11 semantics.

Although designed for ARMv7/POWER, most of the arguments developed in the proof informally translate to the rules of C11 in a straightforward fashion. In all cases that do not involve cumulativity, the `seq_cst` relation (defined in 4.1) combined with dependences, which form the core of the ARMv7/POWER proof, may be replaced with analogous properties pertaining to the C11 happens-before relation combined with release–acquire semantics. The one notable difference between the two models lies in the absence of cumulativity in the design of the C11 abstract machine: neither C11 fences nor C11 atomic accesses guarantee cumulativity. A similar effect can be achieved by chaining alternating release–acquire writes and reads, which form a happens-before path. But this device does not work in situations where propagation needs to be asserted between two reads, rather than a read followed by a write.\(^3\) This situation occurs in the `steal` operation. Informally (see Lemma 10 for the formal description), it must be that two concurrent `steal` and `take` do not read “old” values of both `bottom` and `top`, where “old” could be defined as “older than the value known to the other party in coherence order”. The presence of the two cumulative barriers in `steal` and `take` on ARMv7 guarantee such a condition.

- if the `take` barrier is ordered before the barrier in `steal`, then the program-order-previous write to `bottom` will be propagated to the instance of `steal`;
- conversely, if the `steal` barrier is ordered before the barrier in `take`, then value read by the program-order-previous read from `top` will be propagated to the instance of `take`.

In the second case, it is important to remark that the write that produced the value read in `steal` might belong to another thread, and thus not be sequenced before the barrier. In the absence of cumulativity, it need not be propagated to the instance of `take`.

To enforce this particular case of cumulativity in C11, we rely on the properties of sequential consistency. By making all writes (actually, CAS operations) to `top` sequentially consistent, we ensure that there is a total ordering between the two fences (in `take` and `steal`) and the write that produced the value of `top` read in the instance of `steal`. Furthermore, if that read uses acquire semantics, then there is a happens-before relation between it and the `steal` barrier. Hence, the write must come before said barrier in `sequential consistency total order`. Then, either the barrier in `steal` is ordered before the barrier in `take`, or the other way around:

- if the `steal` barrier is ordered before the barrier in `take`, then it follows from `seq_cst` barrier semantics that the value of `top` read by `take` cannot be older than the one read in `steal`;
- conversely, if the `take` barrier is ordered before the one in `steal`, then the value of `bottom` read by `steal` cannot be older than the one written in `take`\(^3\).

### 6. Experimental results

We present experimental results on three current and widely used architectures: (1) a Tegra 3 ARMv7 processor rev 9 (v7l) with 4 cores at 1.3GHz and 1GB of RAM; (2) an Intel Core i7-2720QM machine with 4 cores (hyper-threading disabled) at 2.2GHz and 4GB of RAM; and (3) a dual-socket AMD Opteron Magny-Cours 6164HE machine with 2 × 12 cores at 1.7GHz and 16GB of RAM.

All tests were compiled with GCC 4.7.0, the first release of GCC to introduce built-in support for C11 atomics.

\(^2\) Hence a thread eventually reaches a stationary state where \(b = t\); it should be noted that the model does not guarantee progress; it is legal for a thread to end up looping on a non-final state where \(b = t\) but \(b \neq \beta_{n_F}\).

\(^3\) C11 defines a happens-before relation, which does not fully encapsulate the notion of cumulativity. The only inter-thread edges in happens-before come from write–read pairs with release–acquire semantics (see [6] 5.1.2.4p11 and p16). In the absence of a write instruction, no fence or other operation can propagate accumulated information to another thread—in other words, it is not possible to establish a happens-before path between two reads in different threads without an intervening write. Hence the reliance on `seq_cst` primitives, enforcing a `sequentially consistent total order`.\(^4\)


6.1 Synthetic benchmarks

We designed a synthetic benchmark to simulate the depth-first traversal of a balanced tree—with breadth $b$ and depth $d$—of empty tasks by a main worker thread, reproducing the prototypical execution of a Cilk program. One or more thieves attempt to steal these tasks. For robustness and predictability, the worker always creates and pushes the same number of tasks in the deque, following the depth-first pattern, regardless of whether a specific continuation has been stolen by another thread (it is simply recorded as stolen, but subsequent tasks spawn normally and locally). The thieves perform steal actions at a configurable rate, and discard stolen tasks.

We have experimented with two different methods of steal distribution, the goal being to uniformly spread the contention over the entire life of the worker thread. The first method is based on the CPU clock of the core dedicated to each thief; with this technique, the clock is regularly sampled and the appropriate number of steal operations is performed accordingly. The second method relies on a random number generator, called in a busy loop, which allows steal operations with a set probability. While the clock-based approach produces more reliable results, it can only be used if a low-overhead CPU clock is available from user space, which is unfortunately not the case on our ARM-based system. Conversely, the second technique suffers from imprecision when targeting smaller ranges of frequencies, which is necessary on faster processors or when the number of cores increases. Hence, the former is used on x86 and the latter on ARMv7, with appropriate empirical tuning to gather results over a common representative range of steal throughput.

We selected two workloads: a reasonably broad tree ($b = 3; d = 15$) and, as a special case, a degenerate comb-shaped tree ($b = 1; d = 10^5$). The former is meant to reproduce normal contention with steal operations alongside both push and take, while the latter illustrates a case of contention between take and steal only.

We measure the time taken by the worker thread to complete the specified number of task creations and consumptions. This in turn serves to compute the push/take throughput—the combined number of $\text{push}$ and $\text{take}$ operations completed per unit of time, as well as the effective steal throughput, defined as follows: the test protocol strives to perform a number of steals over time, at a fixed, nominal steal throughput; the effective throughput is the real throughput as could be observed after the experiment, i.e., how many steals were actually performed during the lifetime of the worker thread. These metrics provide a measure of the efficiency of the algorithm on its critical path at various levels of contention.

In order to assess the impact of the added barriers on the different architectures, raw throughput values have been normalized by the near-ideal throughput on the same workload (see Table 2), obtained on a single thread with no contention and no synchronization: memory barriers are replaced with simple compiler fences, and CAS operations with a simple branch and conditional assignment. These numbers provide a good approximation of the upper bound on the achievable throughput on each machine, though other minor factors can contribute to higher observable values. In particular, it should be noted that counting the throughput in number of operations per second is, by design, a generalization: the execution time of each operation depends on its nature and the exact control path taken; for example, an invocation of $\text{take}$ returning empty will be faster than one returning a task.

\[\begin{array}{ccc}
\text{Core i7 (2 threads)} & 4.87562 \times 10^8 & 3.60053 \times 10^8 \\
\text{Opteron (2 threads)} & 2.55142 \times 10^8 & 2.04978 \times 10^8 \\
\text{Tegra 3 (2 threads)} & 5.47223 \times 10^7 & 4.12112 \times 10^7 \\
\text{Core i7 (4 threads)} & 4.88618 \times 10^8 & 3.66404 \times 10^8 \\
\text{Opteron (24 threads)} & 2.56214 \times 10^8 & 2.03235 \times 10^8 \\
\text{Tegra 3 (4 threads)} & 5.48473 \times 10^7 & 4.11242 \times 10^7 \\
\end{array}\]

Table 2. Near-ideal throughput (s$^{-1}$)

All the results based on the mixed push and take “tree” workload show a marked improvement of the hand-written native and cilk versions over the naive sequentially consistent translation of the original Chase–Lev algorithm, seqcst. While the relative gain remains stable at all levels of contention on the Core i7 and Tegra 3, it drops sharply on the Opteron, presumably because of the higher number of cores. Nevertheless, for low values, which more closely model realistic scenarios, the optimized implementations perform at least 1.5 times better than seqcst on both x86 and ARM.

Comparing x86 and ARM, we note that a higher relative throughput is achieved on ARM (peak at above 85%) than on x86 (peak at above 50%), indicating that the first serializing instruction introduced in the code is very costly on x86, especially if it is added to the critical path (as is the case in native, cilk and seqcst, but not in nofences). This could suggest either the stronger guarantees of the x86 memory model—a full memory fence is required to linearize history in order to maintain total store order [13]—or aggressive local optimizations for single-thread execution without communication.

From these observations, we can postulate that advanced ARM architectures such as the Tegra 3 benefit the most from a well-written concurrent program that takes full advantage of the flexibility allowed by their memory model, and conversely struggle relatively more with literal interpretations of algorithms designed with stricter, simpler hypotheses in mind.

6.2 Task-parallel benchmarks

We further experiment on common task-parallel benchmarks, mostly extracted from the Cilk benchmark suite, to evaluate the impact of the memory barrier optimization on realistic workloads and load-balancing scenarios.

Fibonacci is the tree-recursive computation of the 35th Fibonacci number; it illustrates the raw cost of the scheduling algorithm as each task only performs a single addition.

In all diagrams, we have included a set of points labeled nofences, for comparison purposes. These correspond to the least common denominator among all the tested barrier placement strategies: only relaxed CAS operations are included, with otherwise no memory barriers. The nofences version violates the semantics of the work-stealing deque. Each of our proposed implementations of the algorithm can be seen as adding a different set of barriers to nofences, making it correct. Hence, results obtained with nofences should be taken as no more than a general baseline, as the complete lack of fences can lead to unexpected behavior. For instance, Figures 3 and 4 show greater throughput values at high contention for the comb-shaped workload on ARM. Those are the results of a long tail of fast empty take operations, an artifact due to the nature of the comb-shaped test and the absence of synchronization between empty take and steal (enabled by the lack of barriers in take).

6 The ARMv7 C15 cycle counter register can only be queried if first enabled from kernel mode, and is delegated to a monitoring co-processor, with unclear consequences for the bus, caches, and memory model as a whole.

7 On higher end processors with multiple cores acting as thieves, higher steals probability can yield many times more steals attempts than there are tasks created over a set period.

8 In the case where the deque is empty, neither take nor steal needs to execute a CAS instruction; furthermore, in the absence of barriers, the ARMv7 memory model does not require successive decrements and increments of bottom in take to propagate to the thieves.

9 http://supertech.csail.mit.edu/cilk
Figure 3. Synthetic single-thief benchmarks

Figure 4. Synthetic multi-thief benchmarks

Figure 5. Task-parallel benchmark speedups against the C11 sequentially consistent baseline

**FFT-1D** computes the Cooley-Tukey fast Fourier transform over a vector of $2^{20}$ elements.

**Matmul** is the blocked matrix multiplication, of size $256 \times 256$ on the Tegra 3 and Core i7 platforms, and of size $384 \times 384$ on Opteron to ensure a sufficient computation time.

**Strassen** is an optimized matrix multiplication algorithm, running on matrices of size $512 \times 512$ on the Tegra 3 and Core i7 platforms, and of size $2048 \times 2048$ on Opteron.

**Knapack** is the usual resource allocation problem. A set of objects, each with a given weight and value, must be picked from
a pool to fit a total weight constraint while maximizing value. We use 33 objects.

**Seidel** simulates heat transfer using the Gauss-Seidel method which iterates a 5-point stencil over an two-dimensional array. We used a resolution of 1024×1024 points with 20 iterations.

We compare the four implementations of the Chase–Lev deque presented in Section 2. The sequentially consistent, direct translation to C11 serves as a baseline to measure the speedups obtained with the three other implementations. We observe that the **nofences** version is inherently incorrect and generally results in erroneous executions. This version is only presented as a rough upper-bound on the performance gains of memory barrier optimization.

Figure 5 shows similar trends to the balanced tree synthetic kernel, with a clear advantage to the two optimized implementations (**native** and **c11**) over the seqcst baseline. **Fibonacci**, **FFT-1D**, **Matmul** and **Strassen** use a recursive divide-and-conquer pattern, leading to balanced binary trees. They appear in increasing order of granularity, ranging from a single addition to the multiplication of matrix blocks of size 16×16. On **Fibonacci**, the lowest granularity kernel, the results are very similar to the throughput achieved by the synthetic benchmark: the optimized versions show up to 1.19× speedup on the Tegra 3 platform against the seqcst version, 1.3× on Core i7 and up to 1.13× on Opteron. These speedups gradually decrease as granularity increases, hiding the cost of the scheduling deque. Yet we still observe significant speedups on the Matmul kernel, with a granularity of 64 (vector) multiply-add operations per task: we obtain up to 1.03× speedup on Tegra 3, 1.1× on Core i7 and 1.04× on Opteron. On Strassen, the largest granularity kernel, we no longer observe any significant improvement: the deque operations are entirely hidden by the work performed in each task.

The **Knapsack** kernel is also based on a divide-and-conquer pattern, yet it does not result in a balanced tree because of the non-deterministic, dynamic pruning of sub-optimal branches. Unsynchronized communications are used to share the best total value reached on any branch; this value is used to stop exploring branches known to represent sub-optimal prefixes. The **nofences** version shows lower performance, on Tegra 3, than our optimized c11 and native versions because of longer delays until the best value is propagated to all cores, resulting in less pruning and more work. The performance improvement is reduced on this benchmark because additional barriers improve the accuracy on the current best value. Finally, the **Seidel** kernel iterates on skewed wave-fronts of data-parallel tasks. A single main thread is responsible for spawning every task in a wave-front. It en-queues all tasks on its own work-stealing deque until it reaches a synchronization barrier. This scheme relies on stealing exclusively for the distribution of work among cores. This behavior puts a lot of strain on a particular deque, and induces a high level of contention. This explains the high performance gains of our optimized implementations on the 24-core Opteron platform: up to 1.3× speedup against the seqcst baseline, even higher than the speedups observed at a lower granularity on **Fibonacci**. However, despite its somewhat low granularity, corresponding to 16 additions and 4 multiplications of double precision floating point values per task, this benchmark only shows up to 1.05× improvement from our optimized versions on the Tegra 3 platform and up to 1.2× speedup on the Core i7. This is in line with the equivalent speedups observed for the similar granularity on **FFT-1D**, as the low number of cores on these platforms induce much less contention compared to the Opteron configuration.

Interestingly, our experiments show that the performance of our optimized versions is very close to the **nofences** version on the Tegra 3 platform. This validates our hypothesis about the benefits of an implementation that takes full advantage of the ARM relaxed memory model, rather than translating the classical sequentially consistent algorithm. Furthermore, the large performance gains on the two x86 platforms show that even in the case of stricter memory models such as total store order [13], relying on sequentially consistent algorithms represents a significant source of overhead.

### 7. Conclusion

We provided optimized implementations of Chase and Lev’s concurrent deque, targeting the weak memory models of the POWER and ARM processors, as well as the C11 standard. Based on recent progress in the formalization of memory consistency, we established the first proof of the Chase–Lev deque for the weak memory model of a real-world processor. This paves the way for robust parallel library and programming language implementations based on a work-stealing scheduler.

Comparing our optimized implementation with portable C11 versions, we observed unrecoverable overheads in the interaction between atomic operations and the non-cumulativity of memory barriers in C11, a slight mismatch with the POWER and ARM memory models. We obtained strong performance gains on ARM and x86, and performance levels comparable to an (incorrect) fence-free version. This indicates that a high-throughput scheduler can be implemented efficiently on a weak memory model such as a multicore ARM, benefitting from its scalability and energy savings.

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### References


