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To cite this version:
Louis Mandel, Florence Plateau, Marc Pouzet. Static Scheduling of Latency Insensitive Designs with Lucy-n. FMCAD 2011 - Formal Methods in Computer Aided Design, Oct 2011, Austin, TX, United States. hal-00654843

HAL Id: hal-00654843
https://inria.hal.science/hal-00654843
Submitted on 23 Dec 2011

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Static Scheduling of Latency Insensitive Designs with Lucy-n

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Abstract—Lucy-n is a data-flow programming language similar to Lustre extended with a buffer operator. It is based on the n-synchronous model which was initially introduced for programming multimedia streaming applications. In this article, we show that Lucy-n is also applicable to model Latency Insensitive Designs (LID). In order to model latency introduced by wires, we add a delay operator. Thanks to this new operator, a LID can be described by a Lucy-n program. Then, the Lucy-n compiler automatically provides static schedules for computation nodes and buffer sizes needed in shell wrappers.

I. INTRODUCTION

The theory of Latency Insensitive Design ([11], [2]) was introduced to cope with the problem of long wires in Systems on Chips (SoC). Due to the length of wires, data can take more than a single clock cycle to go from one computation node (also known as Intellectual-Property or IP) to another. It raises the issues of activating IPs only when all inputs are available and storing the inputs awaiting to be processed. They are treated by encapsulating each computation node in a process, called a shell wrapper, that is used as a communication interface. In order to synchronize all the inputs, the shell wrappers have a buffer on each input wire. To respect the desired clock period, long wires are split into shorter segments by inserting relay nodes, called relay stations.

Different dynamic scheduling protocols for the shell wrappers have been proposed [2], [3]. Those protocols use back pressure mechanisms to inform the producer node that the consumer node has no more room to keep the inputs waiting to be processed. When a producer node is not executed, the shell wrapper has to inform the consumer node through a control channel that no valid inputs have been sent.

To avoid the communication overhead introduced by these dynamic protocols, static scheduling methods have been proposed [4], [5], [6], [7], [8]. Schedules are represented as ultimately periodic binary words indicating the instants where nodes have to be executed.

The schedules of [4], [5] and [6] fire the execution of the nodes As-Soon-As-Possible (ASAP). While in [7] a well-balanced schedule is sought in order to minimize buffer sizes for a fixed rate. This method is semi-automatic: prefixes of schedules must be found by hand. The approach of [8] is to search for schedules that can be shared between several IPs. The advantage of this method is that it reduces the complexity of the algorithm which finds the schedules and simplifies the circuits needed to generate them.

The approaches for finding schedules are either analytic [4], [7] or based on simulation [6], [8].

This paper presents a novel analytic way to compute static schedules for Latency Insensitive Designs by encoding LID models in the n-synchronous language Lucy-n [9], [10]. The schedules obtained by the Lucy-n compiler are not yet as good as the ones obtained by previous techniques. However, the advantage of our technique is to be able to compose modularly IPs that have already been statically scheduled. This can be useful for example when IP blocks are provided as black boxes. These Statically Scheduled IPs (SSIPs) have the particularity of not reading all their inputs nor writing all their outputs at each activation.

The paper is organized as follows. Section II presents the Lucy-n language. Section III explains how to encode LID models in this language and presents the new delay operator that is mandatory for the encoding. Section IV defines the typing of our new operator and presents a way of solving the typing constraints. Section V discuss the composition of SSIPs. Section VI presents experimental results. Finally, section VII concludes.

The Lucy-n compiler, the complete code of the paper examples and additional materials are available at http://www.lri.fr/~mandel/lucy-n/fmcad11.

II. A BRIEF OVERVIEW OF LUCY-N

Lucy-n [10] is a programming language similar to the synchronous data-flow language Lustre [11] extended with a build-in buffer operator. The goal of this language is to relax synchrony constraints by inserting buffers without abandoning the guaranties given by synchrony, namely, determinism and execution in bounded time and memory. To this end, the compiler must compute both static schedules so that executions can be performed with finite buffer sizes and the buffer sizes themselves.

We present the language through the example of a cyclic encoder that takes as input a stream of bits and returns as output the same stream where after every 50 bits are added 3 redundancy bits. The program is given Figure 1.

The input flow i goes into a redundancy node that computes three flows of redundancy bits (line 2): bit0, bit1

```cpp
i = (i & 0xFFFFF0) + (i & 0x00000F) * 3;
```

Output of the redundancy node: bit0, bit1.
let node cyclic_encoding i = o3 where rec (bit0, bit1, bit2) = redundancy i and o1 = merge (1 ∘ 50 0) i (buffer bit0) and o2 = merge (1 ∘ 51 0) (buffer bit1) and o3 = merge (1 ∘ 52 0) o2 (buffer bit2)

\( \forall \alpha. \alpha \text{ on } (1^50) \rightarrow \alpha \text{ on } (0^501) \times \alpha \text{ on } (0^501) \times \alpha \text{ on } (0^501) \)

Fig. 1. Graphical and textual representation of a cyclic encoder in Lucy-n.

This rule indicates that in the typing environment \( H \), the expression \( \text{merge ce e}_1 \ e_2 \) has type \( ct \) if: (1) the merging condition \( ce \) has type \( ct \), (2) the expression \( e_1 \) has type \( ct \) on \( ce \) and (3) the expression \( e_2 \) has type \( ct \) on \( \text{not ce} \). It expresses the synchronous semantics of the \( \text{merge} \) operator: with respect to a rhythm \( ct \), the presence instants of the flow \( e_2 \) (i.e. \( \text{not ce} \)) are the complement of the presence instants of the flow \( e_1 \) (i.e. \( ce \)), and the output flow of the \( \text{merge} \) is present at each instant of the reference rhythm \( ct \).

In the \( n \)-synchronous language Lucy-n, the buffer operator relaxes the synchronous hypothesis by introducing of a subtyping rule to the clock calculus.

\[
H \vdash e : ct \quad ct \ll : ct' \\
H \vdash \text{buffer } e : ct'
\]

This typing rule means that if an expression \( e \) has type \( ct \) and if clocks represented by \( ct \) are \( \text{adaptable} \) to clocks represented by \( ct' \), then we can use the results of \( e \) on the type \( ct' \) provided we store them in a buffer. The adaptability relation ensures that such buffers are bounded. It is denoted \( w_1 < : w_2 \) where \( w_1 \) is the clock of writes into the buffer and \( w_2 \) is the clock of reads, and it is defined as the conjunction of two conditions. First, no reads may occur on an empty buffer, i.e. the \( j \)th reading in a buffer must always occur after the \( j \)th writing. Second, there must be a bounded number of values in the buffer, i.e. the difference between the number of writes and reads since the beginning of an execution must be bounded. These conditions can be checked at compile time provided clocks are periodic.

The clock calculus automatically infers the type of the flows. For example, the type inferred for the entire \( \text{cyclic_encoding} \) node is: \( \forall \alpha. \alpha \text{ on } (1^500^3) \rightarrow \alpha \).\(^2\) From such types, it is possible to build a static schedule for the program and to compute the buffer sizes needed. Here, the compiler finds that the node \( \text{cyclic_encoding} \) can be executed without buffering \( \text{bit0} \) and with buffers of size one for \( \text{bit1} \) and \( \text{bit2} \). For more information about Lucy-n and its type system refer to [13], [10], [14].

III. LID ENCODING IN LUCY-N

To illustrate the encoding of Latency Insensitive Designs in Lucy-n, we use the first example given in [4]. We first model the synchronous circuit of Figure 2(a), and then we model the variation of Figure 2(b) where a relay station is added to model a communication latency from \( B \) to \( A \).

\(^1\)In the rest of the article, we use the term \( \text{type} \) instead of \( \text{clock type} \) since data types are not considered here.

\(^2\)This type shows that the input must be absent during the insertion of the redundancy bits into the output.
A. Encoding of Computation Nodes

In the theory of LID, each computation node or IP reads all its input and produces all its outputs at each activation. Hence, IPs are encoded as Lucy-n nodes of clock \( \forall \alpha. \alpha \times \cdots \times \alpha \rightarrow \alpha \times \cdots \times \alpha \). Since we do not have to know the behavior of the IPs to compute the scheduling of the system, the IPs can be represented as dummy nodes with the correct clock type. For example, the IPs of Figure 2 can be modeled as:

\[
\begin{align*}
\text{let node ip}_A & \ x = x \\
\text{let node ip}_B & \ x = x
\end{align*}
\]

B. Encoding of Wires

In the synchronous circuits described in [4], data takes one clock cycle to go from one IP to another. Hence, a wire cannot be represented as a Lucy-n variable, because variables in synchronous languages model instantaneous communication channels. We thus model wires with a new operator, called delay, that transmits its input to its output with one instant of delay. With this operator, a wire from a source src to a destination dst is written:

\[
dst = \text{delay src}
\]

To put an initial value on a wire as \( A_0 \) and \( B_0 \) in the example of Figure 2(a), we use the merge operator with the condition 1(0).

\[
dst = \text{merge} \ 1(0) \ \text{init} \ (\text{delay src})
\]

The condition 1(0) equals 1 at the first instant then 0 forever. So, at the first instant, the value init is transmitted to the destination dst. Then, thereafter, the values coming from the source src are transmitted.

Now, following the encoding of computation nodes and wires, we can program the example of Figure 2(a):

\[
\begin{align*}
\text{let node figure}_2a \ (\text{init}_A0, \ \text{init}_B0) &= \ (\text{out}_A, \ \text{out}_B) \ \text{where} \\
\ \text{rec out}_A &= \ \text{ip}_A \ \text{in}_A \\
\ \text{and out}_B &= \ \text{ip}_B \ \text{in}_B \\
\ \text{and in}_A &= \ \text{merge} \ 1(0) \ \text{init}_B0 \ (\text{delay} \ \text{out}_B) \\
\ \text{and in}_B &= \ \text{merge} \ 1(0) \ \text{init}_A0 \ (\text{delay} \ \text{out}_A)
\end{align*}
\]

In this node, out_A and out_B are the flows of values computed by the IPs A and B. The definitions of in_A and in_B describe the wires between A and B. The node

\[
\begin{align*}
\text{let node figure}_2b \ (\text{init}_A0, \ \text{init}_B0) &= \ (\text{out}_A, \ \text{out}_B) \ \text{where} \\
\ \text{rec out}_A &= \ \text{ip}_A \ \text{in}_A \\
\ \text{and out}_B &= \ \text{ip}_B \ \text{in}_B \\
\ \text{and in}_A &= \ \text{delay} \ \text{out}_R \\
\ \text{and in}_B &= \ \text{delay} \ \text{out}_R
\end{align*}
\]

The type of the node computed by the compiler is equal to

\[
\forall \alpha. \alpha \ \text{on} \ 1(0) \times \alpha \ \text{on} \ 1(0) \rightarrow \alpha \times \alpha
\]

It means that the initial values need only be present at the first instant and that the two IPs produce some outputs at each instant. Since the presence instants of IPs outputs correspond to their activation instants, output types give the activation instants of the IPs, i.e. their static schedules. Here, we can verify that in the case of the synchronous circuits, all the IPs must be executed at the same instants.

C. Encoding of Shell Wrappers

In latency insensitive designs, each computation node is enclosed inside a shell wrapper that controls the activation of the node and bufferizes the inputs until this activation. To model this behavior, we need only put a buffer in front of each input and the activation condition will be automatically computed by the clock calculus. Hence, if we want to put the ip_A of the previous example in a shell wrapper, we only have to write:

\[
\begin{align*}
\text{out}_A &= \ \text{ip}_A \ (\text{buffer} \ \text{in}_A)
\end{align*}
\]

D. Encoding of Relay Stations

A relay station is just a dummy node that splits a wire into two segments and thus introduces a delay.

\[
\begin{align*}
\text{let node relay} & \ x = x
\end{align*}
\]

Now that we have presented the encoding of computation nodes, wires, shell wrappers and relay stations, we can model the circuit of Figure 2(b).

3Even if the pre operator of Lustre introduces a delay, it does not have exactly the same semantics as the one of delay. If we consider a flow x of clock (100), the values of x are output by pre x on the clock 000(100) whereas they are output by delay x on the clock 0(100). The pre operator outputs a value only when a new input arrives.

4Notice that there is no initial value on the wire between the relay station and the ip_A (line 6).
VI. COMPOSITION OF STATISTICALLY SCHEDULED IPs

To the best of our knowledge, the only work on the composition of Statically Scheduled IPs (SSIPs) is [15], where different composition techniques are proposed depending on the nature of SSIPs involved.

For SSIPs where the same number of values are consumed and produced on all ports, they propose using dynamic scheduling protocols like those used in the dynamic scheduling of LIDs. If it is not the case, they propose encoding the composition of SSIPs with Synchronous Data-Flow graphs (SDF) [16]. This encoding is similar to the encoding of Cyclo-Static SDF graphs [17] into SDF. It raises two problems. First, the initial phases of the schedules cannot be encoded. Second, the encoding is an abstraction where some information is lost and thus correct networks with cycles may be rejected.

In the context of Lucy-n, the composition of SSIPs is classical node composition. Indeed, in Lucy-n nodes, consumption and production patterns are arbitrarily complex ultimately periodic binary words, so SSIPs are Lucy-n nodes. We think that the main strength of our method is that it treats with IPs and SSIPs uniformly.

VI. EXPERIMENT

One of the LIDs that we have encoded is shown in Figure 3. It is the MPEG-2 video encoder from [2] where the relay stations are at the same places as in [4]. This program is compiled by the Lucy-n compiler in less than 0.1 seconds and has the following type:

\[
\text{mpeg} :: \forall \alpha. \alpha \text{ on } (10) \rightarrow \alpha \text{ on } 0(10)
\]

The throughput of the solution computed with our algorithm is 1/2 whereas the one of the solution computed in [4] is 2/3. Nevertheless, the programmer can give a hint to the compiler with an option `-nbones 2` asking it to seek a solution with twice as many 1s in the periodic pattern of the schedule. With this option, the new solution is:

\[
\text{mpeg} :: \forall \alpha. \alpha \text{ on } (110) \rightarrow \alpha \text{ on } 00(101)
\]

with a throughput of 2/3.

5As \(\defeq\) is antisymmetric, equality constraints can be translated into two inverse adaptability constraints.
6The compilation line is: `lucync -nbones 2 -obj r mpeg.ls`
For the moment, only a few small-scale experiments have been performed, but thanks to our experiments on other Lucy-n programs [14], we think that it is possible to schedule systems with hundreds of elements.

VII. Conclusion

The contribution of this paper is the introduction of a delay operator to the language Lucy-n and a demonstration of its utility for modeling Latency Insensitive Designs. The benefit of modeling LIDs in Lucy-n is that it gives a new algorithm to automatically compute static schedules for the designs. The advantage of this method is that it allows designs that have already been scheduled to be incorporated in compositions.

We are working to improve the quality of the schedules. We can already influence the resolution algorithm by choosing the number of 1s in the sought solution and by giving different objective functions during step 4 of the typing algorithm, for instance to privilege buffer sizes or throughput. Nevertheless, we do not yet have optimality results. Thus, we hope to adapt the results of the works cited in this article. Note, however, that our problem is more difficult because the consumption and production patterns are more complex. But, this is precisely why we can deal with IPs and SSIPs uniformly.

ACKNOWLEDGMENT

The authors would like to thank the anonymous reviewers for their useful remarks and Timothy Bourke for its careful reading of the paper.

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